



Research on Low Power Analog Integrated Circuit Design Technology

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Abstract. This paper delves into the critical issue of power consumption in analog integrated circuits and explores a wide range of optimization techniques spanning from Register Transfer Level (RTL) design to back-end implementation. Power consumption has become a growing concern in modern circuit design, as it directly impacts system performance, reliability, and energy efficiency. By identifying key factors contributing to power dissipation, this study proposes targeted solutions that address these challenges at various stages of the design process. The proposed optimization methods are validated through their application to an actual chip design, demonstrating their effectiveness in achieving significant reductions in power consumption without compromising performance. The results highlight that by thoughtfully combining multiple optimization techniques, designers can attain substantial power savings while maintaining flexibility to adapt strategies to specific design requirements. This approach ensures that the balance between performance and power optimization is preserved, preventing any degradation in system functionality. Furthermore, the implementation of these strategies lowers the operating temperature of chips, improves system reliability, and mitigates risks associated with leakage, overheating, and thermal-induced failures. This study provides a practical and systematic framework for low-power design in modern integrated circuits, addressing key challenges in energy-efficient, high-performance electronic systems.

Keywords: Power Consumption, Chip Design, Analog Integrated Circuit.

1 Introduction

Low-power design has become a critical focus in modern integrated circuit (IC) technology due to its extensive applications and its significant role in ensuring system performance, energy efficiency, and reliability. The exponential growth in computational demands, coupled with the miniaturization of IC components, has resulted in power consumption becoming a primary concern for designers. Excessive power consumption in chips can lead to a sharp rise in temperature, which, in turn, causes several adverse effects. One of the most significant issues is thermal-induced leakage, where increased temperatures exacerbate leakage currents in transistors,

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leading to higher power dissipation. This not only degrades the chip's performance but also risks permanent damage to the chip and associated system equipment. Additionally, excessive heat can compromise the reliability of electronic systems, causing failures in both the short and long term. As chips become more complex and densely packed, the challenge of managing power consumption grows exponentially, necessitating innovative and efficient design strategies to address these issues [1, 2].

One of the primary motivations for low-power design is the need to mitigate the negative effects of overheating. By effectively reducing power consumption, designers can lower the operating temperature of the chip, thereby enhancing the stability and reliability of the chip and the overall system. Furthermore, reduced power consumption extends the lifespan of electronic devices by minimizing wear and tear caused by thermal stress. This is particularly critical in applications such as portable electronics, IoT devices, medical equipment, and large-scale data centers, where energy efficiency and system reliability are paramount. Low-power design also has environmental implications, as it contributes to reduced energy consumption and carbon emissions, aligning with the global push toward sustainable technology solutions.

To address the growing demands for low-power circuits, researchers and engineers have developed a wide range of techniques. These span from architectural and algorithmic optimizations to transistor-level innovations. For example, at the Register Transfer Level (RTL), power-aware techniques such as clock gating and power gating can significantly reduce dynamic and leakage power. Similarly, at the back-end implementation stage, layout optimizations and advanced fabrication technologies, such as FinFETs and near-threshold voltage (NTV) designs, play a crucial role in minimizing power dissipation [3]. By employing these methods in combination, designers can achieve substantial power savings without compromising performance, thus enabling the creation of high-performance, energy-efficient chips for modern applications.

As the demand for portable and battery-operated devices continues to rise, low-power design has become a fundamental aspect of all stages of IC development. It is no longer sufficient to focus solely on improving performance; achieving high performance must now go hand-in-hand with minimizing power consumption. This paradigm shift has inspired the development of holistic design methodologies that integrate power management at every level, from system architecture to circuit layout.

This study delves into various low-power design strategies, analyzing their effectiveness and trade-offs in real-world scenarios. By applying these methods to practical chip designs, it provides insights into how these techniques can mitigate power-related challenges while enhancing overall system functionality. The findings presented here aim to contribute to the advancement of low-power design practices, offering a framework for engineers seeking to develop energy-efficient, reliable, and high-performance integrated circuits [4, 5].

2 Low Power Analog Integrated Circuit Design Technology

Tsung-Heng Tsai and colleagues conducted a detailed study on designing energy-conscious analog integrated circuits specifically for wireless electrocardiogram (ECG) acquisition systems, as presented in their publication, "Low-Power Analog Integrated Circuits for Wireless ECG Acquisition Systems." Their research highlights the vital role of portable and long-term monitoring devices in modern healthcare.

The rising prevalence of chronic cardiovascular diseases, driven by fast-paced lifestyles, has amplified the need for body sensor network technologies in healthcare monitoring. This study utilized the IEEE 802.15.4 standard—well-known for its low-power and cost-effective properties—as the foundation for creating a wireless ECG transceiver integrated circuit. The system was developed to support patient self-monitoring and seamless data communication via interconnected body and local sensor networks. The ECG acquisition board was designed to record physiological signals from the body and converts them into six leads, which were processed using a low-pass filter and a successive approximation ADC. To enhance integration and achieve lower power consumption, two chips were fabricated using the 0.18 μm TSMC CMOS process, creating a compact solution for wearable device applications.

The analog front-end architecture incorporated an OTA-C anti-aliasing filter and a low-power SAADC within the ECG acquisition board. The OTA-C filter was optimized to efficiently capture ECG signals while employing a common-mode feedback circuit to extend battery life. The SAADC, featuring an 8-bit resolution and a 10 KHz sampling rate, adopted multiple low-power techniques to meet system performance requirements. On the transmitter side, the RF front-end employed innovative designs such as a double-balanced upmixer, a multi-tanh doublet for enhanced linearity, a diode linearizer to manage gain compression, and a QVCO with subharmonic and injection-locked mechanisms to reduce both power consumption and chip size.

The receiver's RF front-end utilized a current-reused folded design, which integrated a low-noise amplifier, a differential power splitter, and a quadrature mixer. By operating the transistors in the subthreshold region, the design reduced noise and power consumption while improving gain efficiency. Experimental results confirmed the system's high-level performance. The ECG acquisition board accurately captured and processed signals, while the RF front-end ensured reliable data transmission and reception in compliance with the IEEE 802.15.4 standard. Future work aims to integrate all analog front-end components into a single chip, achieving further miniaturization and power efficiency for wearable ECG monitoring devices [6].

Refet Firat Yazicioglu and collaborators proposed a 30 μW Analog Signal Processor (ASP) Application Specific Integrated Circuit (ASIC) for ambulatory biopotential signal monitoring in their work, "A 30 μW Analog Signal Processor ASIC for Biomedical Signal Monitoring." This innovation tackled critical challenges such as power consumption and motion artifact interference in portable biomedical systems.

While advancements in biopotential readout circuits have improved energy efficiency, digital signal processing and wireless communication remain significant

power drains. Furthermore, motion artifacts present persistent challenges, requiring advanced solutions to maintain signal fidelity. The ASP was meticulously designed to address these issues, extracting ECG signals with minimal power usage while improving system performance. It incorporated an ECG readout channel, quadrature impedance monitoring channels, fluctuation tracking channels, and an activity detector. Chopper-stabilized instrumentation amplifiers enhanced the Common Mode Rejection Ratio (CMRR) and reduced flicker noise. By sharing a single input stage across multiple signal paths, the ASP achieved better power efficiency than traditional designs.

Motion artifacts were mitigated by measuring electrode-tissue impedance without interrupting ECG signal acquisition. This was accomplished through the application of AC currents to the electrode-tissue interface, with low-pass filters separating impedance and ECG signals in the frequency domain. A key feature of the ASP was its activity detector, which dynamically adjusted the ADC sampling rate based on the frequency content of the ECG signal. When high-frequency components, such as QRS complexes or motion artifacts, were identified, the sampling rate increased from 64Hz to 1024Hz, optimizing power consumption in digital processing and wireless communication.

Performance evaluations demonstrated the ASP's effectiveness, consuming less than $13.5\mu\text{A}$ from a 2V supply with the activity detector active. The system reliably detected high-frequency components and distinguished between QRS complexes and motion artifacts, leveraging impedance measurement channels. By focusing on system-wide power efficiency rather than just the readout front-end, the ASP provided a robust solution for ambulatory biomedical signal monitoring [7].

In their research, "A Fully Digital Front-End Architecture for ECG Acquisition System with 0.5 V Supply," Maryam Zare and Mohammad Maymandi-Nejad introduced an all-digital front-end design for ECG acquisition systems using an ultra-low supply voltage of 0.5 V. Their work aimed to overcome the limitations of traditional analog-based designs under low-voltage conditions and meet the rising demand for compact, energy-efficient biomedical devices (Fig. 1).

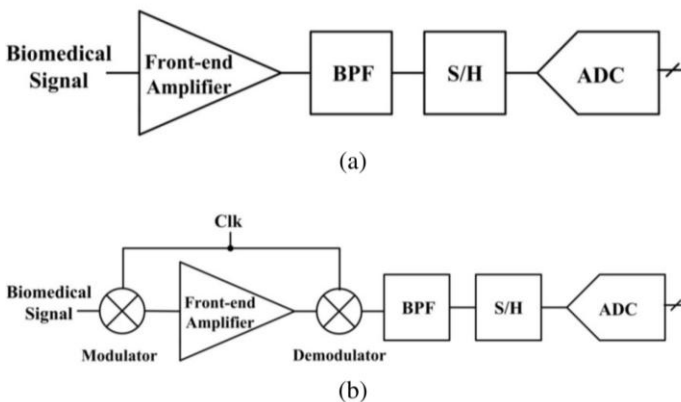


Fig. 1. Biomedical signal acquisition system [8].

As CMOS technology advances, supply voltages for integrated circuits continue to decrease. However, conventional biomedical signal acquisition systems relying on analog components face challenges such as reduced voltage headroom and increased energy consumption. To address these limitations, the researchers transitioned signal processing to the digital domain, proposing a fully digital architecture.

At the heart of the system is a voltage-to-time converter (VTC), which transforms analog ECG signals into time-domain representations. These representations are further processed by a moving average voltage-to-time converter (MA-VTC), which functions as both an anti-aliasing filter and a noise-reducing integrator. A novel offset cancellation technique, involving digital feedback loops and high-pass filtering, was implemented to handle electrode DC offsets, ensuring accurate signal processing. Fabricated using 0.18- μm CMOS technology, the system operates in the subthreshold region to minimize energy consumption. Simulations revealed that the circuit consumed just 274 nW and successfully reduced offset voltages from 50 mV to under 5 mV. Tested with ECG signals from the MIT-BIH arrhythmia database, the system demonstrated reliable signal reproduction, making it a promising solution for modern compact biomedical devices [8].

Yu-Cheng Su and colleagues developed a wireless ECG detection system, integrating a low-power analog front-end (LPAF) circuit with Bio-processing ZigBee (BioZigbee) firmware, as detailed in "Wireless ECG Detection System with Low-Power Analog Front-End Circuit and Bio-Processing ZigBee Firmware." This innovation was tailored to meet the growing demand for portable, energy-efficient ECG monitoring devices, particularly in home care settings.

As medical diagnostic technologies advance, achieving portability and prolonged operation requires minimizing power consumption. The system combines effective ECG acquisition, signal processing, and wireless data transmission while maintaining low energy requirements. The LPAF circuit includes an acquisition board and a low-pass filter. The acquisition board features an instrumentation amplifier, high-pass and notch filters, and a common-level adjuster to pre-amplify weak ECG signals. The low-pass filter, fabricated using 0.18 μm TSMC CMOS technology, operates at a 1 V supply and consumes just 453 nW, filtering out high-frequency noise. The high-pass filter eliminates noise below 0.1 Hz, ensuring clean signal capture.

The BioZigbee firmware handles system operations, from digitizing ECG signals via an ADC controller to optimizing data resolution for transmission. Digitized data is sent via ZigBee technology, displayed on a graphical interface, and stored for further analysis. Tests on human subjects validated the system's effectiveness, demonstrating smooth integration between the LPAF circuit and BioZigbee firmware. Future work will focus on integrating all components into a single chip to achieve even lower power consumption and a more compact design for wearable ECG monitoring devices [9].

Yan Li et al. conducted an extensive review of analog integrated circuit (IC) design techniques for processing physiological signals in their study, "Analog Integrated Circuits Design for Processing Physiological Signals." With the increasing prevalence of chronic diseases and a growing focus on proactive healthcare, wearable and implantable medical devices have become essential. Analog ICs, as core components of these devices, face unique challenges due to the distinct characteristics of physiological signals.

Physiological signals, including bio-potentials, chemical quantities, and physical quantities, are typically characterized by low frequency and small amplitude, often accompanied by noise contamination. As a result, analog ICs for processing these signals must exhibit low power consumption, low cutoff frequency, and minimal input-referred noise.

The review discussed various low-power design techniques. Subthreshold circuits, which bias MOSFETs in the subthreshold region, were highlighted for their ability to significantly reduce power consumption while increasing gain and minimizing input-referred noise. Other methods, such as low-threshold-voltage designs using bulk-driven or floating-gate MOSFETs, were introduced for enabling operation at lower supply voltages. The log-companding technique, leveraging the current-voltage behavior of semiconductors, was also reviewed as a method to reduce power at the circuit level.

For low-frequency designs, strategies to achieve large time constants were detailed. MOS pseudo-resistors, which achieve high resistance in the subthreshold region, were emphasized for their use in neural recording circuits. Additionally, filter designs such as OTA-C filters and current-steering filters were explored, demonstrating how small transconductances and large capacitances can meet the requirements for processing physiological signals.

To address noise challenges, chopper stabilization (CHS) emerged as a key technique, modulating signals to higher frequencies to avoid $1/f$ noise and then demodulating them after amplification. Auto-zeroing and other noise-optimization methods were also discussed. Applications of analog ICs in diverse physiological domains were reviewed, including bioelectrical signal processing (ECG, EEG, neural recording, pacemakers), acoustic signal processing (breathing detection, bionic ear processors), and physical and chemical quantity measurements (photoplethysmography, bladder pressure, ion-sensitive sensors).

In conclusion, this review highlighted the importance of innovative design techniques for addressing challenges in analog IC design for medical applications. As the demand for medical ICs grows, new methods are needed to enhance performance, reduce power consumption, and minimize device size, enabling the development of advanced wearable and implantable medical devices [10].

3 Conclusion

Low-power design in analog integrated circuits is pivotal in tackling the challenges of escalating power demands in modern electronic systems. This paper explores diverse strategies and methodologies aimed at reducing power consumption across applications, including biomedical devices, physiological signal processing, and wireless health monitoring systems. It highlights innovative techniques implemented across various design stages, from Register Transfer Level (RTL) to back-end processing, as well as advancements in fabrication technologies such as subthreshold circuits, FinFET architectures, and near-threshold voltage (NTV) approaches.

Case studies, including implementations like wireless ECG acquisition systems, analog signal processors, and fully digital front-end architectures, illustrate how combining architectural optimization with circuit-level innovations leads to

substantial power reductions while maintaining system performance and reliability. These solutions not only enhance system efficiency but also improve device portability and integration, addressing the needs of modern healthcare, wearable devices, and IoT applications.

The analysis underscores the necessity of balancing power efficiency with performance requirements, presenting a comprehensive framework for designing high-performance, energy-efficient analog ICs. As technology continues to evolve, the adoption of low-power techniques will remain a cornerstone in the development of compact, reliable, and sustainable electronic systems, driving future advancements in both consumer electronics and medical technology.

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