



# Advancements in STT-MRAM Circuit Design for Enhanced Write Efficiency and Reliability

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**Abstract.** STT-MRAM excels with fast reads, low write power, and high endurance, making it a key focus in emerging non-volatile memory research. However, write randomness, different P and AP write times, and temperature fluctuations challenge write efficiency and reliability. Fixed write cycle designs ensure state switching but waste power. This paper examines optimized write self-termination, write driver, word line driver, and peripheral auxiliary circuits for write. Write self-termination circuits save energy by detecting MTJ resistance changes to stop the write operation early. They each have advantages in terms of area, sensing margin, and speed, but they cannot balance all of them. In addition, in high-density and high-capacity storage, the parasitic capacitance effect and IR drop will reduce the drive ability of the write driver circuit. So this article also studies the write drive circuit, word line drive circuit, and peripheral auxiliary circuit to improve the write drive ability.

**Keywords:** STT-MRAM, Write driver circuits, Write self-termination circuits, Word line driver circuits, Peripheral auxiliary circuits

## 1 Introduction

Emerging non-volatile memory is a research hotspot in recent years, among which magnetic random access memory (MRAM) has attracted much attention due to its unique advantages. MRAM has two branches: spin-transfer torque magnetic random access memory (STT-MRAM), spin-orbit torque magnetic random access memory (SOT-MRAM), and voltage-controlled magnetic anisotropy magnetic random access memory (VCMA-MRAM). Compared with toggle MRAM, STT-MRAM has significantly lower write energy consumption and higher integration. Its disadvantage is poor thermal stability. The benefits of SOT-MRAM include higher speed and higher reliability in applications [1]. The drawback is the challenge of mass production [2]. The core of the STT-MRAM storage cell is an MTJ, which is composed of two ferromagnetic layers with different thickness and a layer of several nanometer-thick nonmagnetic isolation layers. It writes information through spin current. STT-MRAM has reading speed, low writing power consumption, and high

durability comparable to SRAM, which gives it great potential in high-performance computing, embedded systems, and artificial intelligence [3-5].

However, the write drive capability limits the efficiency and reliability of write operations. STT-MRAM has write randomness, and P and AP state that write times are asymmetrical [6]. Traditional writing operations usually rely on fixed write cycles to ensure the MTJ state can be successfully reversed under the worst conditions. However, this method results in additional power consumption overhead.

This article investigates STT-MRAM's write self-termination circuits, write driver circuits, word line driver circuits, and peripheral auxiliary circuits. Write self-termination circuits detect MTJ resistance changes to terminate write operation subsequently, featuring low energy consumption. Write driver circuits supply current to flip MTJ states, characterized by efficient driving and low stress. Word line driver circuits meet distinct read/write electrical requirements, offering low power consumption. Peripheral auxiliary circuits ensure stable voltage and current, which are distinguished by high reliability.

## 2 Basics of STT-MRAM Storage

### 2.1 Introduction of MTJ in STT-MRAM

Figure 1 shows the structure of the MTJ, the core component of the STT-MRAM storage cell, which consists of two layers of ferromagnetic material separated by an interlayer insulation material [6]. The magnetization direction of the pinned layer is fixed, serving as a reference layer for reading data. The free layer has a variable magnetization direction, which is flipped by the current through the spin transfer torque effect, thus realizing data writing. The Tunnel Barrier is an extremely thin insulator (MgO or Al<sub>2</sub>O<sub>3</sub>) that transfers electrons between the fixed and free layers through the quantum tunneling effect [7]. MTJ is divided into two states: parallel and antiparallel. In the parallel state, the magnetization directions of the pinned layer and the free layer are the same. Electrons with majority spin occupy majority spin states, while those with minority spin occupy minority spin states, showing a low resistance  $R_P$ . In the antiparallel state, the magnetization directions of the pinned layer and the free layer are opposite, electrons with majority spin occupy minority spin states, whereas those with minority spin occupy majority spin states, showing a high resistance  $R_{AP}$  [7]. The resistance change rate is called TMR. The larger the TMR, the greater the sensing margin [8]. Reading stored data by sensing MTJ resistance is the core working principle of MTJ as a storage unit.

### 2.2 Write termination criteria for STT-MRAM

When P is written in STT-MRAM,  $V_{BL}$  decreases more and  $V_{SL}$  increases less. When writing AP,  $V_{BL}$  decreases less and  $V_{SL}$  increases more, as shown in Figure 2 [9]. The traditional method only detects changes in  $\Delta V_{BL}$  or  $\Delta V_{SL}$ . Unilateral detection has a small sensing margin, can not effectively interrupt the circuit, and has high power consumption.

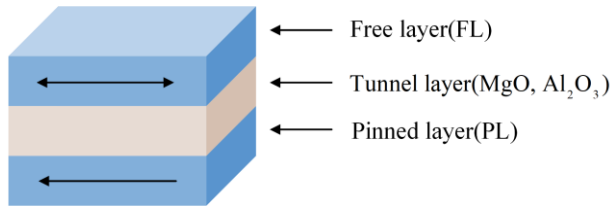


Fig. 1. The structure of MTJ [6]

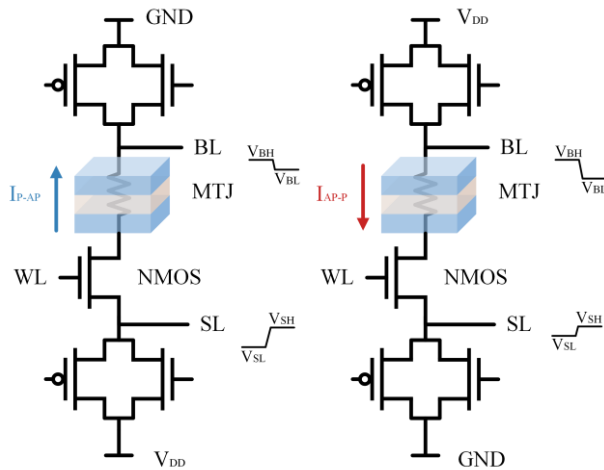


Fig. 2. Voltage characteristics of STT-MRAM [9]

### 3 Development of Writing Circuits in STT-MRAM

#### 3.1 Introduction

Excellent circuit design can optimize the write operation of STT-MRAM, mainly including write drive circuit, write self-termination circuit, word line drive circuit, and peripheral auxiliary circuit. These modules work together to provide sufficient current and voltage to drive the MTJ to complete the state reversal, while minimizing energy consumption.

#### 3.2 Research on Write Self-Termination Circuit

The write self-termination circuit consists of a write-sense circuit and a write termination circuit. The following are several ways to optimize the write-sense circuit.

A paper published in IEEE Transactions on Nanotechnology by Jiangnan University proposes a write self-termination circuit without read verification, as shown in Figure 3 [10]. First, the write self-termination circuit copies the current flowing through the MTJ through the current mirror. For convenience, the circuit only uses one  $V_{REF}$ . When writing P, the circuit opens  $M_{W1}$ ,  $M_{W3}$  and  $M_{W5}$ .  $V_{X0AP}$  is lower

than  $V_{REF}$  before MTJ switching.  $V_{XOP}$  is higher than  $V_{REF}$  after MTJ switching. When writing AP, open  $M_{W2}$ ,  $M_{W4}$  and  $M_{W6}$ .  $V_{X1P}$  is higher than  $V_{REF}$  before MTJ switching.  $V_{X1AP}$  is lower than  $V_{REF}$  after MTJ switching. The values of  $R_0$  and  $R_1$  must satisfy the condition that  $V_{REF}$  lies between the  $V_X$  values before and after the switching. Then the circuit compare the  $V_X$  and  $V_{REF}$  voltages to provide signals for the write termination circuit. The structure has the advantage that the circuit can be terminated in advance to reduce energy consumption. The write-sense circuit requires more transistors, and the energy transmission is delayed. At the same time, it is vulnerable to different MTJ resistances, resulting in a smaller sense margin.

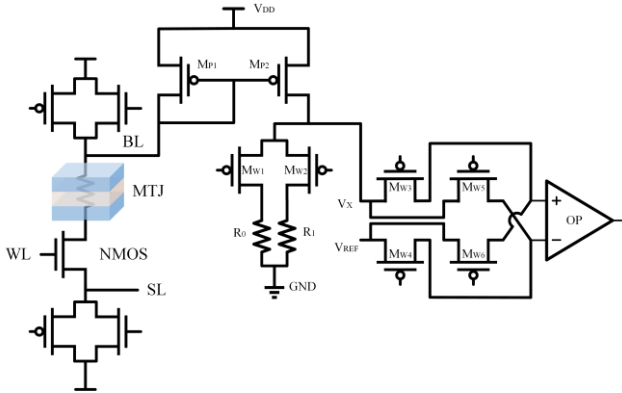


Fig. 3. Write-sensing circuit without read verification [10]

The paper published by the University of Texas at Austin in IEEE Transactions on Very Large-Scale Integration Systems uses a capacitor to store the original voltage of BL, as shown in Figure 4 [11]. After writing, voltage difference on BL is detected. This method avoids the error caused by MTJ process variation and only detects the difference in BL voltage. However, only  $\Delta V_{BL}$  changes are detected. Unilateral detection has a small sensing margin, can not effectively interrupt the circuit, and has high power consumption.

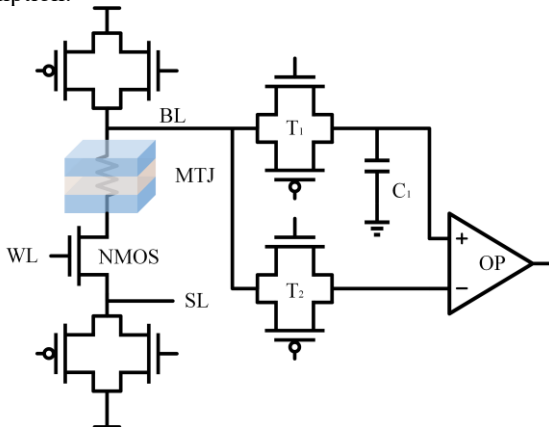


Fig. 4. Write sensing circuit with unilateral difference writing sensing circuit [11]

The paper from Yonsei University, published in IEEE Transactions on Circuits and Systems I: Regular Papers, also proposed the decline of sampling BL when writing P, and the rise of sampling SL when writing AP, as shown in Figure 5 [12]. Whether writing P or AP, the change in detected voltage difference is relatively large. The circuit has high precision, providing accurate signals for the write termination circuit. The disadvantage is that a voltage generator is required, the circuit area is expensive, and the mass production cost is high. Only  $\Delta V_{BL}$  or  $\Delta V_{SL}$  are detected, and the detection margin is relatively small.

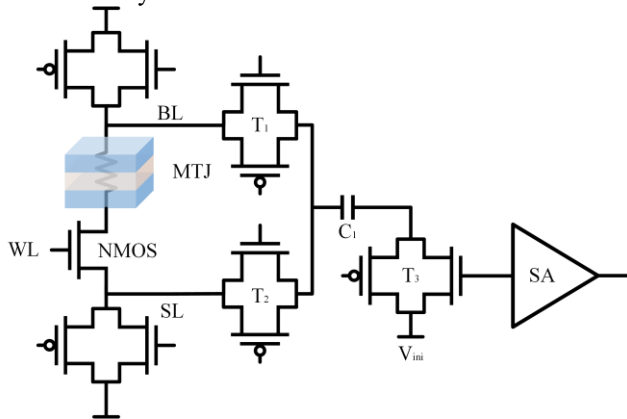


Fig. 5. Write-sensing circuit for detecting the significant difference [12]

The paper published by Jiangnan University in IEEE Transactions on Circuits and Systems I: Regular Papers captures the voltage changes on BL and SL when MTJ resistance changes by storing BL and SL voltage changes through capacitors in Figure 6 [9]. Detect the sum of BL and SL voltage changes, amplify the difference value of the amplifier, and the Schmitt trigger flips the voltage to provide accurate signals for the write termination circuit. The circuit has a large sensing margin, can accurately capture the changes of MTJ, and has high storage accuracy. The disadvantage is that multiple capacitors are used, and the area cost in circuit layout design is very huge.

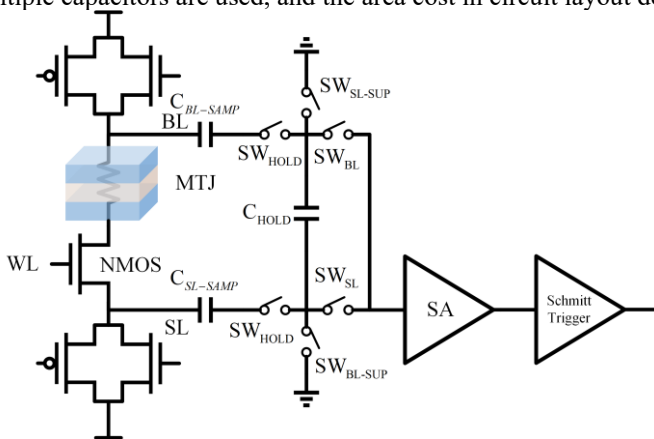


Fig. 6. Write sensing circuit with three capacitors, bilateral difference [9]

A paper published by Aarhus University in IEEE Transactions on Very Large Scale Integration Systems proposes self-referenced write termination circuit in Figure 7 [13]. The circuit using  $0.5V_{DD}$  for original voltage. After performing write operations, it detects the voltage of BL+SL voltage. This method adopts self-referencing bilateral detection, which has a high perceptual margin and avoids errors caused by different BL and SL reference voltages in different MTJ production processes. It detects the BL+SL voltage difference, with low error and high accuracy, providing accurate signals for the write termination circuit. The drawback is the presence of a bias voltage, which can easily terminate the circuit prematurely and cause incorrect operation.

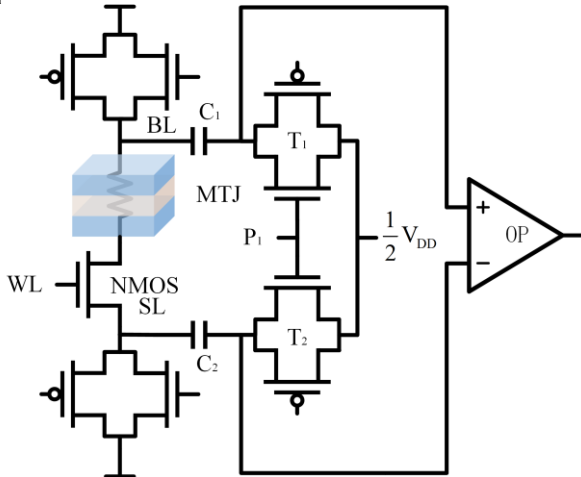


Fig. 7. Write sensing circuit with dual capacitors bilateral difference [13]

The Karlsruhe Institute of Technology proposed a self-timed detection method in a paper published in IEEE Transactions on Very Large Scale Integration Systems in Figure 8 [14]. This circuit uses two different branches, the AP-branch and the P-branch. During the write operation, the structure detects the current difference between data-cell and reference-cell, confirming that the circuit flips correctly. The conversion time from AP to P is short, while the conversion time from P to AP is long. The enable signal times of transistors N13 and N14 are related to the statistical duration of writing P and AP in the paper to ensure the correct writing of data.

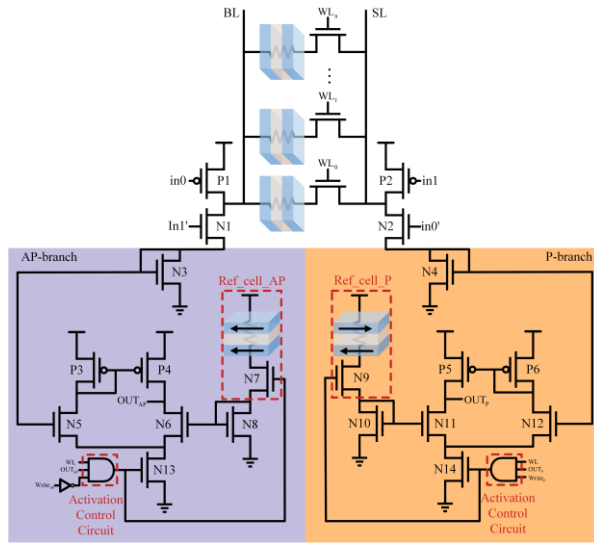


Fig. 8. Self-timed write sensing circuit [14]

### 3.3 Write Driver Circuits and Peripheral Auxiliary Circuits

In high-capacity and high-density storage, the parasitic capacitance effect and IR drop weaken the drive ability of the write drive circuit. So the following section introduces the optimization of write drive circuit, word line drive circuit, and peripheral auxiliary circuit to ensure the high-quality completion of write operation. High driving voltage can easily lead to excessive MTJ current, increasing the stress conditions of tunneling oxides and reducing the lifespan of MTJs [15].

The paper from Intel, published in ISSCC 2019, mentioned a scheme of weak and strong writing, which involves writing a portion of the MTJ with a small voltage in the first attempt, which is weak writing in Figure 9 [16]. After the writing operation is completed, the resistance state of the MTJ is detected, and if writing is performed, the relevant driver is disabled. Otherwise, the MTJ is rewritten with a large voltage, which is strong writing. This scheme can effectively reduce energy consumption, but the disadvantage is that it requires three more ref write cycles to perform a complete write, which requires high agility of the device.

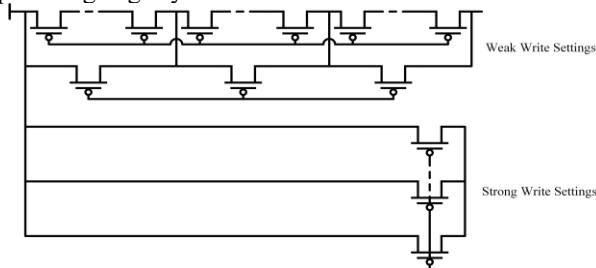


Fig. 9. Secondary write driver circuit [16]

The paper from Purdue University, published in IEEE Transactions on Very Large Scale Integration Systems, mentions multiple efficient ways of peripheral auxiliary circuit [17]. Increasing the access gate voltage  $V_{GS}$  can cause the transistor current to exceed the transition threshold current at lower  $V_{DS}$ . This method ensures the completion of writing.

The TSMC organization's paper published in ISSCC 2024 mentions that the electrical conditions for read and write operations differ, as shown in Figure 10 [18]. Write voltage greater than 1.5V, read voltage less than 1.1V. So, different WL voltages can be output by choosing IO Devices transistor or Core Devices transistor. This circuit meets the requirements of different electrical conditions for reading and writing, reducing the energy consumption of word lines.

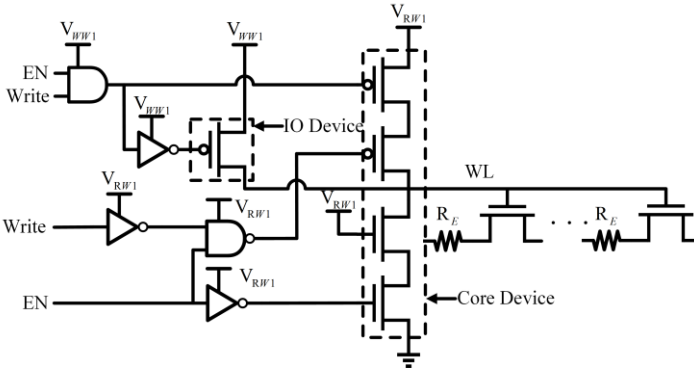


Fig. 10. Independent read and write word line driver circuit [18]

A paper jointly published by KIOXIA Korea and SK Hynix, in ISSCC 2025, introduces different gate voltages for writing AP and P, meeting the requirements of varying writing electrical conditions in Figure 11 [19]. The disadvantage is that no matter how one writes AP or P, one transistor always does not work, which causes the low efficiency of transistor usage.

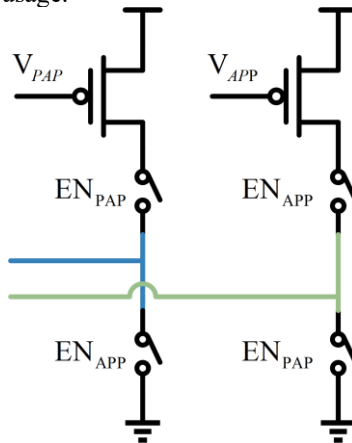


Fig. 11. Single transistor peripheral auxiliary circuit [19]

The TSMC organization's paper published in ISSCC 2024 introduces different driving methods for BL and SL when it writes P and AP in Figure 12 [20]. BL uses dual transistor to pull down and pull up for a high voltage. While SL uses a single transistor to pull down and pull up. Reduced write bias in AP and P by 7% and 9%, respectively, and reduced TMR by 5%.

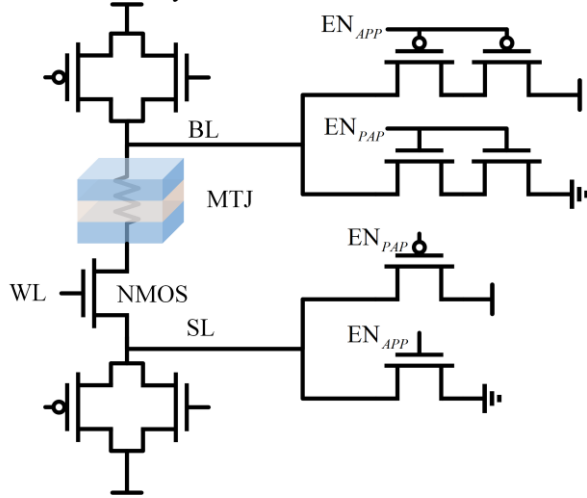


Fig. 12. Dual transistor peripheral auxiliary circuit [20]

Synopsys proposes a new writing strategy, using a mimic bitline to compensate for IR drops on ISOCC 2024 in Figure 13 [21]. The circuit can still maintain a strong driving ability at lower voltage headroom. The purpose of resistance is to sample the voltage drop and compare it with the reference voltage. Then the circuit outputs a digital signal, enabling the corresponding transistor to drive the word line. The advantage of the circuit is that the IR drop is excluded and is independent of process, voltage, and temperature. It also meets the requirement of no standby current and low voltage headroom, to have enough strong driving ability for bitcell.

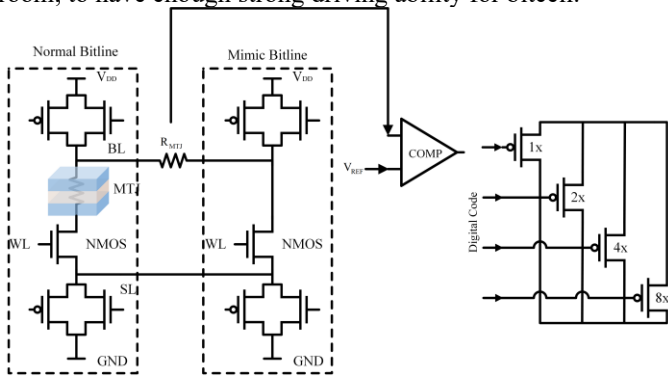


Fig. 13. Digital circuit controls different transistor outputs [21]

## 4 Conclusion

The reliability and efficiency of write operations in STT-MRAM are undermined by issues like write randomness, varying write durations for parallel and antiparallel states, and inconsistencies caused by process variations and temperature changes. Conventional designs that use fixed write cycles guarantee state switching in worst-case conditions but result in considerable power consumption. In high-density storage, the drive circuit is far from the bitcell, leading to a decline in drive capability.

This paper summarizes the fast, low-power write self-termination circuits, write driver circuits, word line drive circuits, and peripheral auxiliary circuits with strong driving ability. In recent years, there has been a lot of research on writing self-terminating circuits. These circuits improve the response margin of MTJ conversion, reduce the detection conversion time to terminate the circuit in-time. Write driver circuits provide different driving voltages according to the electrical signals. Word line driving circuits and peripheral auxiliary circuits also play an important role in driving circuits so that each bitcell can be successfully driven.

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