Traditional and Emerging Memory Technologies: Principles, Applications and Future Trends

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Abstract. Memory is fundamental for preserving and accessing vast amounts of data in the digital age, this paper summarizes the principles, applications, advantages, and disadvantages of various types of memory, including SRAM, DRAM, flash, RRAM, STT-MRAM, FeRAM, and PCRAM. SRAM, used in CPU caches for its high speed at nanosecond seconds, but faces leakage issues and large area. DRAM, the highest-selling IC, employs 1T1C cells, evolving with 3D stacking (HBM, PIM) for high bandwidth. Flash (NAND/NOR) dominates non-volatile storage with 3D stacking but suffers from slow writes. Among emerging memories, RRAM has low voltage and high density, and it is also used in computing-in memory, and STT-MRAM has high speed, high endurance, and due to cross point technology it has ultra-high density. FeRAM replaces the capacitor material on the basis of DRAM, retaining the advantages of DRAM while also having non-volatile properties. PCRAM also has fast speed, high density, and low voltage but struggles with high energy and high cost. In the future, different technologies will be applied to these storage devices based on different needs, playing different roles. Emerging nonvolatile memories, RRAM and STT-MRAM may become the next generation of storage and promote the evolution of the paradigm of "memory computing integration".

Keywords: Memory, Chip, Traditional Memory, Emerging Memory

1 Introduction

Memory plays a critical role in computer systems, as market projections show it will account for 29% (186 billion) of the 650 billion semiconductor market by 2025 [1].

Memory includes volatile memory and non-volatile memory. Traditional memory includes SRAM and DRAM, and Flash is commonly used as traditional non-volatile memory. Emerging non-volatile memory includes RRAM, STT-MRAM, FeRAM, PCRAM.

SRAM has high read and write speed and low read and write power consumption, but it loses data and has high leakage current when it loses power. DRAM has high integration density and low latency, but requires dynamic refresh. Flash, a traditional non-volatile memory, has significant market applications. However, it has slow write speed and high write power consumption. When the CMOS process develops to

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below 28nm, its compatibility with MOS is not good. Emerging memories include FeRAM (DRAM-like with low power but density limitations), PCRAM (fast, reliable but power-hungry and thermally unstable), RRAM (low-voltage, fast, high-capacity but costly), and STT-MRAM (high-speed, high-density, commercialized) [2].

There are many types of memories, and different types of memories are used in different fields, playing different roles. This article will summarize the principles, uses, advantages, and disadvantages of different types of memories.

2 Traditional Memory

2.1 SRAM

SRAM (static random access memory) is widely used as a CPU cache because of its high speed. A typical 6T-SRAM unit is composed of two pairs of transistors and two access transistors, which are controlled by word line (WL) and bit line (BL/BLB). The structure is shown in Fig 1. Its three working states are: hold, write, and read. Due to the dependence on continuous power supply(VDD), SRAM is volatile, and data loss occurs when power is cut off.

SRAM has many other topologies, including 7T, 8T, 9T, and 10T. The following Table 1 lists some SRAM chips from 2020 to 2025 [3-7].

The table shows that 6T SRAM remains the dominant design approach, and these articles are all based on advanced 3nm FinFET technology, with 3nm SRAM becoming relatively mature. In 2024, TSMC Design Technology Japan [3] designed SRAM with low read and write power consumption (3.8/4.1uW/Hz), while Taiwan Semiconductor Manufacturing Company [4] designed SRAM with a large capacity (1280Kb) and high density (28.48Mb/mm2). This indicates two different manufacturing trends have emerged: low-power versions for energy-sensitive applications and high-density variants for storage-intensive uses. In 2025, Taiwan Semiconductor Manufacturing Company (TSMC) designed a high-frequency (4.3GHz), small area (0.0031mm2) SRAM, which shows that frequency and size have also become two research hotspots for precise scenario adaptation [5]. Recent SRAM research prioritizes area and performance optimization. Vertical stacking with complementary transistors shows promise by reducing parasitics [8]. Yu Cheng Lu's conflict-free 4N4P CFET 8T SRAM design demonstrates improved speed, power efficiency, and area savings through double-sided signal routing [9].

Table 1. SRAM chips

	VLSI'24 [3]	**VLSI'24 [4]**	**JSSC'25 [5]**	**JSSC'25 [6]**	**ISSCC'25 [7]**
Technology	3nm FinFET	3nm FinFET	3nm FinFET	3nm FinFET	3nm FinFET
Macro Capacity	288Kb	640/1280Kb	65Kb	N/A	20Kb
Bit Cell Type	6T	6T	6T	6T	6T
Density	5.92	27.48, 28.48	21.1	28.55	8.29

(Mb/mm^2)					
Frequency(GHz)	0.62 - 1.64	2.42, 1.95	4.3(Max)	1.93	3.18(Max)
Supply Voltage(V)	0.5 - 1.24	0.65	1	0.75	1
Read/Write Power (uW/MHz)	3.8/4.1	7.7/9.1, 4.8/5.2	N/A	10.5/11.0	N/A
Macro Area	N/A	N/A	$0.0031mm^2$	$0.0123mm^2$	$0.052um^2$ bitcell

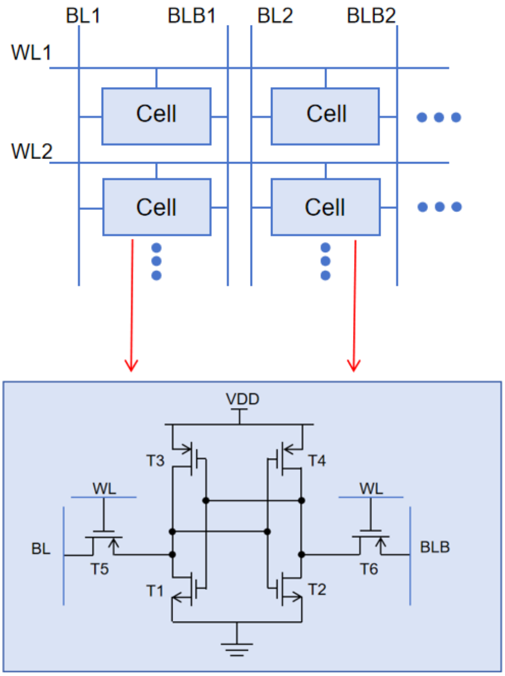


Fig. 1. Array of SRAM and memory unit of 6T-SRAM.

2.2 DRAM

DRAM, the highest-selling IC product, is crucial in modern electronics. The mainstream 1T1C structure uses one transistor and capacitor controlled by WL (write) and BL (read/write). While simple and dense, it requires refresh due to leakage. 2T0C DRAM employs floating-body effects for a smaller area but higher refresh needs, which is ideal for embedded SoCs. The 3T1C structure improved leakage but was phased out due to the large area. 3D stacked DRAM like HBM (High Bandwidth Memory) and PIM (Processing-in-Memory) were developed for higher integration [10]. HBM uses TSV stacking for ultra-high bandwidth but at a higher cost [11]. PIM integrates compute units (adders, multipliers) into DRAM to reduce data movement and boost energy efficiency, though it increases design complexity and thermal challenges [12]. Fig 2 shows a typical 3D stacked DRAM structure.

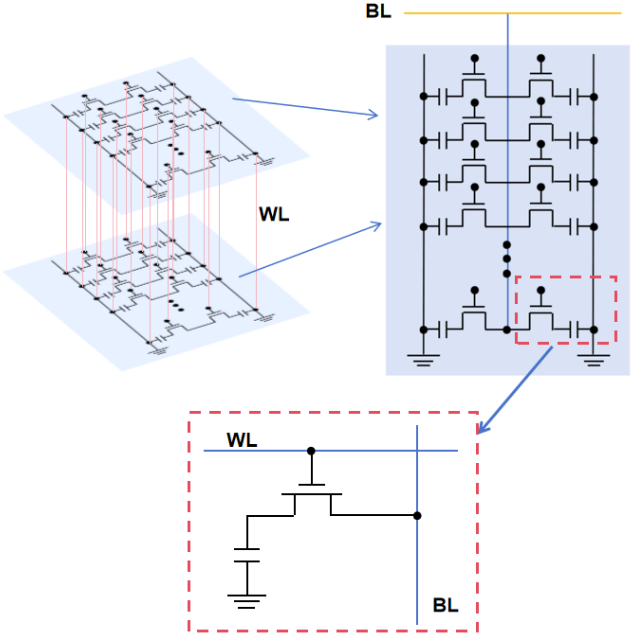


Fig. 2. Stacked array of DRAM and memory unit of DRAM

Table 2. DRAM chips

	TVLSI'19[13]	ISSCC'20[14]	ESSCIRC'21[15]	JSSC'21[16]	ISSCC'23[17]
Technology	55nm	40nm	28nm	28nm	40nm
Architecture	Digital-DLL	Digital-DLL	Digital-DLL	Digital-DLL	Digital-PLL
Clock	Correc.	Correc.	Correc.	Gen./Correc.	Gen./Correc.
Freq. Range	1.0 - 3.0GHz	0.8 - 2.3GHz	0.8 - 3.2GHz	1.3 - 4.0GHz	1.0 - 4.0GHz
Power Cons. @f_{QCLK}	2.1mW @3.0GHz	8.9mW @2.3GHz	9.8mW @3.2GHz	6.5mW @4.0GHz	0.9mW @2.0GHz
Power Efficiency	0.69mW /GHz	3.87mW /GHz	3.06mW /GHz	1.63mW /GHz	0.45mW /GHz
Area(mm^2)	0.003	0.012	0.010	0.004	0.011

The following Table 2 shows the chips of DRAM in recent years, including process technology, operating frequency, power efficiency [13-17]. Early DRAM technology primarily used 55nm nodes [13], shifting to 40/28nm [14-17] after 2020. Frequency improved at higher speeds, alongside significant energy efficiency gains. By 2023, a new architecture (Digital-PLL) [17] was introduced, reducing power consumption in 40nm below 28nm levels. Seoul National University had a new design that also supported multi-mode duty cycles and increased area for optimized efficiency. Overall, DRAM research shifted focus to high-frequency, dynamic clock optimization and balancing area with energy consumption.

2.3 Flash

Flash memory is also widely used in electronic devices, such as smartphones, tablet computers. Flash has the advantages of good durability. The most significant difference between Flash, SRAM, and DRAM is that Flash is a non-volatile memory.

Modern Flash memory is mainly divided into NOR and NAND. NOR Flash memory adopts independent unit connection mode and supports byte addressing with fast reading speed but slow writing/erasing speed and high cost; NAND Flash memory adopts a series structure, with fast writing/erasing but slow read speed. Both of them adopt floating gate transistors and use hot electron injection (NOR) or FN tunneling principle (NAND) to realize data writing [18,19], but both must be erased before writing. During erasure, the floating gate charge is released through the tunneling effect induced by a strong electric field. NOR is more suitable for code storage, and NAND is ideal for large-capacity data storage. The structure is shown in Fig 3.

Table 3 demonstrates Flash memory's rapid evolution from 2021 to 2025 [20-24], marked by three key advancements.

From TLC (3bitscell) in ISSCC'21 [20], ISSCC'23 [22], ISSCC'24 [23] to QLC (4bitscell) in ISSCC'22 [21], ISSCC'25 [24], the capacity increase has been achieved through a low-voltage design that optimizes energy efficiency. In 2024, Micron Technology [23] designed a high throughput (>300MB/S) Flash with six planes and a low read time (32us). SK hynix [24] developed a large capacity (2TB) Flash with six planes and 321 stacked layers in 2025, indicating that indicating that multi-plane and large capacity have become two research hotspots for Flash.

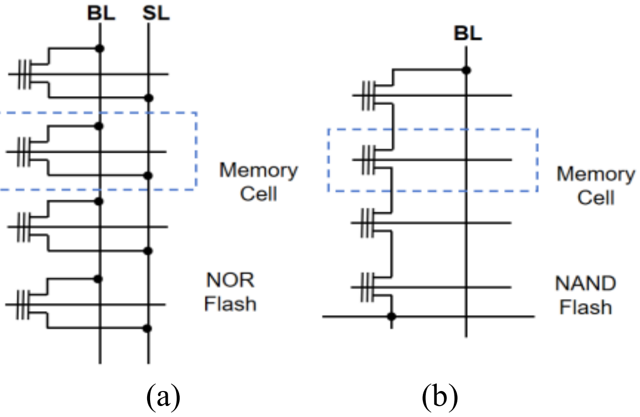


Fig. 3. (a) Array and bitcell of NOR Flash memory. (b) Array and bitcell of NAND Flash memory.

The growing AI and smartphone markets drive 3D Flash demand, but traditional stacking faces limitations like increased channel resistance. Emerging solutions include HFC architectures to address VG constraints [25] and a-BN-based space charge trap engineering, which improves erase speeds by 10 times [26]. Since 1987, NAND density has scaled over a million-fold with future progress likely focusing on logical/physical expansion, performance scaling, and AI computing applications [27].

3 Emerging Memory

3.1 RRAM

RRAM is also emerging nonvolatile memories, which are expected to replace the traditional Flash and DRAM.

Memristors are the core component of RRAM, featuring three states: high resistance state (HRS, logic 0), low resistance state (LRS, logic 1), and intermediate state with controllable resistance. The "SET" process switches HRS to LRS, while "RESET" reverses it. Applying a voltage that can toggle between states, and the resistance remains stable after power-off (nonvolatile).

Table 3. Flash Memory chips

	ISSCC’21 [20]	ISSCC’22 [21]	ISSCC’23 [22]	ISSCC’24 [23]	ISSCC’25 [24]
Technology	> 170 WL layers	176 layers	>300 layers	2YY Tiers	321 layers
Capacity	1 Tb	1 Tb	1 Tb	1 Tb	2 Tb
Bitscell/Planes	3/4	4/4	3/4	3/6	4/6
Page size	(16KB+ECC)/Page	N/A	16KB/Page	16KB/Page	16KB/Page

Die size	98 mm^2	67.55 mm^2	N/A	N/A	N/A
Density(Gb/mm^2)	10.4	N/A	> 20	> 20	28.2
Read time	50 us	90 us	34 us	32 us	80 us
Throughput	160 MB/s	40 MB/s	194 MB/s	> 300 MB/s	75 MB/s

Table 4. RRAM chips

	ISSCC’23 [28]	ISSCC’24 [29]	TED’24 [30]	ISSCC’24 [31]
Technology	40nm CMOS	40nm CMOS	16nm FinFET	12nm FinFET
Memory Type	N/A	N/A	1T10R 5layers	N/A
Size	20.25 mm^2(die)	20.25 mm^2(die)	0.104 um^2(cell)	0.0249 um^2(cell)
Throughput	11.1Mevents/s	12.8 GB/s	N/A	3.2 GB/s
VDD	0.9 V	0.8 ~ 1.1V	N/A	0.63 - 0.77V
Density	N/A	2.7 Mb/s	0.1 Gb/mm^2	256K x 144
Frequency	100 MHZ	80 ~ 210MHz	N/A	200MHz

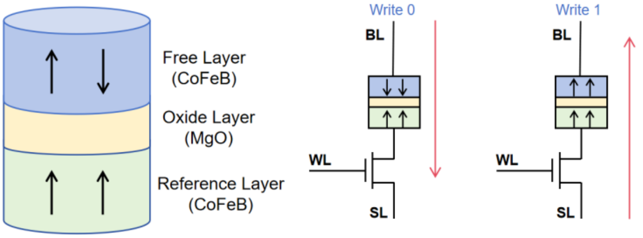
Table 4 shows RRAM developments from 2023-2025 [28-31], highlighting a research shift from energy efficiency to high-density integration and advanced processes. ISSCC'23 [28] and ISSCC'24 [29] designed RRAMs with low voltage (0.9V/0.8-1.1V) and high throughput (100MHz/80-210MHz), respectively, and they seemed to focus on low-power techniques like dynamic voltage scaling to improve energy efficiency and throughput. Subsequent studies (TED'24 [30], ISSCC'24 [31]) advanced high-density solutions including 1T10R 5 layer cells and compact designs, optimizing memory bandwidth and low-voltage operation.

However, RRAM still contends with conductivity instability caused by relaxation effects. Although high-temperature forming, triangular SET pulses, RP, and DV enhanced performance, they couldn't sufficiently address cost and programming time. The newer COPS approach mitigates relaxation while preserving fast programming. Emerging Bulk RRAM technology offers improved endurance and retention, supporting Few-shot On-Chip Learning [32], with additional applications in secure AI memory computing and chip encryption [33,34].

3.2 STT-MRAM

STT-MRAM has attracted much attention due to its advantages, such as its small size, high speed, and low power consumption.

The memory cell adopts a 1T-1T structure composed of a transistor and magnetic tunnel junction (MTJ). MTJ is composed of CoFeB ferromagnetic layer (free layer/reference layer) and MgO oxide layer and change its resistance through magnetization direction (parallel with low resistance/antiparallel with high resistance). During writing, WL activates the transistor and applies current to BL/SL to change the magnetization direction of the free layer. MTJ is stacked by the Back End process [35], which has high-density and is suitable for high performance storage scenarios. The structure is shown in Fig 4.



(a) (b)

Fig. 4. (a) Structure of MTJ. (b) Bitcell of STT-MRAM and write 0, 1 operation.

Table 5 presents the evolution of STT-MRAM technologies from Nature'22 to ISSCC'25 [36-40], demonstrating significant progress in memory density and access speeds. Nature'22 [36] designed a 22nm computing-in memory, but its area is large (2mm^2). Subsequent advancements at ISSCC'24 [37,38] achieved breakthroughs in both density and scalability, including ultra-compact 0.0187μm^2 memory cells with 16.5Mb/mm^2 density and improved embedded memory solutions. The most notable innovation emerged in ISSCC'25 [40] with the cross-point array architecture, which eliminates selector devices through self-selecting memory cells to achieve an industry-leading 0.001681μm^2 cell size.

Table 5. STT-MRAM chips

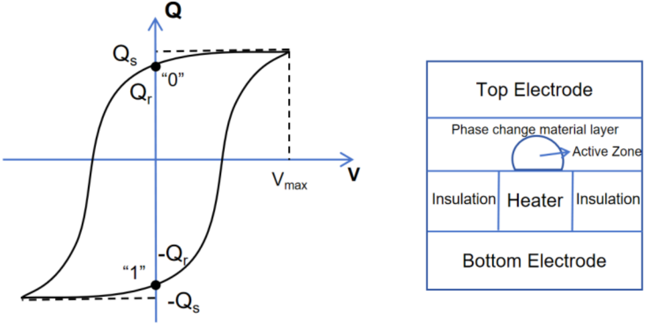
	Nature’22 [36]	ISSCC’23 [37]	ISSCC’24 [38]	ISSCC’24 [39]	ISSCC’25 [40]
Technology	22nm CMOS	16nm FinFET	22nm CMOS	16nm FinFET	20.5nm COMS
Cell Size	2 mm^2	0.033um^2	0.0456 um^2	0.0187um^2	0.001681 um^2
Structure	1T1MTJ	N/A	MTJ-OTP	N/A	1MTJ Cross-point
Array Size	N/A	N/A	N/A	N/A	4K-Row*2K-Col
Read/Write Width	N/A	6ns/N/A	4.2ns/N/A	7.5ns/20ns	2-5ns/15ns
Density	N/A	N/A	N/A	16.5Mb/mm^2	64Gbit

This architecture enables ultra-high-density storage with fast access times while maintaining the endurance and energy efficiency benefits of MTJ-based cells, making it particularly suitable for storage-class memory and neuromorphic computing applications. The progression from early MTJ concepts to advanced cross-point arrays highlights the semiconductor industry's pursuit of ultra-high-density memory solutions. This shift reflects innovations in cell miniaturization, selector-less architectures, and 3D integration to overcome traditional density barriers.

4 Other Emerging Memory

4.1 FeRAM

FeRAM replaces DRAM's conventional capacitors with ferroelectric capacitors, offering non-volatility, low power, high endurance, and radiation resistance. As shown in Figure 5 (a), it stores data by switching polarization states (Qr(0) or -Qr(1)) through applied voltage, retaining data stability at zero voltage. Writing "1" involves applying a negative voltage to transition from -Qs to -Qr(1).



(a) (b)

Fig. 5. (a) Spontaneous polarization characteristic curve of ferroelectric materials. (b) Structure of PCRAM.

Regarding the advantages of DRAM, the nonvolatile nature of FeRAM solves the shortcomings of DRAM power-off data loss well. Therefore, FeRAM is expected to be widely used in designing and manufacturing integrated circuits for mass production. Still, it is necessary to study and explore its materials and structures continuously.

4.2 PCRAM

The phase change memory (PCRAM) uses the crystalline amorphous characteristics of chalcogenide compounds such as Ge2Sb2Te5 to store data [61], which is written by heating melting or controlling crystallization, and use low-temperature reading to ensure accuracy. The structure of PCRAM is shown in Fig 5 (b). However, its high cost, high energy consumption and material stability limit its development. However, PCRAM still has market potential if it can make a breakthrough in material technology.

5 Conclusion

Memory architectures continue evolving to meet performance and power demands. Though constrained by power and cost, SRAM remains dominant for cache despite static power issues, and DRAM improves bandwidth through HBM. Flash maintains capacity advantages via vertical NAND stacking, but erasing and latency limitations spur demand for alternatives. Emerging nonvolatile memories are gaining traction: FeRAM succeeds in embedded systems with ultra-low power and endurance; RRAM leads for in-memory computing and neuromorphic chips due to energy efficiency and analog capabilities; STT-MRAM penetrates embedded and storage-class memory markets with speed and reliability; while PCRAM declines due to high-power needs and costs. Future memory hierarchies will become more collaborative, with SRAM for caching, DRAM for main memory, and RRAM/Flash for mass storage. Though RRAM and STT-MRAM face manufacturing and cost challenges, memory-computing integration will transform AI accelerator design. Nonvolatile, low-power RRAM and STT-MRAM will likely dominate the next-generation memory landscape, shifting from storage compute "separation" to "integration" architectures.

References

1. Kim S S, Yong S K, Kim W, et al.: Review of semiconductor flash memory devices for material and process issues. Advanced Materials, 35(43): 2200659(2023).
2. Salahuddin S, Ni K, Datta S: The era of hyper-scaling in electronics. Nature electronics, 2018, 1(8) pp. 442-450.
3. Tanaka, T. et al.: A 3nm Fin-FET 19.87-Mbit/mm2 2RW Pseudo Dual-Port 6T SRAM with High-R Wire Tracking and Sequential Access Aware Dynamic Power Reduction. IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2024, pp. 1-2.
4. Huang, M.-C. et al.: A 3.3GHz 1024X640 Multi-Bank Single-Port SRAM with Frequency Enhancing Techniques and 0.55V-1.35V Wide Voltage Range Operation in 3nm FinFET for HPC Applications. IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2024, pp. 1-2.
5. Haraguchi, M. et al.: A 3 nm-FinFET 4.3 GHz 21.1 Mb/mm2 Double-Pumping 1-Read and 1-Write Psuedo-2-Port SRAM With a Folded Bitline Multi-Bank Architecture. In IEEE Journal of Solid-State Circuits, 60(1), 197-204(2025).
6. Osada, Y. et al.: 3.7-GHz Multi-Bank High-Current Single-Port Cache SRAM With Leakage Saving Circuits in 3-nm FinFET for HPC Applications. In IEEE Journal of Solid-State Circuits, 60(3), 1113-1121(2025).
7. Fujiwara, H. et al.: 29.5 A 3nm 3.6GHz Dual-Port SRAM with Backend-RC Optimization and a Far-End Write-Assist Scheme. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2025, pp. 500-502.

8. Pal, A. et al.: Novel Logic & SRAM Interconnect Design for Advanced Complementary FET (CFET) Based Technology Nodes. IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2024, pp. 1-4.
9. Lu, Y.-C., M. -L. Wu and V. P. -H. Hu. Conflict-Free and Area-Efficient 4N4P CFET 8T SRAM with Double-Sided Signal Routing for Multibit Compute-in-Memory in AI Edge Devices. IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2024, pp. 1-4.
10. Lee, J. C. et al.: High bandwidth memory(HBM) with TSV technique. International SoC Design Conference (ISOCC), Jeju, Korea (South), 2016, pp. 181-182.
11. Cho, Y. et al.: Suppression of the Floating-Body Effect of Vertical-Cell DRAM With the Buried Body Engineering Method. In IEEE Transactions on Electron Devices, 65(8), 3237-3242(2018).
12. Kim, S. and H. -J. Yoo.: Opportunities and Challenges of DRAM-based Computing-in-Memory for AI Accelerator. 21st International SoC Design Conference (ISOCC), Sapporo, Japan, 2024, pp. 193-194.
13. Chae, J. et al.: A Quadrature Clock Corrector for DRAM Interfaces with a Duty-Cycle and Quadrature Phase Detector Based on a Relaxation Oscillator. IEEE Tran. VLSI, 27(4), 978-982(2019).
14. Shin, S., et al.: 22.6 A 0.8-to-2.3GHz Quadrature Error Corrector with Correctable Error Range of 101.6ps Using Minimum Total Delay Tracking and Asynchronous Calibration On-Off Scheme for DRAM Interface. ISSCC, 2020, pp. 340-341.
15. Yoon, H. et al.: A 3.2-12.8Gb/s Duty-Cycle Compensating Quadrature Error Corrector for DRAM Interfaces With Fast Locking and Low Power Characteristics. ESSCIRC, Sept 2021, pp. 463-466.
16. Park, H., et al.: A 1.3-4-GHz Quadrature-Phase Digital DLL Using Sequential Delay Control and Reconfigurable Delay Line. IEEE JSSC, 56(6), 1886-1896(2021).
17. Shin, Y., Y. Jo, J. Kim, et al.: 28.5 A 900μW, 1-4GHz Input-Jitter-Filtering Digital-PLL-Based 25%-Duty-Cycle Quadrature-Clock Generator for Ultra-Low-Power Clock Distribution in High-Speed DRAM Interfaces. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 408-410.
18. Guterman, D.C., I. H. Rimawi, R. D. Halvorson, et al.: Electrically alterable hot-electron injection floating gate MOS memory cell with series enhancement. International Electron Devices Meeting, Washington, DC, USA, 1978, pp. 340-343.
19. Maheshwari, V., S. Malipatil, N. Gupta, et al.: Modified WKB Approximation for Fowler-Nordheim Tunneling Phenomenon in Nano-Structure based Semiconductors. International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE), Vellore, India, 2020, pp. 1-5.
20. Higuchi, T., Kodama T, Kato K, et al.: 30.4 a 1Tb 3b/cell 3D-flash memory in a 170+ word-line-layer technology. IEEE International Solid-State Circuits Conference (ISSCC), 2021, pp. 428-430.
21. Cho, W. et al.: A 1-Tb, 4b/Cell, 176-Stacked-WL 3D-NAND Flash Memory with Improved Read Latency and a 14.8Gb/mm2 Density. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2022, pp. 134-135.
22. Kim, B. et al.: 28.2 A High-Performance 1Tb 3b/Cell 3D-NAND Flash with a 194MB/s Write Throughput on over 300 Layers. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 27-29.
23. Kawai, K. et al.: 13.7 A 1Tb Density 3b/Cell 3D-NAND Flash on a 2YY-Tier Technology with a 300MB/s Write Throughput. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 244-246.

24. Cho, W. et al.: A 321-Layer 2Tb 4b/cell 3D-NAND-Flash Memory with a 75MB/s Program Throughput. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2025, pp. 512-514.
25. Oda, M. et al.: Superior Scalability of Advanced Horizontal Channel Flash for Future Generations of 3D Flash Memory. IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2024, pp. 1-4.
26. Kang, D.H., J. J. Jeong, Y. K. Park, et al.: Spatial Charge Trap Engineering with Boron Nitride Barrier for 3D V-NAND Flash Memory. IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2024, pp. 1-4.
27. Goda, A.: NAND Flash Innovations and Future Scaling. IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2024, pp. 1-4.
28. Chang, M. et al.: A 73.53TOPS/W 14.74TOPS Heterogeneous RRAM In-Memory and SRAM Near-Memory SoC for Hybrid Frame and Event-Based Target Tracking. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 426-428.
29. Spetalnick, S.D. et al.: 30.1 A 40nm VLIW Edge Accelerator with 5MB of 0.256pJ/b RRAM and a Localization Solver for Bristle Robot Surveillance. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 482-484.
30. Huang, Y.-H. et al.: High-Density Embedded 3-D Stackable Via RRAM in 16-nm FinFET CMOS Logic Process. In IEEE Transactions on Electron Devices, 71(6), 3614-3619(2024).
31. Huang, Y.-C. et al.: 15.7 A 32Mb RRAM in a 12nm FinFet Technology with a 0.0249μm2 Bit-Cell, a 3.2GB/S Read Throughput, a 10KCycle Write Endurance and a 10-Year Retention at 105°C. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 288-290.
32. Kumar, A. et al.: Filament-Free Bulk RRAM with High Endurance and Long Retention for Neuromorphic Few-Shot Learning On-Chip. IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2024, pp. 1-4.
33. Chen, Y. et al.: First Demonstration of Unclonable Double Encryption 28nm RRAM-Based Compute-in-Memory Macro for Confidential AI. IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2024, pp. 1-4.
34. Sun, J. et al.: First Demonstration of Masked Polynomial Multiplier Based on 40nm 1TG1R RRAM Secure Chip for Lattice-Based Cryptography. IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2024, pp. 1-4.
35. Tomczak, Y. et al.: Influence of the Reference Layer Composition on the Back-End-of-Line Compatibility of Co/Ni-Based Perpendicular Magnetic Tunnel Junction Stacks. In IEEE Transactions on Magnetics, 52(7), 1-4.
36. S. Jung et al.: A crossbar array of magnetoresistive memory devices for in-memory computing. Nature, 601, 211-216(2022).
37. Lee, P.-H. et al.: 33.1 A 16nm 32Mb Embedded STT-MRAM with a 6ns Read-Access Time, a 1M-Cycle Write Endurance, 20-Year Retention at 150°C and MTJ-OTP Solutions for Magnetic Immunity. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 494-496.
38. Ogawa, T. et al.: 15.8 A 22nm 10.8Mb Embedded STT-MRAM Macro Achieving over 200MHz Random-Read Access and a 10.4MB/s Write Throughput with an In-Field Programmable 0.3Mb MTJ-OTP for High-End MCUs. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 290-292.

39. Lin, K.-F. et al.: 15.9 A 16nm 16Mb Embedded STT-MRAM with a 20ns Write Time, a 1012 Write Endurance and Integrated Margin-Expansion Schemes. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 292-294.
40. Hatsuda, K. et al.: 0.6 A 64Gb DDR4 STT-MRAM Using a Time-Controlled Discharge-Reading Scheme for a .001681\mu\mathrm{m}$ 1T-1MTJ Cross-Point Cell. IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2025, pp. 1-3.