Fpga Design and Optimization of Adaptive Filters

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Abstract. This paper discusses the role of adaptive digital filters in modern signal processing systems, highlighting their ability to dynamically adjust to varying signal environments. Two widely used algorithms, Least Mean Squares and Recursive Least Squares are analysed. LMS is computationally efficient and suitable for low-resource hardware but has limited convergence speed and sensitivity to signal correlation. RLS offers faster convergence and higher accuracy at the cost of increased computational complexity. With the increasing demand for real-time and low-power processing in fields such as wireless communication, biomedical devices, and industrial automation, Field Programmable Gate Arrays have become a preferred platform. Recent developments in FPGA-based adaptive filtering include optimization techniques such as sparse computation, pipeline parallelism, distributed arithmetic, and approximate computing. These strategies enhance performance while reducing power and hardware usage. Furthermore, methods like delayed LMS and diagonal loading RLS improve adaptability and stability in real-time systems. FPGA-optimized adaptive filters demonstrate high efficiency, robustness, making them ideal for high-throughput, low-latency, and dynamic applications.

Keywords: Adaptive Filters, FPGA, LMS, RLS, DSP.

1 Introduction

Adaptive filtering finds extensive usage in communications, control, and numerous other fields. Over the years, a variety of adaptive filtering algorithms have been put forward [1]. Unlike traditional fixed-coefficient filters, adaptive filters are capable of learning and evolving in real time, enabling them to track signal changes and mitigate disturbances effectively. This adaptability is particularly valuable in a wide range of practical applications, such as active power filtering, hearing aids, active noise control, biomedical signal processing, radar systems, and next-generation wireless communication technologies like 5G [2].

As signal environments become increasingly complex and time-varying, the demand for real-time, low-latency, and energy-efficient adaptive filtering solutions continues to grow. Modern applications in biomedical devices, industrial automation, and communication networks require filtering systems that not only provide high accuracy but also operate under stringent constraints on power consumption and

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computational resources. This has driven a surge of interest in hardware-based implementations of adaptive filters, particularly those leveraging Field Programmable Gate Arrays (FPGAs). FPGAs offer a reconfigurable and parallel computing architecture, ideal for accelerating adaptive filtering tasks with balanced flexibility and performance.

In this context, optimizing adaptive filtering algorithms for FPGA platforms has become a key area of research. These optimizations aim to overcome the limitations of conventional digital signal processors (DSPs) by improving throughput, reducing latency, and minimizing hardware resource usage-all without compromising filtering accuracy. With ongoing advancements in hardware and algorithmic design, adaptive filters will play a crucial role in next-generation signal processing systems.

2 Adaptive Filters

Adaptive Digital Filters are self-designing systems which are used in a wide variety of digital signal processing applications. Adaptive Digital Filters are usually applied in active power filters, bearing prognosis hearing aids, active noise control, cerebellum modeling, 5G technology. As modern communication networks, biomedical devices, and industrial automation increasingly rely on real-time adaptive filtering to enhance signals and suppress noise, thus the demand for optimizing these algorithms is also growing. Therefore, improving computational efficiency and adaptability has become a key research focus to ensure real-time performance while minimizing resource consumption. The general structure of a transversal adaptive filter or a Finite Impulse Response Filter is shown in Fig. 1.

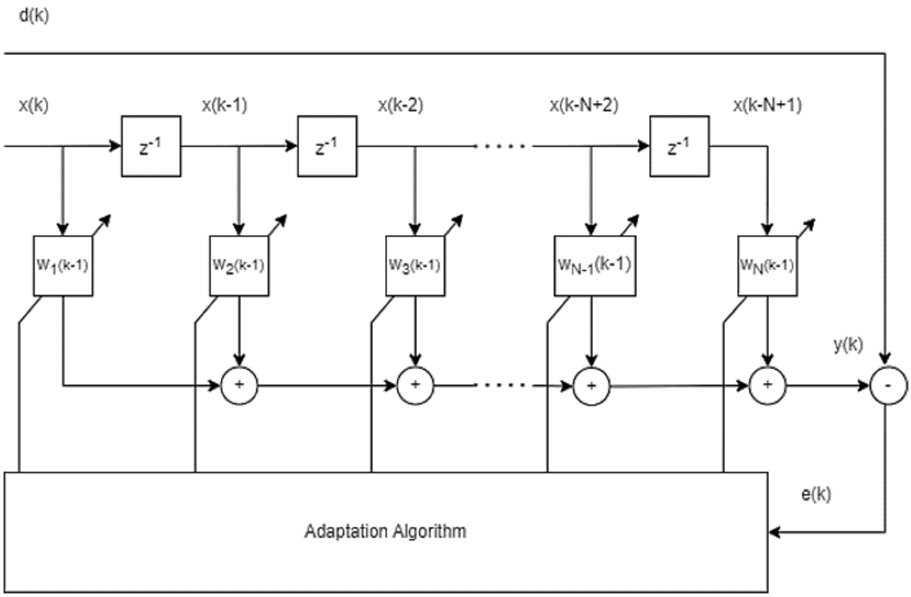

Fig. 1. Structure of Finite Impulse Response Filter (FIR-Filter) [3]

Adaptive filtering works by iteratively updating its filter coefficients. The goal is to reduce the difference between the output signal and a desired signal. Among various approaches, the Least Mean Squares (LMS) and Recursive Least Squares (RLS) algorithms are most frequently employed. LMS is simple to compute and requires minimal hardware resources, but it has slow convergence and is sensitive to correlated input data. RLS converges faster and provides higher filtering accuracy. However, it has high computational complexity, making it difficult to implement in real-time applications with limited computing resources.

2.1 LMS Algorithm

To optimize LMS on FPGA, various techniques have been explored to improve performance. These include sparse conjugate gradient methods, data reuse strategies, affine projection algorithms, and multi-innovation update methods. These methods aim to enhance convergence speed while reducing computational overhead. Additionally, fractional-order adaptive filtering has been introduced as an alternative to classical integer-order methods, demonstrating improvements in both convergence speed and parameter estimation accuracy.

Furthermore, improvements in Kalman filtering algorithms and AI-based adaptive filtering techniques have gained attention. Particularly in noise suppression tasks under complex signal environments, deep learning techniques have exhibited strong generalization capabilities and robustness, making them valuable for adaptive filtering applications [3].

2.2 RLS Algorithm

To reduce the computational complexity of RLS in FPGA implementations, a sparse RLS adaptive filtering algorithm with diagonal loading has been proposed. By optimizing the computational process, this method achieves a balance between lower computational complexity and high filtering performance. Traditional RLS algorithms, despite their high accuracy, have an $O(N^2)$ computational complexity, which limits their feasibility in real-time applications due to high resource consumption [4]. To address this issue, an optimized $O(N)$ complexity algorithm has been developed, bringing its performance closer to that of an oracle RLS, which assumes perfect prior knowledge of the system's sparsity.

This method employs a diagonal loading strategy, combined with reweighting methods and coordinate descent iterations to enhance computational efficiency. By reformulating the sparse system identification problem, the algorithm approximates nonlinear equations into a solvable linear system, significantly improving computational feasibility. The method utilizes the Dichotomous Coordinate Descent (DCD) iterative algorithm, an efficient approach for solving linear equations, effectively reducing FPGA resource consumption and enhancing real-time processing capabilities [5].

Experimental results indicate that both LMS and RLS achieve a threefold reduction in white noise, significantly improving signal quality, but some residual noise remains. RLS demonstrates superior noise suppression but is highly sensitive to parameter tuning, which, if not carefully managed, can lead to numerical instability. Moreover, the optimized sparse RLS algorithm reduces steady-state Mean Square Deviation (MSD) by 6 dB compared to conventional sparse RLS and by 14 dB compared to classical RLS. The result is shown in Fig. 2.

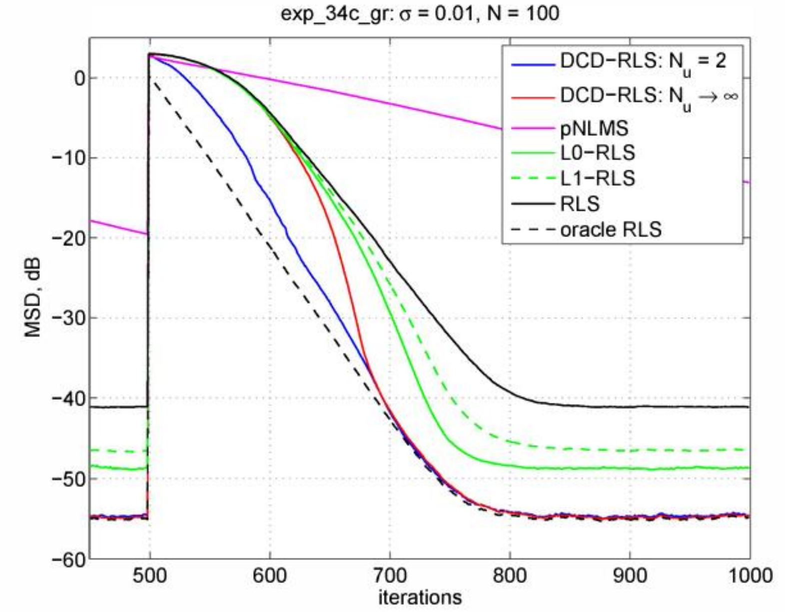

Fig. 2. MSD performance comparison of the adaptive algorithms, with parameters N=100, σ=0.01, and K=5 [4]

It also exhibits greater robustness to impulse response variations, making it suitable for real-time sparse system identification applications. In FPGA hardware design, optimizing filter order selection, memory management, parallel computing structures, and pipeline optimization is crucial. This ensures low-latency, high-throughput real-time filtering. Combining FPGA pipeline optimization, parallel computing, and storage management strategies, future FPGA-based adaptive filtering systems will achieve superior real-time signal processing performance in biomedical signal processing, wireless communications, and industrial automation.

3 FPGA-Based Adaptive Filtering Design

FPGA-based optimization of adaptive filtering algorithms has seen significant advancements in recent years, particularly in reducing hardware complexity and improving real-time adaptability. Researchers have focused on key methods such as LMS, RLS, and Distributed Arithmetic (DA) while integrating techniques like pipeline parallel computing, resource sharing, sparse computing, and Approximate Computing to enhance computational efficiency, reduce hardware complexity, and improve real-time adaptability. As a low-power, high-throughput reconfigurable computing platform, FPGA provides a strong hardware foundation for accelerating adaptive filtering computations in digital signal processing, wireless communications, radar monitoring, and biomedical signal analysis.

3.1 FPGA-Based LMS Filter Optimization

Implementing LMS filters on FPGA has been a primary research focus. Traditional DS based LMS filters suffer from serial computation constraints, making them unsuitable for high-throughput and low-latency real-time signal processing. To address this challenge, researchers have proposed FPGA-based LMS adaptive filtering architectures, adopting a modular design that divides the LMS processing into control, error computation, weight update, and storage modules. By incorporating dual-port RAM and pipeline optimizations, high-efficiency data read/write and computation are achieved. Experimental results show that FPGA-based LMS filters outperform DSP implementations in speed, interference resistance, and power efficiency. They reduce processing delay to 75 ns, significantly lower than the 406 ns delay observed in conventional DSP designs [6].

Additionally, this optimization leverages Xilinx DSP48 computational units for hardware acceleration. By utilizing resource sharing and pipeline optimizations, the DSP48 unit consumption for a 12-tap LMS filter is reduced from 36 to just 3, thereby leading to a 4.7-fold reduction in dynamic power consumption [7]. The operating frequency is increased from 285 MHz to 500 MHz, providing an effective solution for low-power embedded signal processing, intelligent speech recognition, and wireless communication systems.

3.2 FPGA-Based RLS Filter Optimization

Despite its computational simplicity and ease of hardware implementation, LMS suffers from slow convergence and sensitivity to correlated input signals, which limits its effectiveness in dynamic signal environments. In contrast, RLS, with its weighted least squares error minimization, offers superior convergence speed and filtering precision, making it more suitable for complex signal processing applications such as radar and biomedical imaging. However, RLS requires $O(N^2)$ computational complexity per update, consuming substantial FPGA resources, which limits its feasibility in high-throughput, low-power applications.

To overcome this limitation, researchers have introduced a sparse RLS algorithm with diagonal loading, optimizing the computational workflow to reduce complexity while maintaining high filtering performance. By adopting the DCD iterative method and reweighting techniques, the algorithm reduces computational complexity to $O(N)$ [5]. Experimental results indicate that the optimized sparse RLS algorithm achieves a 6 dB lower MSD compared to traditional sparse RLS and a 14 dB reduction compared to classical RLS, while also demonstrating superior robustness to impulse response variations. This makes it ideal for wireless communication channel estimation, image denoising, and biomedical signal analysis, where computational resources are critical.

3.3 FPGA-Based Distributed Arithmetic (DA) Adaptive Filtering

Beyond LMS and RLS, distributed arithmetic (DA)-based adaptive filtering has also emerged as a research focus in FPGA applications [8]. DA replaces traditional multiplications with look-up table (LUT) operations, providing advantages in efficient computation and low power consumption [9]. However, non-pipelined DA structures require an exponentially increasing number of LUTs as filter order increases, leading to excessive storage overhead and reduced implementation efficiency. To address this, researchers have proposed conjugate OBC-DA structures. These structures combine LUT decomposition, pipeline optimizations, and block processing techniques to reduce LUT requirements and enhance computational throughput. Experimental results indicate that these optimizations significantly improve performance in 5G communications, real-time radar imaging, and ultrasonic signal processing. Additionally, integrating Approximate Computing into DA-based optimization enables dynamic trade-offs between computational accuracy and hardware resource consumption, further expanding its applicability in low-power adaptive filtering systems.

3.4 FPGA-Based Delayed LMS (D-LMS) Optimization

To further enhance the efficiency of LMS adaptive filtering in FPGA implementations, a Delayed Least Mean Squares (D-LMS) adaptive filter has been developed. Traditional LMS filters, despite their simplicity, suffer from slow convergence and high computational complexity in large-scale implementations, making them less suitable for real-time, high-throughput applications [10]. D-LMS improves upon this by introducing a delay in the weight update process, effectively decoupling the error computation from weight updates. This delay allows for more efficient pipelining and parallelization, reducing hardware resource consumption while maintaining comparable filtering performance.

The FPGA-based implementation of D-LMS integrates several key optimizations. The Wallace Tree Multiplier is employed to accelerate the weight update calculations while minimizing the number of logic elements required. Unlike conventional multipliers, the Wallace Tree structure enables faster arithmetic operations through a hierarchical reduction process, reducing propagation delay and improving overall computational efficiency. Additionally, Block Carry Look-Ahead Adders replace conventional ripple-carry adders. This further enhances processing speed by reducing carry propagation delay during weight update calculations. To optimize memory utilization, register-based LUT structures are incorporated to store intermediate computation results, reducing redundant calculations and improving power efficiency.

Experimental results demonstrate that the FPGA-optimized D-LMS filter achieves lower power consumption and enhanced resource utilization compared to traditional LMS implementations. The design achieves significant reductions in hardware latency and computational complexity, making it particularly advantageous for low-power, real-time applications. The simulation results show that the modified D-LMS algorithm maintains the same execution speed as standard LMS implementations while achieving notable power savings. Furthermore, its robustness in dynamic signal environments makes it well-suited for applications such as biomedical signal processing, real-time image denoising, speech enhancement, and low-power wireless communications.

4 Conclusion

This paper has explored the implementation and optimization of adaptive digital filters on FPGA platforms, focusing on the widely used LMS and RLS algorithms. Through a range of strategies including sparse computation, pipeline parallelism, resource sharing, and approximate computing, it is possible to significantly reduce computational complexity while improving real-time adaptability and power efficiency. Experimental results confirm that FPGA-based adaptive filtering systems outperform traditional DSP-based approaches in terms of speed, flexibility, and energy consumption. Moreover, DCD iteration and diagonal loading methods effectively support high-performance filter deployment in constrained environments. Adaptive filtering plays a vital role in wireless communication, biomedical signal processing, and intelligent sensing. Further research into algorithm-hardware co-design, dynamic reconfiguration, and AI-assisted filtering will drive future advancements. FPGA-based adaptive filtering offers a scalable, low-power, and high-throughput solution for modern real-time signal processing demands.

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