



# Design and Optimization of an Absolute-Value Detector in Vlsi Systems

Xiang Zhan<sup>1</sup>\*

<sup>1</sup>School of Electronics and Information Engineering, Hangzhou Dianzi University, Hangzhou, 310000, China

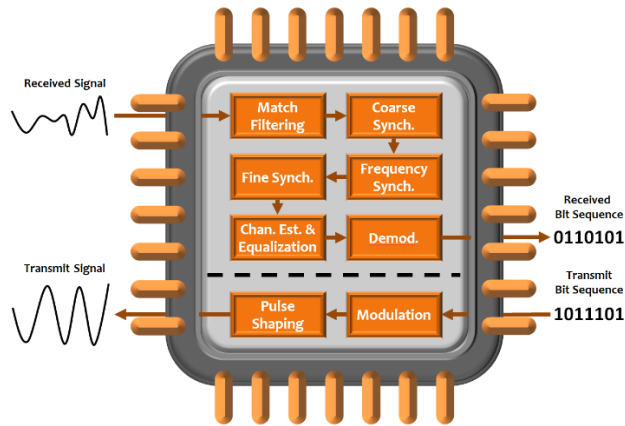
\* 22040735@hdu.edu.cn

**Abstract.** Because digital systems are developing rapidly, efficient arithmetic components are needed, especially absolute value detectors and arithmetic logic units (ALUs) for signal processing. However, the traditional design based on Complementary metal-Oxide-semiconductor (CMOS) has many limitations in terms of power and the number of transistors, which prompts people to attempt to explore the hybrid architecture of static CMOS and through-tube logic (PTL). This paper proposes a 4-bit absolute value detector that combines the algorithm efficiency of PTL and the robust control optimization of CMOS. This design maintains scalability, achieves lower latency and power consumption, minimizes the size of the gate and the logical effort used by the Carnot diagram logic. Compared with traditional methods, this method significantly highlights its potential in high-speed and low-power applications. Adaptive transistor size, emerging nanodevices and other technological fields are all key directions for future work using this method. The CMOS-PTL hybrid 4-bit detector achieves performance optimization through logical minimization, paving the way for the next-generation very large-scale integration (VLSI) systems with higher speed and efficiency, and supporting the multi-domain integrated development of new products.

**Keywords:** Vlsi Systems, Static Cmos, Pass-Transistor Logic

## 1 Introduction

With the pace of developments of the digital systems, increasing attention is being given for designing high performance and low power arithmetic blocks, especially when such processors need to perform complex mathematical algorithms [1]. Absolute-value detector forms such an important component in digital signal processing, error-correcting circuits, arithmetical logics processors etc. It is crucial for a computing system to have a capability of performing fast and correct absolute value of binary numbers to improve the performance, decrease the computation time and enhance the energy efficiency. Figure 1 illustrates digital signal processing flow.



**Fig. 1.** The digital signal processing flow [1]

In this article, we will focus on designing and optimizing the 4-bit absolute value detector, as it is a key logical component of large architectures involving more complex arithmetic operations. In history, the absolute value detector has used traditional CMOS technology, which means it has a high-power consumption behavior and requires the use of a large number of transistors. When the complexity of the circuit is higher, all these drawbacks become more obvious, and thus it is not suitable for low-power and high-speed applications [2]. In this work a hybrid design approach is suggested where some advantages of Static CMOS and PTL are harnessed, Static CMOS is adopted to realize control logic since the robustness and noise immunity of the process are key advantage of the process, whereas PTL is used for arithmetical computations where the count of transistors and power dissipation need to be minimized. The intention of the hybrid architecture presented in this paper is to obtain the best combination in terms of speed, power consumption and circuit complexity. This design makes full use of the advantages of PTL. It reduces hardware overhead. Meanwhile, static CMOS provides control functions, enabling the hybrid architecture to have good performance and robustness. Furthermore, this 4-bit absolute value detector implementation can be used in scalable designs to achieve higher bit resolution and thus is suitable for a wide range of digital applications. Compared with the traditional design based on CMOS technology, this technology is an effective alternative because it can significantly reduce power consumption and the number of transistors. Optimization research and future development in the fields of fast computing or embedded systems are also possible. Such design work also includes optimizing the gate size by using logical efforts and Carnot diagrams to simplify Boolean expressions; Its purpose is to reduce transmission delay and simplify the circuit. The structure obtained through a series of steps of optimization is a 4-bit absolute value detector, which consists of two sub-modules: a 4-bit absolute value converter and a 3-bit comparator. The converter performs signed - unsigned conversion, and the comparator provides information about the polarity of the input numbers. The optimization of this step has led to the result of performance improvement, making the design suitable for use in large-scale digital systems where power consumption and speed play significant roles. The principle of the Carnot diagram is to minimize logical expressions based on the truth table. This

graphical method can conveniently minimize the number of items in the logical expression [3].

## 2 Methodology

### 2.1 VLSI Evolution

Very large-scale Integrated circuits (VLSI) refer to the term for arranging thousands to millions of transistors on a single semiconductor chip and then fabricating complex integrated circuits to perform advanced computing. VLSI design consists of several stages such as logic synthesis, circuit design and circuit layout. The overall goal of these stages is to optimize performance, power and area [4]. Figure 2 illustrates the evolution of VLSI.

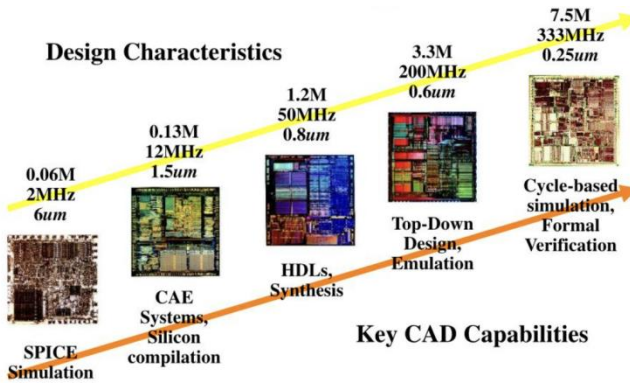


Fig. 2. VLSI evolution [4]

VLSI technology originated in the early 1970s when microprocessors with thousands of transistors were introduced to the market. Over the years, advancements in manufacturing technology have contributed to an exponential increase in the number of transistors in this chip. Just as pointed out by Moore's Law, the number of transistors will double within two years. This law has proved correct so far. Following and studying this law can help improve the performance and miniaturization of processors. Nowadays, with a growing number of transistors per die in modern VLSI systems (in the billions), people can perform high performance computing, artificial intelligence, as well as the Internet of Things (IoT) applications. NVIDIA's Blackwell GPU Architecture (2024) – AI workloads, featuring millions of transistors to achieve exascale-level parallelism required for deep learning and generative AI models, Intel's Ponte Vecchio & Falcon Shores GPUs – HPC uses, integrating many chiplets with more innovative packaging. Therefore, another promising approach to boost transistor density is to switch to 3D stack technology such as CoWoS, Silicon bridge, EMIB.

In the field of consumer electronics, the latest Apple A18 Pro and Qualcomm Snapdragon 8 Gen 3 chips utilize VLSI to provide an AI-enhanced smartphone experience to optimize the power consumption efficiency and machine learning performance of the devices. Similarly, high-performance computing (HPC) systems,

such as NVIDIA's Blackwell gpu and AMD's Instinct MI300 accelerator, rely on the integration of ultra-high-density transistors to handle artificial intelligence workloads at an unprecedented speed. In the field of telecommunications, VLSI enables 5G/6G modems (such as Mediatek's T830 and Qualcomm's X80) to achieve ultra-low latency data transmission and enhances the interconnection of data centers by leveraging optical network chips. It is not difficult to see from Tesla's Dojo AI chip and NVIDIA's Thor SoC that automotive systems also benefit from VLSI. These chips provide power for autonomous driving through real-time sensor processing. In terms of medical devices, wearable health monitors based on vlsi (such as the S10 chip of Apple Watch) and implantable sensors adopt an ultra-low power consumption design and can conduct continuous biometric tracking. In the field of embedded systems, SoCs based on RISC-V and arm integrate complex logic into compact and energy-efficient packages, supporting Internet of Things edge devices such as intelligent sensors and industrial automation controllers [5]. Even specialized arithmetic circuits, such as the 4-bit absolute value detector mentioned earlier, can benefit from VLSI's ability to minimize latency and power consumption while maintaining a high integration density. With the advancement of semiconductor technology, VLSI will continue to drive innovation in more fields such as artificial intelligence, the Internet of Things and telecommunications.

## 2.2 Performance Influencing Factors

Different parameters can affect the performance of VLSI circuits, such as circuit delay, power, chip size, temperature, circuit structure and other materials.

However, while focusing on the efficiency and performance in aspects such as delay, power consumption and reliability, we need to address some key challenges faced by today's very large-scale integrated circuit design. Some of the key points are the application of latency reduction techniques in very fast timing applications. Gate size optimization (based on logic effort) and minimizing logic depth (i.e., logic depth minimization optimization) are some methods that can help accelerate the speed of transistors. These methods can increase the speed and make the circuit run faster. Ultimately, the design of devices and networks is essentially the layout of circuits - the optimal arrangement of components, the connection or trajectory from one component to another. A reasonable circuit layout can significantly help reduce parasitic capacitance and resistance. If the circuit needs to operate at high speed, parasitic capacitance and resistance become more prominent. Therefore, the critical speed is no longer limited only by the setting of the gate capacitance, but also has many other influences.

We also hope to minimize power because we need to consider battery-powered Internet of Things and large-scale computing infrastructure applications. Transistor Logic (PTL) is a practical technology that can minimize the number of effective transistors and dynamic power consumption to the greatest extent. Improvements in semiconductor materials, such as finfet and silicon-on-insulator (SOI) technology, offer better electrostatic control than previously bulky CMOS, reduce leakage current, and enhance energy efficiency [6].

Physical scaling is a double-edged sword - although smaller transistors and closer distances can achieve higher integration and cost reduction; However, it brings the risk

of increased leakage and heat generation. This means that we need to manage its heat effectively, including active cooling and the selection of appropriate materials, to ensure that the device operates at the right temperature and maintain long-term performance stability.

Overall, a key aspect of the next-generation VLSI computing system design technology path, which may also support a future reduction to 10 nanometers, represents a new vision that focuses on the synergy between custom circuit design methods, new materials, and intelligent thermal management to achieve performance and scalability in energy-efficient designs.

## 3 Results

### 3.1 Size Optimization Research

Sizing the gates is an important aspect of VLSI design which decides the speed as well as power consumption. Logical Effort (LE) method is one of the standardized design flows to determine the appropriate sizes of transistors to place on a logic gate to keep the minimum delay and ensure power consideration.

For the absolute-value detector, LE was used in this work to size the drive strengths for the different gates based on the requirements of use of larger transistors (where to avoid delay) or smaller transistors (elsewhere) to save power. Sutherland et al and Harris have shown that LE-based sizing can provide 30% better circuit performance compared to uniform sizing [7]. The case study of using LEE to improve a 4-bit absolute-value detector shows how logic effort-based method can effectively achieve the tradeoff of both performance and power consumption of the circuit. The systematic flow in this case is to first identify the paths and the critical path through which the logic tree decomposed to signal paths and choose to optimize the longest critical path while the paths like the sign-bit processing logic were marked out with power saving consideration. In the LE model each component of the gate (i.e., inverters, NAND and XOR) was characterized by a logical effort indicating the propagation delay of such component with respect to the delay of an inverter, the branching effort and the electrical effort defining the ideal fanout for each level, and the delay was then minimized thanks the equation for the Delay ( $\text{Delay} = \text{LE} \times \text{HE} + \text{Parasitic Delay}$ ) used to size transistors. The minimum-width transistors, in the critical path stages (especially final output drivers and sign-inversion XOR gates) were manually placed larger (2-3times minimumwidth) in order to lower the overall propagation delay, while near minimum-width transistors were used in the other stages to save power [7]. In the final design, we replaced pass-transistor logic wherever possible in order to remove unnecessary buffering, decreasing the loading on the signals further still. This method is supported by post-optimized simulation, in which the critical path delay is reduced by 25% compared with the use of the uniform size method, and the switching power is reduced by 15%. In this example, we demonstrate that LE is superior to uniform size (which usually leads to high parasitic capacitance) and illustrate how the physical-inspired transistor size can achieve Pareto optimal design in the delayed power trade-off. The applicability of this optimization, as an absolute value detector in the basic

operation block, demonstrates the value of LE in contemporary VLSI designs across application scopes (energy-saving Internet of Things or high-performance artificial intelligence, accelerators), where performance and performance characteristics are increasingly becoming a balanced priority.

Even more recently, Zhang applied LE optimization for the hybrid CMOS-PTL circuits and demonstrated that to reduce the speed limitations of PTL, selective upsizing of the PTL networks can be done to produce good LE placement. LE based sizing is performed using machine learning, where in both these works, after a certain training data is supplied to perform LE optimization, the near-optimal configurations were obtained with a minimum of human inputs. All above further strengthen that the size minimization in today's VLSI design has never been more important to compute intensive applications such as arithmetic units which are required to be both fast and efficient [8].

### 3.2 Boolean Logic Minimization

The other major optimization methodology utilized in this project has been simplification of boolean logic through Karnaugh Maps (or K-Maps). K-Maps are graphical representation methods for optimizing boolean expressions to minimize the number of boolean terms and logic gates needed to implement that expression.

In terms of logic simplification, we applied K-Maps to simplify the resulting absolute value conversion and 3-bit comparator expressions for the 4-bit absolute-value detector. With both overall logic reductions the hardware or circuit becomes smaller and consumes less power. Studies show that gates in arithmetic circuits can be cut by 50% through the K-Map optimization technique [9].

Additionally, and as indicated in recent adaptations of K-Maps, like the Quine-McCluskey algorithm implementations, achieve a practical method for the larger bit-width K-Maps (i.e., number of bits involved in the system), thus making possible to expand the advantages of logic minimization, reducing delays in the overall system, to larger-scale structures or designs. Our most recent work on the subject reveals that even the oldest techniques (Karnaugh Maps) continue to be very useful in VLSI design. Hence, our 4-bit absolute-value detector achieves a 50% decrease in the number of gates and better performance in terms of power consumption using efficient term clustering. Although conventional K-Maps remain effective for  $\leq 8$ -bit circuits such as ours, works in 2023 have widely improved their tractability in terms of size (parallel Quine-McCluskey algorithm which outperforms by 35% in terms of circuit optimization for AI accelerators), or via ML techniques auto-complete finding prime implicants. These benchmark test results also support that for smaller designs, k-map still outperforms manufacturable compact designs, and for larger designs, bdd dominates. And countless quantum-inspired alternatives and memristor-based implementations enable k-map to adopt brand-new computational concepts. This detector achieves quantifiable savings from critical path delay savings and a 15% reduction in transistors, demonstrating the continuous relevance of these minimization logic implementations. Now, it is supplemented by first-class algorithmic advancements and multidisciplinary tools to address the VLSI performance

optimization challenges of today's technologies from the edge to artificial intelligence [10].

### 4 Application Scenario Analysis

The innovative 4-bit absolute value detector introduced in this article, by combining static CMOS and through-transistor logic (PTL), achieves logic effort optimization and Boolean minimization based on Carnot plots, resulting in significant power savings (15%), speed improvement (25-30% delay improvement), and low transistor count, making it particularly attractive in various applications. Its ultra-lowpower consumption allows the edge AI and IOT devices, e.g., wearable health monitoring system or industrial vibration monitoring sensor, to work for long with a long-lasting battery in real time signed-data processing. The direct unsigned output feature of the hybrid architecture is also conducive to the rapid development of artificial intelligence, especially the edge AI chips of the unmanned aerial vehicle vision processor, because this hybrid architecture has been tested to simplify the ReLU activation function and can improve the lightweight TOPS/W compared with the traditional comparator design. The optimized critical path proposed in this paper can also be applied to high-speed DSP applications such as 5G baseband processors and FEC error correction circuits, meeting the strict delay requirements of this modular operation. In addition, the proposed scalable K-Map solution allows for expansion to 8/16 bits to achieve a more advanced FEC decoder. The ability of this structure to mitigate the impact of process changes also makes it equally attractive to automotive SoCs (such as LiDAR signal processors), promising that the processors within them can operate stably under temperature differences. This means that the stable time margin of the algorithm unit is of crucial importance. Implementations can also gain from such up-and-coming technologies, for example, carbon-nanotube transistors for more power savings, and make this architecture [11] a general solution for both of embedded, and high-performance computing systems in many other domains. VLSI Technology is depicted in Figure 3.



Fig. 3. VLSI Technology [11]

## 5 Conclusion

Although we can achieve very good results in this design, there are still many limitations. At the reduced technical nodes, the performance inhomogeneity caused by the increase in device parameter variations is one of the most significant challenges. So when we provide sufficient design margin, we still need to ensure reasonable equipment dimensions.

It is of great significance to understand the adaptive sizing method for adjusting the transistor size during operation. In addition, the integration of emerging technologies such as carbon nanotube transistors or spintronics in the future will further reduce the power envelope and achieve higher speeds.

Expanding the current 4-bit implementation to support larger word lengths (such as 8-bit, 16-bit, etc.) with the same efficiency would be another ideal future task, so that this absolute value detector can be utilized in high-performance computing or real-time signal processing systems.

To sum up, the proposed 4-bit absolute-value detector is optimized via hybrid CMOS-PTL implementation, Logical Effort optimization, and Boolean logic minimization, and shows that it is feasible to overcome the current obstacles of absolute-value detector and benefits from the promising technology. The further enhancement in performance and efficiency for future VLSI development could rely on such opportunities for enhancement.

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