Investigation of Stt-Mram Technology based on Finfet Process

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Abstract. This paper summarises the research progress and challenges of STT-MRAM technology based on FinFET technology, exploring its core advantages in high-density, low-power, and non-volatile storage. The advantage of FinFET mainly lies in its 3D gate. This paper summarizes relevant papers in recent years, focusing on bit cell structure optimization, adaptive write circuit design, and peripheral circuit coordination. It reveals how FinFET and spintronic device integration breaks traditional storage tech bottlenecks. This paper also compares it with other new storage techs, STT-MRAM's high read speed and low power consumption are highlighted. It also foresees the collaborative innovation of FinFET and STT-MRAM for next-gen non-volatile memory, providing a theoretical framework for future research.

Keywords: Emerging Non-Volatile Memoey, Finfet, Stt-Mram, Low-Power Design

1 Introduction

Integrated circuit technology is essential in the information age, driving digital transformation across sectors. The semiconductor memory market is projected to exceed $234.2 billion by 2025, highlighting its importance.

The current semiconductor storage technology is mainly dominated by two systems: volatile and non-volatile. The former primarily includes dynamic random access memory (DRAM) and static random access memory (SRAM), while the latter has flash memory technology as its core. But with the development of nanotechnology, they face physical bottlenecks: the static power consumption of volatile memory surges, while the multi-transistor structure of SRAM limits storage density; Although Flash dominates the non-volatile market, its write latency and durability are reduced, and its compatibility with CMOS is poor below 28nm [1].

The emerging non-volatile memory STT-MRAM is considered a strong candidate for the next generation of memory. It uses a magnetic tunnel junction controlled by spin-polarised current for high-speed, non-volatile storage. Its three-dimensional heterogeneous integration with FinFET supports high-density arrays, achieving

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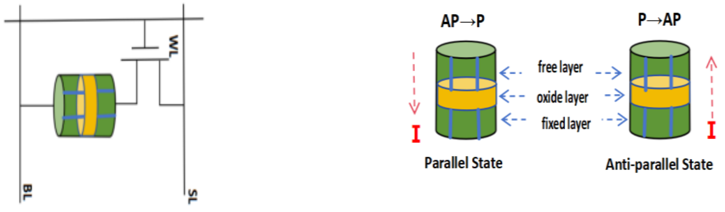
densities similar to DRAM and read speeds similar to SRAM. It solves the incompatibility of flash in CMOS below 28nm and has the advantages of non-volatile, high durability, and low power consumption [2].

FinFET can further promote the development of STT-MRAM towards low power consumption and high performance. Compared to traditional planar MOSFETs, FinFET breaks through the two-dimensional size limitation through its three-dimensional structure. The core innovation lies in vertically constructing the channel region into a fin-like structure and enhancing the electrostatic control of the channel through a three-layer encapsulation of the gate. At the same process node, there is a significant increase in driving current compared to planar MOSFETs, while reducing leakage current by two orders of magnitude [3]. In terms of process compatibility, the manufacturing process of FinFET shares the majority of common steps with conventional CMOS processes, which is crucial for embedded memory integration. When STT-MRAM is combined with FinFET technology, hybrid integration of storage cells and logic circuits can be achieved at 1x nm nodes.

2 PRELIMINARIES

2.1 Introduction to STT-MTJ

As shown in Fig. 1 (a) and (b), The Spin Transfer Torque Magnetic Tunnel Junction (STT-MTJ), a non-volatile memory cell, comprises a free layer, oxide layer, and fixed layer.



a *b*

Fig. 1. STT-MTJ Introduction (a) 1T1M Unit [4]; (b) Parallel and anti-parallel states of MTJ switching [4]

Spin-polarized current controls the free layer's magnetization: The current flowing from the free layer to the fixed layer is written as “0”; On the contrary, written as “1”. Compared to traditional memory, STT-MTJ has advantages such as being non-volatile, high read speed, low power consumption, and high endurance, making it particularly suitable for low power magnetoresistance memory (MRAM) design [4].

The 0 and 1 switching mechanism of STT-MTJ is achieved through the synergistic effect of current intensity and thermal noise, and its core relies on the coupling regulation of critical current (Ic0) and dynamic switching delay (τ). The formula for critical current Ic0 is as follows (1) :

$$\mathrm{I}_{\mathrm{c0}} = \alpha \frac{\gamma e}{\mu_{\mathrm{B}} g}\left(\mu_0 \mathrm{M}_s\right) \mathrm{H}_k V_{sl} \tag{1}$$

STT-MRAM's magnetic flipping depends on parameters (Hk, μ0, Ms) and current thresholds: Using the Sun model (I>Ic0) for 3ns high energy consumption writing in the high current region; low-current zone (I<0.8Ic0) relies on thermal fluctuations (Néel-Brown model), causing slow switching and error risks. In the intermediate region between 0.8Ic0 and Ic0, the STT effect competes with thermal noise, and the physical mechanism is complex and lacks a clear mathematical model, requiring statistical methods to simulate random switching behaviour [5].

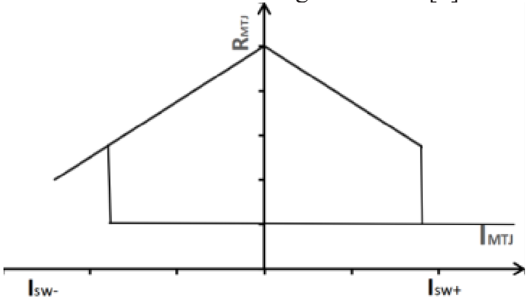


Fig. 2. R (I) curve of the magnetic tunnel junction [4]

As shown in Fig. 2 , the I-R curve of STT-MTJ exhibits a nonlinear relationship of "roof shape". The resistance depends on the magnetic alignment between the free layer and the fixed layer, exhibiting bistable hysteresis. In the AP state, the resistance decreases monotonically with increasing voltage. Slowly changing at low voltage, accelerating the decrease near the critical threshold, and approaching a stable state outside the threshold range to enter the P state.

2.2 Introduction to FinFET

FinFET is a promising technology that is likely to replace traditional SG MOSFETs in future generations. It mitigates short-channel effects and boosts scalability [6]. In addition, compared to traditional MOSFETs, it reduces subthresholds and gate tunnelling leakage currents.

Compared with planar MOSFET, FinFET achieves three breakthroughs through its 3D fin structure: (1) adopting a vertical channel design controlled by the surrounding gate to suppress short channel effects and leakage; (2) The Z-axis conductive channel expansion ($W = 2Hfin + TSI$) optimizes the two-dimensional area while increasing the driving current and integration density; (3) Miniature process enables low voltage operation, balancing performance and energy efficiency. As shown in Fig. 3, the vertically stacked channels enhance gate potential regulation, providing a core solution for advanced node devices [7].

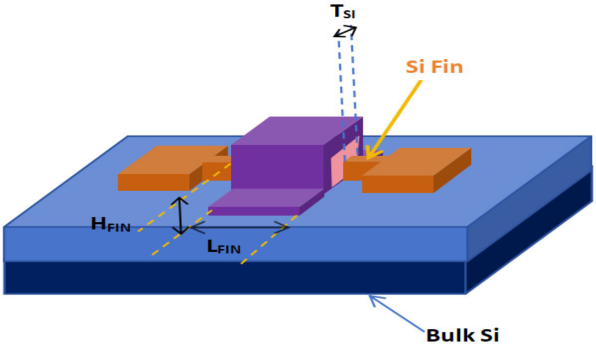


Fig. 3. FinFET structure [7]

3 STT-MRAM and FinFET team up

3.1 STT-MRAM bit cell-based FinFET technology

FinFET technology provides a high-density, low-power solution for new non-volatile memory through the synergistic optimization of three-dimensional structure, electrical performance, and process.

This paper summarizes the STT-MRAM bit cells based on FinFET reported in recent years.

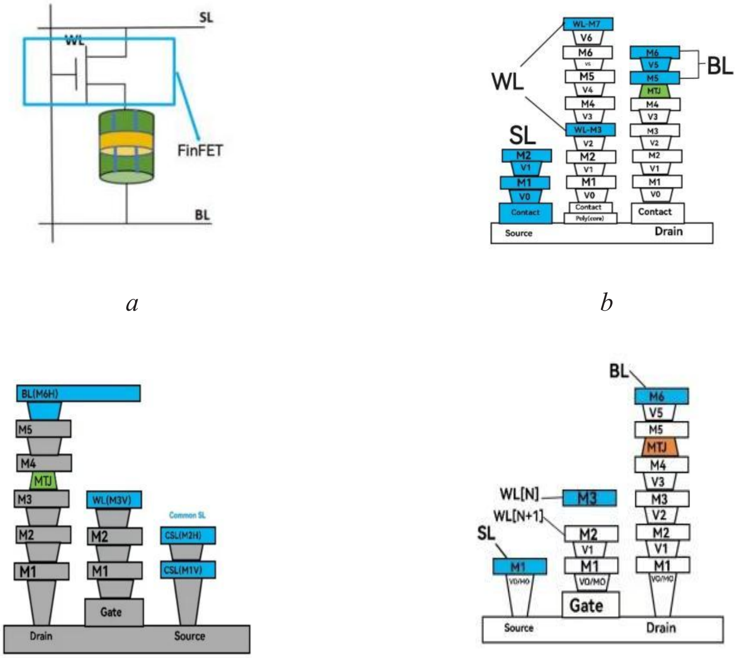
Intel launched a 0.0486 μm² STT-MRAM bit cell with the 1T1MTJ structure at International Solid-State Circuits Conference (ISSCC) in 2019 [8], consisting of two polycrystalline silicon word lines (WL), one metal 4 bit line (BL), and one metal 1 source line (SL), The multiple connections between polycrystalline silicon WL and M5 optimize the switching speed and signal efficiency of WL, Optimizing the metal layer and balancing the reading margin of precision resistor arrays to achieve high-density and reliable integration.

As shown in Fig. 4 (a) and (b), Taiwan Semiconductor Manufacturing Company (TSMC) reported on a 0.033μm² STT-MRAM bit cell at the 2020 International Electron Devices Meeting (IEDM) conference; MTJ is located between M4 and M5, with BL vertically connecting M5, M6, and SL composed of M1 and M2; WL uses parallel wiring of M3 and M7 to shorten the path; Four unit shared CSL4 reduces parasitic resistance, BL current sensing reduces capacitance, and achieves high-density, low-power reliable storage [9].

As shown in Fig. 4 (c), TSMC proposed a 0.033μm²STT-MRAM bit cell with 1T1MTJ at the 2023 ISSCC conference, with WL wiring on M3, BL wiring on M6, and common SL wiring on M2 [10].

As shown in Fig. 4 (d), TSMC showcased a 0.0187μm² STT-MRAM bit cell at the 2024 ISSCC conference, integrating MTJ between M4 and M5; The word line adopts M2 and M3 alternating wiring optimized by DTCO to achieve balanced line width and spacing, Four shared source lines (CSL4) minimize parasitic resistance and capacitance, while downstream process integration improves array density and signal transmission efficiency [11].

To boost STT-MRAM write current, wider access transistors are needed, increasing cell area. FinFETs enhance density: For the same W requirements, compared to traditional CMOS, the two-dimensional area of FinFET devices can be reduced by increasing Hfin [7].



a *b*

c *d*

Fig. 4. Bit cell structure (a) FinFET in 1T1M cell [4]; (b) Cross section of the unit structure in IEDM'20 [9]; (c) Cross section of Unit Structure in ISSCC'23 [10]; (d)Cross section of Unit Structure in ISSCC'24 [11]

3.2 Read and Write Circuit of STT-MRAM Based on FinFET

STT-MRAM read and write circuits using FinFET technology achieve higher performance and integration. Intel designed a sense amplifier that utilizes offset cancellation and double sensing margin structure at the 2019 ISSCC conference, achieving 4ns read at 0.9V and 8ns read at 0.6V, improving reliability [8]. TSMC proposed an STT-MRAM design based on 16 nm FinFET technology at the 2020 IEDM conference, which minimizes reference current drift as much as possible, achieves read interference resistance, eliminates induction offset through independent IO adjustment, and improves the read efficiency of high-performance MCU by 12% [9]. In 2022, Peking University proposed a reading circuit based on 16nm FinFET technology at the International Symposium on Circuits and Systems(ISCAS), which was enhanced by TSMC's Continuous recording enhanced voltage sensitive amplifier(CRE-VSA) proposed in ISSCC 2018 [12]; It added a reset acceleration transistor to eliminate residual voltage on sensitive nodes and achieved high-speed operation and low-power advantages through the superior electrostatic control of FinFET [13]. Samsung Electronics showcased a 128Mb MRAM based on 14nm FinFET technology at the 2023 IEEE Symposia on VLSI Technology and Circuits (VLSI) conference, which features cell-based read offset compensation (CROC) to reduce IO read margin variations and parasitic resistance effects; The optimization of NFET size in the SA branch minimizes process variations to the greatest extent possible, achieving a 31% reduction in DNL while improving read reliability [14]. TSMC released a 16Mb STT-MRAM based on 16nm FinFET technology at ISSCC 2024, which has a dual reference function and reduces read errors by 26%, SA clamp transistor optimizes BL voltage to achieve lower power and higher linearity [11].

Renesas Electronics Corporation introduced self-terminating slope Write (STW-SVP and SCP) with adaptive voltage and current slope adjustment [10] at IEDM in 2021; Optimizing energy consumption in two stages: the first stage uses low voltage to simultaneously write 4N-bits, and the second stage uses a charge pump to correct the remaining bits. This solution reduces total write energy consumption by 72% and write time by 50% [15]. In 2022, Peking University proposed a write termination circuit based on 16nm FinFET technology at ISCAS that can save 82.3% of power consumption at a Low write error rate, support high-density 1T1M cells, and is suitable for high-capacity cache applications [13]. Samsung Electronics introduced the merged source follower write driver (MSWD) and enhanced transmission gate column multiplexer (BPCM) at the 2023 VLSI conference [14]. These devices avoid write interference and double write throughput through optimized energy efficiency.TSMC proposed an STT-MRAM writing circuit in ISSCC in 2024 that can improve writing efficiency, doubling the writing speed, greatly improving durability, dynamically correcting errors to reduce bit error rates, and improving accuracy and array yield [11].

3.3 World Line driver

TSMC proposed an STT-MRAM design based on 16 nm FinFET technology that utilized dual M3 and M7 word-line layers at the 2020 IEDM, reducing stabilization time by 40% and area by 15% compared to the 22nm process through optimized interconnect design [9]. Renesas Electronics Corporation presented Self-termination write schemes with slope write voltage and current pulse of a 20Mb embedded STT-MRAM test chip in a 16nm FinFET logic process. It reduced spin-flip time variation, boosting write stability; WL drivers adopt VCC direct power (no charge pump), shrinking area while maintaining efficiency [15]. The innovation proposed by Samsung Electronics at the 2023 VLSI Conference is that the Gated WL Driver (GWLD) supports high write voltage through thick oxide transistors, switches to VDD during reading to ensure reliability, uses Vddio power supply and VGWL bias control, bypasses N1 NFET to achieve fast stability [14]. TSMC launched an RRAM-based word line driver at ISSCC in 2024, reducing BL to ground resistance by 50%. It minimizes WL position dependence, supports extended BL routing to improve area efficiency, and enhances the reliability and layout optimization of high-density Resistive Random Access Memory (RRAM) [16].

3.4 STT-MRAM chips based on FinFET technology

As shown in Table 1 , FinFET-based STT-MRAM chips show rapid density advancements. Bit cell area shrank 61.5% from 0.0486μm²[8] to 0.0187μm² [11], It reflects the significant improvement of storage density due to technology iteration. The bit cells proposed by IEDM in 2020 and 2021, as well as ISSCC in 2023, remain stable at 0.033 μm² [9][10][15], In 2023, VLSI will use 14nm technology to achieve 0.024 μm²[17], demonstrating the synergistic effect of process miniaturization and design optimization. The overall trend indicates that STT-MRAM based on FinFET is evolving towards a high-density and low-cost direction. The reading time is generally controlled within 10ns. IEDM proposed in 2020 that STT-MRAM maintain a read time of <9 ns within the temperature range of -40 ℃ to 125 ℃, emphasizing temperature stability design [9]; The read time of STT-MRAM proposed by ISSCC in 2023 is 6 ns at 0.68V [10], while the read time of STT-MRAM proposed by ISSCC in 2024 is 7.5 ns at [11]. The small performance fluctuations indicate that process improvements have not significantly affected speed. In 2023 [14], VLSI proposed that MRAM operate at 80MHz (≈ 12.5 ns) at 0.64V and 150 ℃, with a focus on high-temperature environmental adaptability. Overall, STT-MRAM based on FinFET achieves multi-scenario compatibility through process optimization and circuit design while maintaining low latency. STT-MRAM technology has achieved a significant reduction in bit cell area and improvement in read performance through methods such as process miniaturization and 3D structural innovation.

Table 1. Summary of STT-MRAM chips based on FinFET presented at international conferences from 2019 to 2024

	ISSCC'19 [8]	IEDM'20 [9]	IEDM'21 [15]	ISSCC'23 [10]	VLSI'23 [14]	VLSI'23 [17]	ISSCC'24 [11]
Technology	22FFL FinFET	16nm FinFET	16nm FinFET	N16 MRAM	14nm FinFET	14nm FinFET	16nm FinFET
Bit cell area	0.0486μm²	0.033μm²	0.033μm²	0.033μm²	N/A	0.024μm²	0.0187μm²
Read access time	4ns@0.9v, 8ns@0.6v	< 9nS@ -40C ~ 125C	N/A	6ns(0.68v)	80MHz @0.64V, 150°C	N/A	7.5ns
Write pulse width	N/A	50ns	STW-SVP/SCP	N/A	N/A	N/A	20ns

Table 2. Summary of data on STT-MRAM chip based on FinFET and its comparison with DRAM, SRAM, ReRAM, and flash at international conferences from 2023 to 2025

	ISSCC’24 [18]	ISSCC’25 [19]	ISSCC’23 [20]	ISSCC’23 [21]	ISSCC’23 [10]	ISSCC’24 [16]	ISSCC’24 [11]
Technology	3D NAND with280 stacked WL layer	3nm	22nm	130nm CMOS	N16	12nm FinFET	16nm FinFET
Memory type	N/A	SRAM	SRAM	FeRAM	MRAM	RRAM	STT-MRAM
Bit cell area	4 bit	0.052μm^2	N/A	N/A	0.033μm^2	0.0249μm^2	0.0187 μm^2
velocity	Write:41 Mb/s tR:85μs	N/A	N/A	Read: 5ns Write: 7ns	Read:6ns @0.68v	Read：200MHz@0.6v	Read: 7.5ns Write: 20ns
Macro capacity	1Tb	20Kb	832Kb	9Mb	32Mb	N/A	16Mb
Vdd	N/A	N/A	0.6v-0.8v	N/A	0.72V-0.88V	0.63v-0.77v	N/A

4 Comparative Analysis of Different Memories Based on FinFET Technology

Table 2 summarizes the different memories based on FinFET technology reported at ISSCC conferences in recent years. Table 2 compares memory technologies: the STT-MRAM based on 16nm FinFET technology storage unit area reported in [11] is 0.0187 μm^2, which is about 25% lower than the 0.0249 μm^2 of 12nm RRAM in ISSCC in 2024 [16]. However, 3D NAND Flash achieves a macro capacity of 1Tb [18] through stacking technology, far exceeding the 16Mb of STT-MRAM [11] and the 20Kb of Static Random-Access Memory (SRAM) [19], highlighting STT-MRAM's need for 3D integration to scale capacity. For working voltage, In 2024 ISSCC [11], STT-MRAM's range is unspecified, but MRAM in [10] operates at 0.72V-0.88V, and RRAM in [16] at 0.63V-0.7V. SRAM in [20] requires 0.6V-0.8V with higher static power. In speed, STT-MRAM's 20ns write delay [11] surpasses NAND Flash's 85μs [18] but lags behind SRAM's 7ns [21]. Magnetoresistive Random Access Memory (MRAM) in [16] shows high-speed potential with 200MHz reads @0.6V, while STT-MRAM's non-volatility suits low-power Internet of Things (IoT). The Ferroelectric RAM (FeRAM) reported in [10] can achieve 5ns of reading, but the CMOS technology used is still 130nm, which will cause significant area overhead. The non-volatile characteristics of STT-MRAM can significantly reduce standby power consumption, but further optimization of dynamic power consumption is needed.

5 Conclusion

This paper systematically analyzes FinFET devices and STT-MRAM, with a focus on the STT-MRAM architecture based on FinFET (including storage units, read and write circuits, WL driver circuits, and peripheral circuits). By summarizing the research on STT-MRAM technology based on FinFET in recent years, it was found that the design based on FinFET has made breakthroughs in the write speed, density, and power efficiency of non-volatile memory. Moreover, the performance of STT-MRAM is superior to other alternatives, with excellent reading speed, endurance and retention time. FinFET and STT-MRAM achieve the optimal balance between density, and power efficiency through multi-level collaborative optimization. This integration overcomes traditional memory bottlenecks and drives the widespread adoption and industrial progress of next-generation general-purpose storage technologies.

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