Design of Absolutely-Value Detector and Optimize its Delay and Power Consumption

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Abstract. With the development of electronic products, integrated circuits have become the focus of research in related fields. In this paper, a 4-bit absolute value detector with low delay and low energy consumption is designed, which is composed of adder, MUX and comparator. When the circuit is working, MUX is used to screen the positive and negative of the 4-bit input signal, the adder converts the negative number into the corresponding absolute value, and transmits the absolute value signal to the comparator through MUX and compares it with the given threshold, and finally outputs the result. Based on the linear delay model, the logical effort and parasitic delay of the circuit are calculated, and the MUX part of the circuit is composed by a transmission gate. Through some calculation and optimization, the optimal delay of the detector is 44.76. By adding a certain delay, the delay reaches 67.14 of the 1.5x optimal delay, and the power consumption of the circuit reaches the optimal 9.72C. Finally, this paper realizes a relatively simple 4-bit absolute value detection circuit with fewer components, which greatly improves the performance of the circuit. This research also has some reference value for the design of related circuits.

Keywords: Integrated Circuit, Energy Consumption, Optimal Delay, Transmission Gate, Logic Effort

1 Introduction

In recent years, with the rapid development of electronics industry technology, there is a large demand for high-performance integrated circuits with high reliability, low delay and low power consumption in related industries. Delay and power consumption are important considerations for designers when designing integrated circuits. A 4-bit absolute value detector, which has lower energy consumption, and a small delay is designed in this paper [1]. The main function of this detector is to derive the absolute value of the input 4-bit two's complement, compare it with a threshold value, and figure out the size relationship between the two [2].

This paper chooses to use half adder and transmission gate to compose the converter part of the circuit, finding the magnitude (absolute value) of the neural signal (x[n]), the input is a two's complementary, which size is important. Therefore, if detector

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wants to get the absolute value of the negative input, it needs to take the inverse of the two's complementary and add 1. And then transfer the input signal to the comparator to compare the size with the threshold value. Y is the output result after comparison. When the sign is greater than the threshold value, y is equal to1. In the other case, y is equal to 0. Then, after completing the preliminary design to realize related functions, this paper optimizes the circuit by Boolean method and Karnaugh diagram, obtains the final circuit, and finds out the critical path of the circuit. The optimal delay of the critical path is obtained by optimizing the calculation. The optimal energy consumption is calculated by python, and the optimal energy consumption with 1.5 times the optimal delay is obtained. The experiments results satisfy the theoretical calculations. The design of this paper helps to optimize energy consumption and reduce delay, which is useful to related industries [3, 4].

2 Logic Gate Design

2.1 Basic Theory and Implement

In order to achieve the design goal, the function of the detector needs to include obtaining the absolute value of the input complement signal, comparing the absolute value and the threshold value, and the final output result. So, the circuit consists of 3 parts: an adder, a compound gate (include a transmission gat), and a comparator [5]. Since the 4-bit input signal is in the form of a two's complement and MSB is a sign bit, the decimal number input ranges from -7 to 7. The conversion of number systems is shown in Table 1.

Table 1. Conversion between two's complement and decimal number

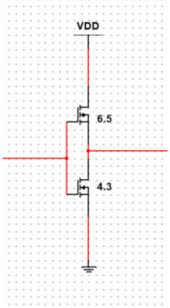
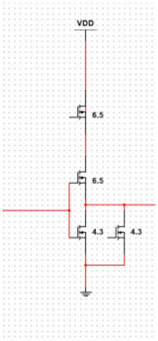
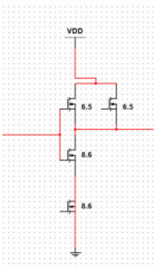
A3	A2	A1	A0	Decimal number
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	1	-1
1	0	1	0	-2
1	0	1	1	-3
1	1	0	0	-4
1	1	0	1	-5
1	1	1	0	-6
1	1	1	1	-7

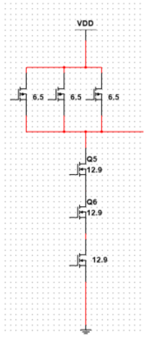
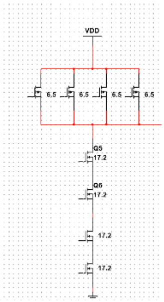
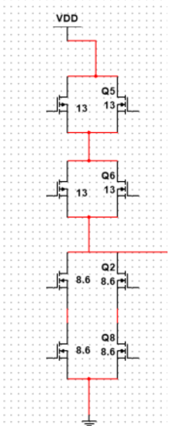
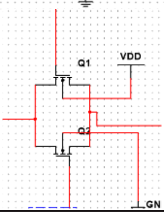
It can be seen from the truth table that the MSB A3 indicates whether the value of the source code of the input two's complement signal is positive or negative.

When A3=0, the input two's complement is equal to its absolute value, which can be directly passed by MUX (transmission gate); When A3=1, the source code of the input two's complement is negative, and its absolute value can be obtained by adder before it can be filtered through MUX (transmission gate). And T2T1T0 is the threshold value. If the input of comparator S2S1S0 is larger than the threshold value T2T1T0, the output is 1. Otherwise, the output is 0 [4].

The parameters of the logic gates required in the design are shown in Table 2.

Table 2. The parameters of the logic gates

Logic gate	Structure (pictures credits: Original)	input	output
Unit inverter		a	a'
2 input NOR gate		a, b	(a+b)'
2 input NAND gate		a, b	(ab)'

3 input NAND gate		a, b, c	(abc)’
4 input NAND gate		a, b, c, d	(abcd)’
2 input XOR gate		a,b	a’b+ab’
Transmission gate		I, O, c, c’	I/O

2.2 Complete Circuit Design

Design of Converter and Adder. First of all, the author designs the converter part, because the inverse code of the negative input signal needs to be taken, so this part is composed of NOT gate.

For how to design the adder, author have made the following considerations for the choice of equipment. Since we only need to use the curry of the previous level and the input of the current level as the input signal of the adder in the absolute value calculation, author choose to use the half adder instead of the full adder. The schematic diagram of the adder is shown in Figure 1.

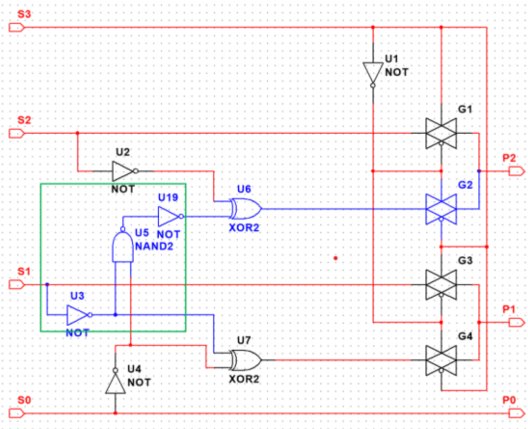


Fig. 1. The schematic diagram of the adder (Picture credit:Original)

When, S3=1, the truth table can be shown in Table 3.

Table 3. The truth table of absolute values of two 's complement

S2	S1	S0	P2	P1	P0
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	0	1

Using the truth table, readers can find that the first term S0 of a four-bit two's complement is always equal to the first term P0 of the absolute value of this two's complement.

A half adder consists of an XOR gate and an AND gate, author choose using the truth table in Table 4 to prove it.

Table 4. Truth table of the half adder

S1	S0	output	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$\text{Output} = S1'S0 + S1S0' \quad (1)$$

XOR gate can be used to describe it.

$$\text{Carry} = S1 * S0 \quad (2)$$

AND gate can be used to describe it.

Each bit needs to pass through the inverter, because of

$$(S1 * S0)' = S1' + S2' \quad (3)$$

the AND gate of the half adder can be replaced with a NOR gate.

The relationship between S0' and Set and Carry is presented in Table 5.

Table 5. The relationship between S0' and Set and Carry

S0’	Set	carry
0	1	0
1	1	1

Through truth table, the carry after S0’ plus 1 is equal to S0', so a NOR gate can be further omitted in the carry calculation of S0 level.

After all, function expressing P2, P1, P0 can be shown,

$$P2 = S2' \oplus (S1 + S0)' \quad (4)$$

$$P1 = S1' \oplus S0' \quad (5)$$

$$P0 = S0 \quad (6)$$

Design of Compound Gate. As can be seen from the introduction, S3 as the symbol bit of the input two’s complement determines the positive and negative of the true form, so author decide to add a transmission gate into the circuit, so that S3 can control the opening or closing of the transmission gate, so as to distinguish the positive and negative of the true form and ensure the accuracy of the absolute value of the output. Since a transmission gate cannot be a single level on the main path, author decided to add a buffer and a transmission gate to form a compound gate by looking at the previous essay. In this way, we need to calculate the logical effort and parasitic delay of the compound gate by drawing the CMOS structure of the two parts.

Circuit Design of Comparator. Firstly, this paper considers a comparator based on serial logic. The reason this article explores a comparator based on serial logic is that if you use this logic, you can get the result directly by comparing the MSB of the current input to the MSB of the threshold, without comparing the rest of the bits. If the input is P2P1P0, the threshold is T2T1T0. The effect diagram of the serial comparator is shown as follows in Figure 2..

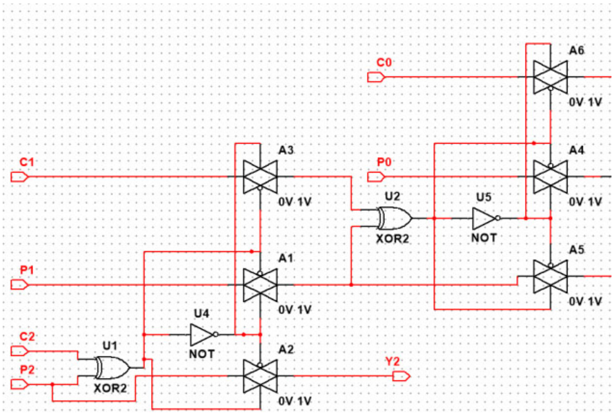


Fig. 2. The schematic diagram of serial comparator (Picture credit:Original)

The following is the truth table for comparing the MSB P2 of the input with the MSB T2 of the threshold in this logic. The operation logic of the first level of the comparator is presented in Table 6.

Table 6. The excitation table of the first level

P2	T2	operation
0	0	Skip
0	1	Y=0
1	0	Y=1
1	1	Skip

From this excitation table, you can see the basic logic of the serial comparator. If the skip state is triggered after a comparison, the comparator automatically compares the next bit of the input P1 to the next bit of the threshold T1. The comparison results between P1 and T1 is shown in the Table 7.

Table 7. The excitation table of the second level

P1	T1	operation
0	0	Skip
0	1	Y=0
1	0	Y=1
1	1	Skip

It can be seen from the data table that when the states of P and C are different, the P_i value is Y, so this paper uses XOR gate to control the transmission gate to achieve this screening. When $P_i=C_i, P_i \oplus C_i=0$, and when $P_i \neq C_i, P_i \oplus C_i=1$.

Based on this serial logic, author design an integrated circuit using transmission gate, so that in some cases, the circuit does not need to be fully used to get the final output answer.In this design, six transmission gates are used. The different states of the transfer gate are presented in Table 8, 9, 10, 11.

Table 8. Case1 P2=C2

P	C	$Output_{XOR}$	A1	A2	A3
0	0	0	Open	Close	Open
1	1	0	Open	Close	Open

Table 9. Case2 P2≠C2

P	C	$Output_{XOR}$	A1	A2	A3
0	1	1	Close	Open	Close
1	0	1	Close	Open	Close

Table 10. Case3 P1=P2

P	C	$Output_{XOR}$	A4	A5	A6
0	0	0	Open	Close	Open
1	1	0	Open	Close	Open

Table 11. Case4 P1≠P2

P	C	$Output_{XOR}$	A4	A5	A6
0	1	1	Close	Open	Close
1	0	1	Close	Open	Close

The other reason six transmission gates are used in this paper, is that the output of XOR gate will always be zero if there is only one input, so author choose to use six transmission gates in order to avoid affecting the circuit performance.

For instance, if we don't use A3, C1 will connect directly with XOR gate. When A1 closes, the output of XOR gate is equal to 0 and the performance of circuit will be affected. The schematic diagram of the first-level comparator is shown in Figure 3.

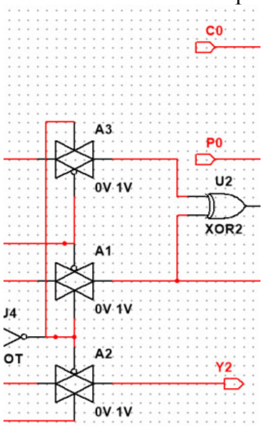


Fig. 3. The schematic diagram of the first-level comparator (Picture credit:Original)

Because of the use of transmission gates, the circuit need to be designed three outputs to achieve its goal. Compare P0 with C0 to get Y0, compare P1 with C1 to get Y1, compare P2 with C2 to get Y2.Due to the use of transmission gates, only one of Y0, Y1, Y2 will have an output, so none logic gates can be used in the last stage, because the suspended input impedance in the CMOS circuit is very high, which may form an intermediate level (non-0 and non-1) due to charge accumulation, resulting in logic errors or device damage. So, users need to detect these three outputs at the same time, and the final output Y is equal to the only valid output level of these three outputs Y0, Y1 or Y2. The positions of Y2, Y1 and Y0 are as shown in the following figure 4.

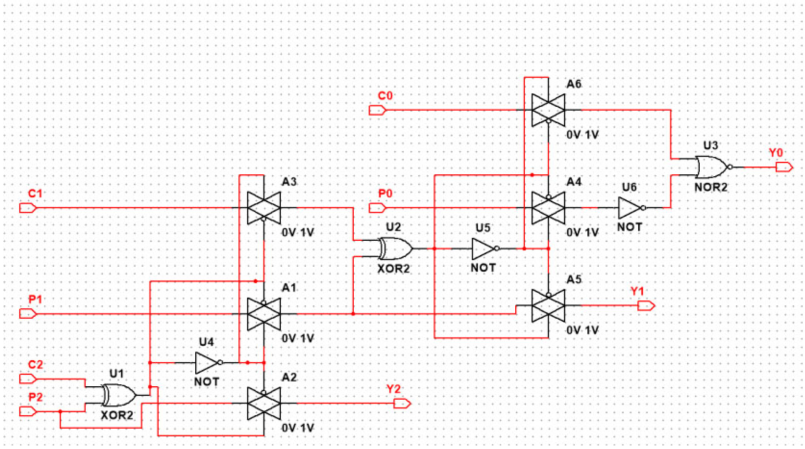


Fig. 4. The position of the output signal in the circuit (Picture credit: Original)

For example, if P2P1P0=100, the excitation table can be shown in Table 12.

Table 12. Excitation table of the serial comparator

P2	P1	P0	C2	C1	C0	Y2	Y1	Y0
1	0	0	0	0	0	1	/	/
1	0	0	0	0	1	1	/	/
1	0	0	0	1	0	1	/	/
1	0	0	0	1	1	1	/	/
1	0	0	1	0	0	/	/	0
1	0	0	1	0	1	/	/	0
1	0	0	1	1	0	/	0	/
1	0	0	1	1	1	/	0	/

This paper also designs a parallel logic comparator, in which the idea is slightly different from the serial logic, the idea is to compare each level of input and threshold size at the same time, through the truth table simplification, author get the simplest logical relation expression. The comparator is designed to compare the output of the magnitude calculator with a fixed 3-bit threshold value. If the magnitude goes beyond the threshold, it will produce a high level (1); otherwise, it will produce a low level (0). The comparator utilizes a cascade of NOR and NAND gates to perform bit-by-bit comparison, ensuring that the output is high only if all comparative evaluations confirm the magnitude is greater than or equal to the threshold. The truth table can be shown in Table 13.

Table 13. The truth table of output

P2	P1	P0	T2	T1	T0	Y
0	0	1	0	0	0	1
0	1	0	0	0	0	1
0	1	0	0	0	1	1
0	1	1	0	0	0	1
0	1	1	0	0	1	1
0	1	1	0	1	0	1
1	0	0	0	0	0	1
1	0	0	0	0	1	1
1	0	0	0	1	0	1
1	0	0	0	1	1	1
1	0	1	0	0	0	1
1	0	1	0	0	1	1
1	0	1	0	1	0	1
1	0	1	0	1	1	1
1	0	1	1	0	0	1
1	1	0	0	0	0	1
1	1	0	0	0	1	1
1	1	0	0	1	0	1
1	1	0	0	1	1	1
1	1	0	1	0	0	1
1	1	0	1	0	1	1
1	1	1	0	0	0	1
1	1	1	0	0	1	1
1	1	1	0	1	0	1
1	1	1	0	1	1	1
1	1	1	1	0	0	1
1	1	1	1	0	1	1
1	1	1	1	1	0	1

By using Karnaugh map to simplify, author calculate the expressing function of output,

$Y = \{(P2T2')'[(P2'T2)'P1T1']'[(P2'T2)'(P1'T1)'P0T0']'\}'$(7)

And the schematic diagram of parallel comparator is shown in Figure 5.

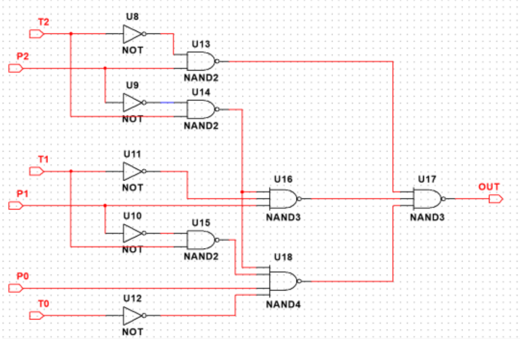


Fig. 5. The schematic diagram of parallel comparator (Picture credit:Original)

By comparing the two methods, this paper finds that the advantage of serial logic is that in some cases, the circuit will not be fully started, thus reducing the power consumption of the circuit in some cases. However, the use of transmission gate increases the difficulty of determining the main path, and because the transmission gate cannot be used as a single level of the main path for analysis. A compound gate with a buffer increases the optimal delay of the circuit by significantly increasing the logical effort and parasitic delay [6]. The advantage of parallel logic is that by simplifying the truth table, author gets the simplest logical expression, so as to optimize the path, and can use the least components, thus reducing the delay of the circuit. The disadvantage is that each level is involved in comparison with the threshold value, thus increasing the power consumption of the circuit. After comprehensive consideration, author finally chose parallel logic as our idea for designing the comparator.

2.3 Optimal and Comparison

Author splits the half adder so that we can calculate the output using the XOR gate alone or the carry using the AND gate. At the same time, author finds some special relations according to the truth table and further simplify the circuit.

Author chose XOR gate and transmission gate to form compound gate before, but after calculation, we found that the values of logic effort and parasitic delay were not very accurate, so author chose to add buffer and transmission gate to form compound gate, which reduced parasitic delay and optimized the optimal circuit delay.

Because this paper finally decided to use parallel logic as the idea of designing the comparator, the simplest logical expression is simplified by the truth table, and the delay of the circuit is further reduced by replacing the logic gate.

Through the above optimization, the simplest form of the circuit can be got, and by simplifying the COMS structure of the compound gate, we get the optimal logical effort and parasitic delay, which further reduces the optimal delay of our circuit.

3 Critical Path Analysis

3.1 Determine the Critical Path

The critical path of the complete circuit is shown in the following figure 6.

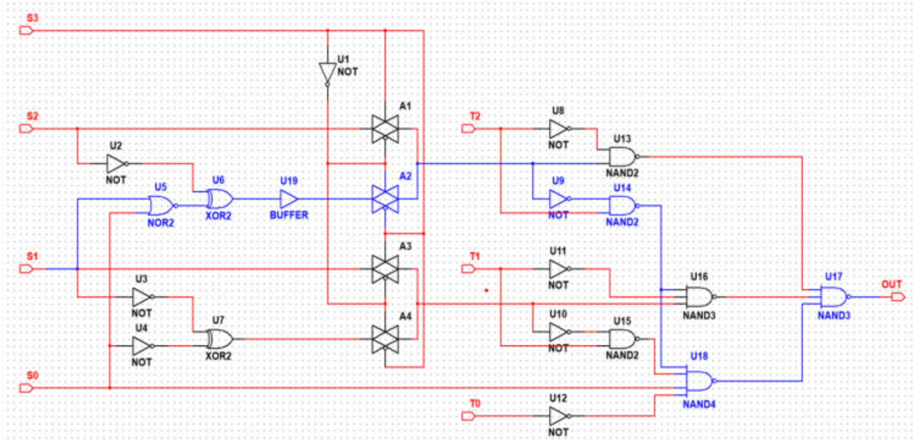


Fig. 6. The schematic diagram of critical path (Picture credit:Original)

When calculating the critical path, the line with the longest continuous operating time on the line is considered to be the critical path [7]. In this paper, the line with the longest delay is selected as the critical path. The critical path is indicated by the blue line in the diagram.

3.2 Calculate the Parameters(g&p)

The definition of logic effort is to reflect the inherent delay of a logic gate due to its structure (such as the number of inputs), regardless of the load. It is a method used to analyze and optimize logic gate delay in digital circuit design.

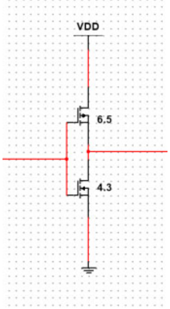
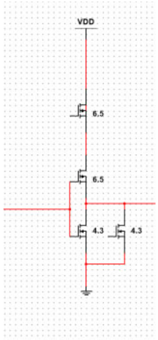
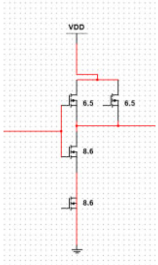
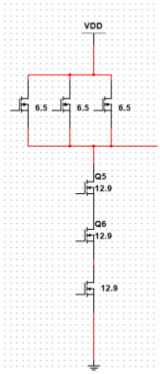
$$g = \frac{C_{ingate}}{C_{inv}} \tag{8}$$

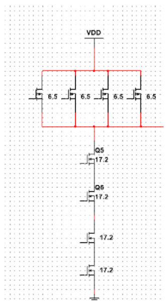
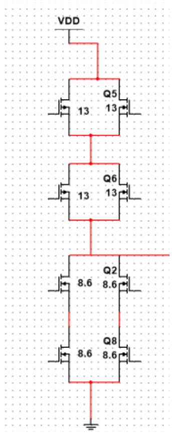
Parasitic delay is defined as a fixed delay caused by capacitors inside the gate, such as transistor diffusion capacitors, independent of the load.

$$p = \frac{C_{par,gate}}{C_{inv}} \tag{9}$$

Assume gamma is equal to 1 for delay modeling, and the unit-sized inverter is Wp = 650nm (pmos), Wn = 430nm (nmos), Lp = Ln = 100nm (drawn L). The calculation of the logical effort and parasitic delay for each logic gate using static CMOS logic. The parameters of the logic gate on the critical path are shown as in Table 14.

Table 14. The parameters of the logic gate on the critical path

Logic gate	Structure (Pictures credits:Original)	Logic effort	Parasitic effort
Unit inverter		1	1
2 input NOR gate		1.6	2
2 input NAND gate		1.4	2
3 input NAND gate		1.8	3

4 input NAND gate		2.19	4
2 input XOR gate		4	4

Because this paper chooses to use a composite gate, for this atypical logic gate, its g and p need to be calculated separately. To calculate the parameters of the compound gate, it is necessary to draw the CMOS structure diagram of the compound gate first. The structure of the compound gate is shown fellow in Figure 7.

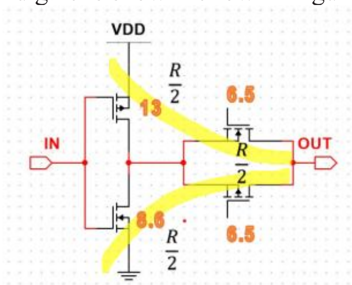


Fig. 7. The structure diagram of compound gate (Picture credit: Original)

Because of $\frac{W_P}{W_N}$=$\frac{6.5}{4.3}$,to simplify, assuming that, penalty effect is equal to $\frac{4.3}{6.5}$,we can get the size in the graph.

When pulling up,

$$\text{gup} = \frac{13+8.6}{6.5+4.3} = 2 \quad (10)$$

$$\text{Pup} = \text{Pout} + \text{Pin} = \frac{13+8.6+6.5+6.5}{13+8.6} + \frac{6.5+6.5}{4.3+6.5} \approx 2.8 \quad (11)$$

When pulling down,

$$\text{Gdn} = 1.92 < 2, \text{Pdn} = 2.76 < 2.8 \quad (12)$$

So that, $g_{compound}$ is 2 and $P_{compound}$ is 2.8.

3.3 Calculate the Optimal Delay

This paper calculates the optimal delay based on the critical path. Firstly, the parameters of each level are shown as in Table 15.

Table 15. The parameters of each level

Stage	1	2	3	4	5	6	7	8
Size	1	a	b	c	d	e	f	g
g	1.6	4	1	2	1	1.4	2.19	1.8
p	2	4	1	2.8	1	2	4	3
h	a	b/a	c/b	2d/c	e/d	2f/e	g/f	32/g
b	1	1	1	2	1	2	1	1

Path logic effort g is equal to the product of each gate's logic effort g.

$$G = \Pi gi = 70.64064 \quad (13)$$

Path electrical effort H is defined as the ratio of the output capacitance that the path must drive to the input capacitance that the path presents.

$$H = \frac{C_{out}}{C_{in}} = 32 \quad (14)$$

Path branching effort **B** is the product of branching efforts **b** between different levels.

$$B = \Pi bi = 4 \quad (15)$$

Path effort F is a combination of path logical effort, electrical effort, and branch effort.

$$F = GHB \quad (16)$$

The product of efforts at all levels is F, independent of the size of the door. If a path has the optimal number of levels N and each level bears the same effort, then the optimal single level effort is defined as f.

N=8,

f^*=3.12,

$$\text{Delay} = \sum gh + \sum P = N * f^* + \sum P = 44.76 \quad (17)$$

So, the critical path's optimal delay is 44.76.

4 Delay and Energy Consumption Optimization

4.1 The Influence of Sizing of 1.5x Delay

Using this formula, we find that we can adjust the sizing of the component to affect h, which in turn affects delay.

$$\text{Delay} = gh + p, \quad (18)$$

$$h = \frac{size_{n+1}}{size_n} \quad (19)$$

The parameters of each stage are shown in Table 16.

Table 16. Adjust the parameters of each level after sizing

Stage	1	2	3	4	5	6	7	8
g	1.6	4	1	2	1	1.4	2.19	1.8
p	2	4	1	2.8	1	2	4	3
b	1	1	1	2	1	2	1	1
Size	1	1	1	1	1	1	1	L
h	1	1	1	2	1	2	L	$\frac{32}{L}$
C_L	2	2	2	2	2	2	1+L	32+L

$\text{Delay} = \sum gh + \sum p = 34.2 + 2.19L + 57.6/L = 67.14(20)$

According to the above formula, as the latency is the 1.5 x optimal latency, the size of L is 13.02C or 2.02C. The value of 1.5x optimal delay is equal to 67.14.

4.2 The Influence of Sizing of Energy Consumption

Parameters related to computing power consumption at each level is shown Table 17.

Table 17. The parameters of power consumption of each level

Stage	1	2	3	4	5	6	7	8
C_L	2	2	2	2	2	2	1+L	32+L
$\alpha_{0\to1}$	0.1875	0.2500	0.2500	0.0625	0.2500	0.1875	0.1210	0.2490

$$E_{avg} = C_L * Vdd^2 * \alpha_{0\to1} \tag{21}$$

When L=13.02, E_{avg}=17.7714, when L=2.02, E_{avg}=11.2114.

Through the above calculation, the average power consumption after adjusting sizing is less than the power consumption of 28.34761 in the optimal delay, and when L is equal to 13.02, the power consumption decreases by about 37.20% [8]. When L equals 2.02, the power consumption decreases by about 60.45%.

4.3 The Influence of Vdd of 1.5x Delay

As it seen below,where k=$\frac{C}{\beta}$

$$\text{Delay} = \frac{Q}{I_D} = \frac{C*Vdd}{\beta*(Vdd-V_{th})^2} = \frac{k*Vdd}{(Vdd-0.2)^2}, \tag{22}$$

The purpose of this paper is to adjust the Vdd to make the delay 1.5 times the optimal delay.

So,

$$1.5 * \frac{k*Vdd}{(Vdd-0.2)^2} = \frac{k*1}{(1-0.2)^2} \tag{23}$$

Where Vdd=0.774, when delay is equal to the 1.5x optimal delay.

4.4 The Influence of Vdd of Energy Consumption

Because, $E_{avg}=C_L * Vdd^2 * \alpha_{0\to1}$. Parameters related to computing power consumption at each level is shown Table 18.

Table 18. Adjust the parameters of each level after Vdd

Stage	1	2	3	4	5	6	7	8
C_L	2.96	3.49	6.30	8.49	15.35	24.59	31.42	50.46
$\alpha_{0\to1}$	0.1875	0.2500	0.2500	0.0625	0.2500	0.1875	0.1210	0.2490

So, E_{avg}=17.0652. Through the above calculation, the average power consumption after adjusting Vdd is less than the power consumption of 28.34761 in the optimal delay, and when Vdd is equal to 7.74, the power consumption decreases by about 39.80%.

4.5 The Influence of Vdd and Sizing of 1.5x Delay of Energy Consumption

Using this formula readers can see the impact of sizing and Vdd on delay.

$$td \approx \frac{C_L * Vdd}{I_d}, \tag{24}$$

So, we can assume that we adjusted sizing to make the delay a times larger [9]. According to the formula, if we want to maintain a 1.5x delay, Vdd should be adjusted and make the delay $\frac{1.5}{a}$x larger. So, function expressing Vdd in terms of a can be shown

$$Vdd = \frac{0.6+0.64a+\sqrt{0.4096a(a+1.875)}}{3} \tag{25}$$

So, function expressing sizing in terms of a can be shown

$$L = \frac{44.76a-34.2-\sqrt{(44.76a-34.2)^2-504.576}}{4.38} \tag{26}$$

Because of $E_{avg}=C_L * Vdd^2 * \alpha_{0\to1}$, so, function expressing $C_L * \alpha_{0\to1}$ in terms of a can be shown

$$C_L(\alpha_{0\to1}) = 10.464 + 0.370L \tag{27}$$

By using python and taking the derivative author find that this function is a monotonically decreasing and then monotonically increasing function, then, using the mathematical method of Newton-Raphson method, author get the zero value of the first derivative of our deduced relation [10]. So, a=1.281, the power consumption is equal to 9.72 and decreases by about 65.70%.

5 Conclusion

In this study, a unique 4-bit absolute value detector was created to generate a circuit with low energy consumption and little delay. This paper optimizes the circuit by adjusting the gate sizing and Vdd to achieve the best power consumption. In this paper, logic gates with low logic effort are used whenever possible by simplifying the computation. Eight components are included in the critical path in conjunction with the input buffer circuit. Then, according to the CMOS structure diagram and the principle of topology, the logical effort and parasitic delay of each level are calculated. The transmission gate is redesigned with a buffer to compose a compound gate, which greatly reduces the parasitic delay of the gates. In the chapter on finding optimal power consumption, by using python, by analyzing the influence of gate size and vdd on power consumption, Newton-Raphson method is used to obtain the relationship between them under the condition of constant delay (1.5x optimal delay) and optimal power consumption. Thus, the optimal power consumption is calculated. When the circuit reaches the optimal delay of 44.76, the energy consumption is 28.34761 C when Vdd is equal to one volt. When the circuit delay reaches 1.5 times of the optimal delay 67.14, according to the Newton-Raphson method, the Vdd of the optimal power consumption is 0.9022V, and the optimal power consumption is equal to 9.72C. Therefore, by sacrificing only 0.5 times the delay, this design can reduce the circuit power consumption by up to 65.70% . In this paper, based on transmission gate and static CMOS logic, a low power 4-bit absolute value detector circuit is designed. At the same time, it also provides a way to simplify the comparator of parallel logic through truth table and can also promote the development of serial logic comparator based on transmission gate theory. Because all the calculations in this paper are based on theoretical calculations, the obtained values are based on the results of the simulation circuit, in practice may affect the actual performance of the circuit due to heat accumulation, and some environmental noise will also affect the work of the transistor. Other wisely, in industrial production, new materials and more advanced manufacturing industry can be used to improve the performance of integrated circuits. However, limited by the time of this study, this paper did not explore the influence of the above factors on circuits, and relevant research is the direction of the author's next exploration.

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