Memory Bitcells: Research on Structures, Performance, Challenges and Innovation Trends

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Abstract. This paper comprehensively investigates bitcell architectures in traditional and emerging memory technologies, including SRAM, DRAM, NAND Flash, STT-MRAM, ReRAM, and FeRAM. As the foundational unit of memory systems, bitcell design critically influences key performance metrics such as density, speed, power efficiency, and reliability. This paper analyses each memory type's classical circuit configurations, operational principles, and performance trade-offs. For instance, SRAM variants (6T, 8T, 9T) exhibit distinct stability-speed-area compromises; DRAM evolves from 1T1C to vertically integrated 2T0C structures to address scaling challenges; and NAND Flash balances density, cost, and endurance through 3D stacking. Additionally, this paper highlights recent advancements, such as Intel's RibbonFet-based SRAM and vertical STT-MRAM architectures, while concluding future research directions: enhancing stability, minimizing power consumption, optimizing area efficiency, and improving noise immunity. This work provides a systematic reference for advancing next-generation memory technologies.

Keywords: Memory bitcell, Circuit architecture, Performance optimisation, Emerging trends, Memory types

1 Introduction

The advancement of memory technology has been fueled by growing needs for greater density, quicker access, and reduced power usage. Early magnetic core memories from the 1960s to 1980s had slow speeds (μs-range) and small capacities (KB-scale). DRAM and NAND Flash were the most popular between 1990 and 2010, reaching GB-scale density but having physical drawbacks such as leakage currents and limited write cycles. Because of its quick access characteristics, SRAM was the preferred high-speed cache memory. After the 2010s, a new generation of non-volatile memories, including STT-MRAM, ReRAM, FeRAM, and PCM, emerged in response to the limitations of conventional memory technologies. These emerging memory types make use of cutting-edge designs and materials. For example, ReRAM depends on the resistive switching of materials such as metal oxides, whereas STT-MRAM uses spin-transfer torque to manipulate magnetic states for data storage. By providing potential answers to issues like leakage currents and finite write cycles, their introduction seeks to go

© The Author(s) 2025
A. J. Moshayedi (ed.), *Proceedings of the 2025 2nd International Conference on Electrical Engineering and Intelligent Control (EEIC 2025)*, Advances in Engineering Research 279,
https://doi.org/10.2991/978-94-6463-864-6_39

beyond the physical constraints of earlier memory technologies and pave the way for new developments in the field.

Bitcells, the basic storage units, directly determine memory performance. DRAM cells, for instance, take up about $6F^2$ of space as opposed to $4F^2$ for ReRAM, while SRAM achieves read-write latency of less than 1 ns as opposed to about 50 μs for NAND Flash. Crosstalk in 3D NAND, write endurance in resistive memories, and stability degradation in scaled SRAMs are examples of persistent issues. This study systematically examines bitcell designs from various memory types, assesses their advantages and disadvantages, and suggests directions for further development.

2 Traditional Memory Bitcells Circuit Configurations and Characteristics

2.1 Static Random Access Memory (SRAM)

With the development of semiconductor technology towards deep submicrons and the improvement of the degree of integration of integrated circuits, SRAM has become increasingly important in electronic systems. The bitcell of SRAM, as the basic unit for data storage, reading, and writing, has a design that affects the performance of SRAM in terms of stability, read-write ability, and power consumption. The following introduces several traditional SRAM bitcell designs, characteristics, and cutting-edge achievements of SRAM bitcells.

Diverse Structures, Characteristics, and Cutting-Edge Achievements of SRAM Bitcells. The most basic and traditional design in the study of low-power SRAM design and performance analysis based on electrostatically doped tunnel CNTFETs [1] is the 6T SRAM bitcell. Fig. 1 depicts the structure of the 6T SRAM Conventional Bitcell. Composed of six transistors, it contains two cross-coupled CMOS inverters, each consisting of one PMOS and one NMOS, along with two NMOS transmission gates. The cross-connected inverters form a stable latch structure for data storage, while the transmission gates control the read-write operations. This structure has the significant advantages of simplicity in implementation and fast read-write speed. However, as the process enters the deep-submicron stage, the continuous reduction in transistor size leads to a decrease in static noise margin, severely impacting storage stability. Moreover, the relatively large number of transistors occupies a large chip area, posing obstacles to improving storage density.

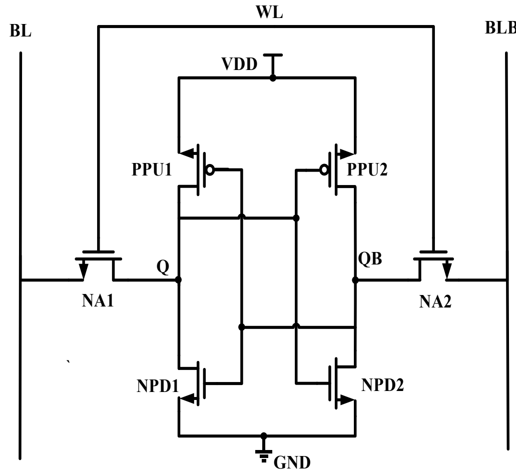

Fig. 1. 6T SRAM Conventional Bitcell.

The 8T SRAM bitcell is depicted in Fig. 2 [2]. Two transistors are added to the 6T layout to optimize read performance. The additional transistors create an independent read port, minimize interference on storage nodes, permit some read-write parallelism, and fix 6T misreading issues brought on by bit-line voltage swings. However, more transistors expand chip area, lower storage density, and increase power consumption, making them unsuitable for power-sensitive scenarios. The study of 8T read performance is embodied in the single-ended 8T SRAM cell suggested in this research, which uses a read buffer to increase stability. The degree to which the two 8T bitcells seen in Fig. 2 and Fig. 3 enhance read performance varies: Power-cut 8T SRAM and feedback-cut 8T SRAM [2]. By severing power channels during readings to reduce current and to improve stability, the Power-cut type reduces excess power and data interference in power-conscious scenarios. The RobbinFet Feedback-cut 8T SRAM uses a feedback circuit to monitor storage nodes. High-precision applications depend on data stability and read accuracy, which are ensured by cutting interfering feedback channels when read risks are identified. Similar to 8T SRAM, both architectures must balance performance and limitations due to their larger area and higher power.

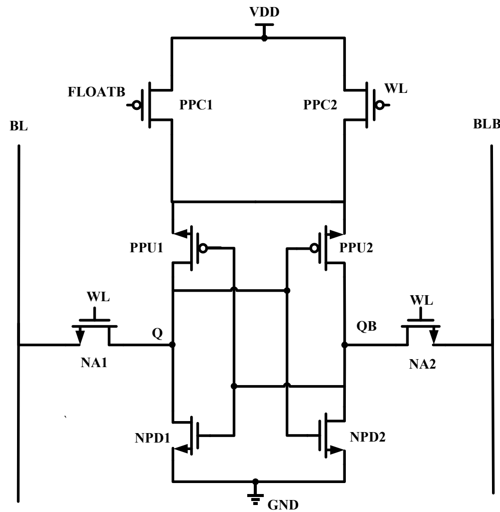

Fig. 2. Power-cut 8T SRAM Bitcell [2].

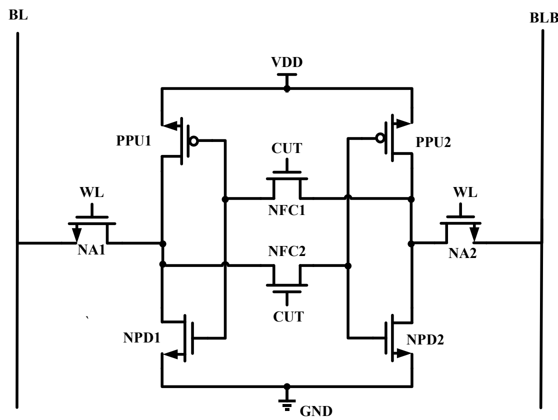

Fig. 3. Feedback-cut 8T SRAM Bitcell [2].

The study also discusses the 9T SRAM bitcell [2], an improvement over the 8T structure with an extra transistor. It maximizes the storage cell's retention properties and increases storage nodes' stability and noise resistance. This arrangement gives the bitcell more robustness, as shown in Fig. 4. It offers more stable data storage. It shows excellent static noise margin performance when facing disturbances like temperature and voltage changes. However, akin to the 8T bitcell, the 9T variant grapples with area and power consumption challenges. As illustrated in the circuit diagram, the transistor increment directly translates to a further expansion of the chip area [3]. This physical enlargement results in significant upticks in static and dynamic power consumption, posing substantial hurdles to effective power management.

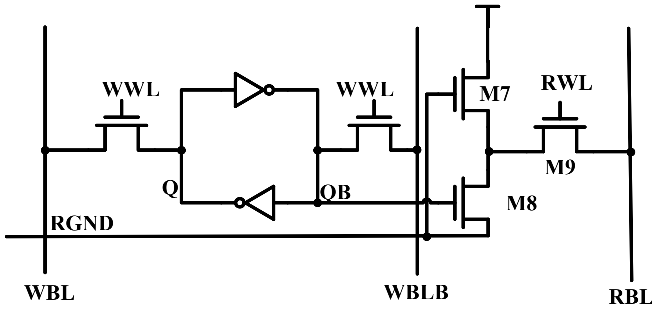

Fig. 4. 9T SRAM Bitcell [2].

The 7T SRAM bitcell strikes a balance between power consumption, area, and performance. Fig. 5 depicts the structure of the 7T Proposed SRAM Bitcell, which was introduced as a hybrid GC-eDRAM/SRAM bitcell for reliable low-power operation [4]. The standard 7T adopts a single-ended read architecture, saving one transistor. During reading, the storage-node signal is converted into a single-ended output. This design maintains good read stability and has a smaller area than 8T and 9T, which is conducive to improving storage density. The power consumption is also reduced due to the decrease in transistors. However, the anti-interference ability of the single-ended architecture is relatively weaker than that of the differential architecture. A trade-off must be made in practical applications according to the performance, area, and power consumption requirements. In some literature exploring the design of new-type SRAM bitcells, 7T SRAM bitcells' attempts to balance performance and resources are mentioned.

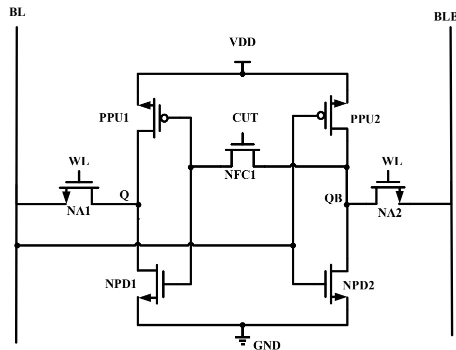

Fig. 5. 7T SRAM Bitcell [4].

In the landscape of cutting-edge SRAM advancements, Intel made significant revelations at the 2025 International Solid-State Circuits Conference (ISSCC). High-current 6T SRAM (HCC) and high-density 6T SRAM (HDC) designs were successfully realized by Intel by utilizing Intel 18a Ribbonfet technology and back-side power-via

technology [5]. The RibbonFET transistors optimise performance, density, and power consumption. Meanwhile, via technology, the power mitigates power droop and refines the peripheral circuit. When measured against conventional FinFET designs, RibbonFET HCC shows advantages in enhancing the $Vmin$ performance. Without the use of aid circuitry, optimization is possible. The performance and the storage density can be further improved by utilizing write-assist technologies [6]. This showcases Intel's prowess in SRAM innovation and sets new benchmarks for the industry, indicating the potential directions for future SRAM development.

In summary, the 6T SRAM bitcell has a simple structure and fast read-write speed, but in the deep-submicron process, it faces problems such as reduced static noise margin, large chip area, and limited storage density; the 8T SRAM bitcell optimises the read performance by adding transistors, reducing read interference and achieving a certain degree of read-write parallelism, but with an increase in area and power consumption; the 9T SRAM bitcell further adds transistors to focus on improving the stability and noise - resistance of storage nodes, but the area and power - consumption problems are more prominent; the 7T SRAM bitcell adopts a single-ended read architecture and achieves a good balance among performance, area, and power consumption, with a small area and low power consumption, but relatively weak anti-interference ability. Future SRAM bitcell design must improve performance (such as stability and read-write speed), reduce power consumption, minimise chip area to increase storage density, and enhance anti-interference ability. The design direction based on 18A RibbonFET technology and back-side power-via technology demonstrated by Intel at ISSCC 2025 provides new ideas for balancing these factors [6].

2.2 Embedded Dynamic Random Access Memory (eDRAM)

Dynamic random-access memory (DRAM) can satisfy large-scale data storage requirements. Its high storage density and low cost make it indispensable to modern computer systems. However, as application requirements and technological advancements have grown, standard DRAM has become a performance-enhancing bottleneck because of its high energy consumption and significant data transmission latency.

eDRAM, or embedded dynamic random access memory, was created to overcome several limitations. Using DRAM technology, logic circuits and storage units are integrated into a single chip, combining compute and storage capabilities. This integration enhances system performance and permits more intricate operations through on-chip logic circuits, lowering energy consumption and data transfer delay.

Diverse Structures, Characteristics, and Cutting-Edge Achievements of eDRAM Bitcells. A 1T1D eDRAM bitcell, which is composed of one storage npn diode (designated "1D") and one control fin-field-effect transistor (FinFET, designated "1T"), which is depicted in Fig. 6, was introduced by E. Ray Hsieh [7]. A FinFET's gate is floated to create the diode. The drain of the FinFET functions as the diode's anode, while the source does the same for the diode. The diode's anode is connected in series with the control FinFET's source, the word line (WL) is connected to the gate, the bit

line (BL) is connected to the drain, and the source line (SL) is connected to the diode's cathode. There are several benefits to this 1T1D eDRAM bitcell. It is tiny and has a high integration density, to start. Despite having a bit density of 41.32Mb/mm^2, which allows for the integration of more memory cells in a constrained space, the cell size is only 0.0242μm^2, or 15.8% of that of a 6T SRAM. Second, it may increase data processing speed by achieving high-speed reading and writing under low-voltage power supplies. Third, this memory cell has a good data retention time, which can guarantee stable data storage within a specific time frame and satisfy the needs of data storage timeliness in most application scenarios.

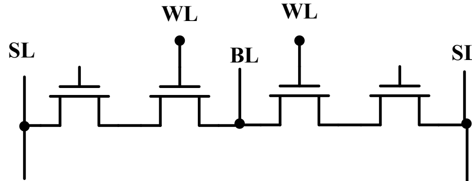

Fig. 6. 1T1D eDRAM memory cell [7].

Bar-Ilan University illustrated a single-supply 3T gain-cell (GC) embedded dynamic random-access memory (eDRAM) bitcell suitable for low-voltage and low-power applications. Its structure consists of a write port, a read port, and a storage node (SN) [8]. The complementary transmission gate of the write port is composed of a PMOS write transistor (PW) and an NMOS write transistor (NW), which are connected to the complementary word lines WWLp and WWLn, espectively, and data is driven through the cstandardwrite bit line (WBL). The read port is based on an NMOS device (NR). The storage node is composed of the parasitic capacitance (C_{SN}) of the three devices and the stacked metal interconnection. Moreover, the entire cell is constructed with standard threshold voltage (V_T) transistors and is fully compatible with standard digital CMOS technology, as shown in Fig. 7. This memory cell has significant advantages. It uses a single-supply voltage and does not require boosted signals, avoiding the complex power-supply-related problems of traditional GC-eDRAM, which facilitates system integration. Its complementary transmission gate can transmit strong signals to the storage node, enhance the initial data level, improve the data retention time, achieve fast write access, and reduce the interference caused by charge injection and clock feed-through.

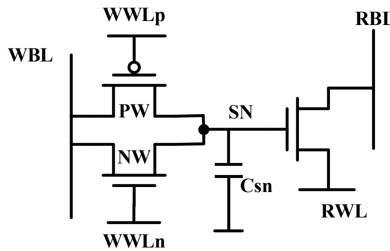

Fig. 7. A 3T GC [8].

A unique 4T GC-eDRAM bitcell was offered by EnICS Labs in 2024 as a new solution for high-performance embedded memory applications [9]. Its structural design uses a special arrangement of transistors to achieve differential readout. Four transistors make up this bitcell, as shown in Fig. 8: three read transistors (NR, PR, and NS) and one write transistor. During read operations, the RBL and the SA's reference node are precharged to the intermediate voltage V_{dmin}. Differential readout is made possible when the RWL is enabled since the voltage of the RBL varies according to the stored logic state. The WWL is activated to transmit the voltage on the WBL to the storage node SN during write operations. The source of the PR transistor is connected to the RWL power supply line, and low-threshold voltage (LVT) transistors are also utilized to maximize the read duration and prevent short-circuit problems brought on by the SN voltage degradation. It offers several benefits in terms of performance: By implementing the differential readout technique, the requirement for an external reference voltage V_{ref} is removed, eliminating associated issues and possible inaccuracies. The access time can be up to three times faster than conventional GC-eDRAM, equivalent to the SRAM read time. The RWL boosting approach with LVT transistors allows for a read speed of up to 55 ns. The layout area of a 65nm CMOS technology is 0.8316μm^2. The bitcell area can be decreased by up to 30% as compared to conventional SRAM solutions, which enhances the chip integration density.

The 3T GC-eDRAM bitcell in 16-nm FinFET technology is shown in Fig. 9. It has a mixed-V_T 3T gain-cell structure, a write port that uses a single-fin NMOS device, and a subthreshold leakage suppressed by lowering the WWL voltage below GND [10]. This structural design has many benefits, including a half reduction in bitcell size compared to a 6T SRAM with the same design rules, a significant increase in data retention time, a decrease in refresh power consumption, and improved memory availability. It also has a wide operating voltage range and strong temperature adaptability.

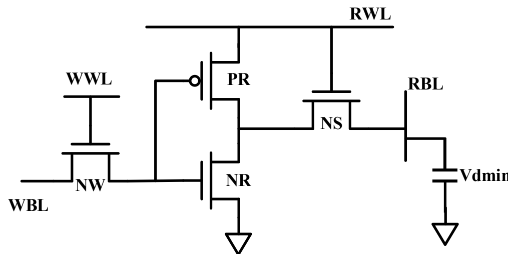

Fig. 8. 4T eDRAM bitcell [9].

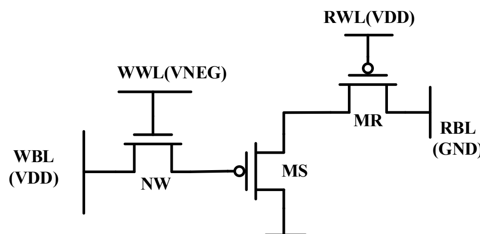

Fig. 9. 3T GC-eDRAM bitcell in 16-nm FinFET technology [10].

2.3 NAND Flash

NAND Flash technology is currently the most popular integrated method for non-volatile storage of large amounts of data. Its success can be attributed to the continuous improvement and miniaturization process that started in the late 1980s [11]. NAND Flash has recently overcome the 1-Tb/in² barrier in volumetric and planar storage density, surpassing magnetic recording on hard disk drive (HDD) platters, marking a significant milestone [11].

This technological progression has steadily driven down NAND technology's cost per gigabyte (GB). As a result, it has been able to penetrate and cater to an expanding range of applications and market segments. Next, this paper will focus on introducing the diverse structures, characteristics, and cutting-edge achievements of NAND Flash bitcells. The structural diversity encompasses various cell designs that have evolved to optimise storage density and performance. Their characteristics involve unique electrical and physical properties influencing data storage and retrieval. Meanwhile, the cutting-edge achievements represent the latest breakthroughs in enhancing reliability, speed, and capacity, driving NAND Flash technology to new heights in data storage.

Diverse Structures, Characteristics, and Cutting-Edge Achievements of NAND Flash Bitcells. NAND flash bitcells' fundamental architecture depends on charge-trap layers or floating-gate transistors. SLC uses a single floating-gate transistor, which requires just two states ("0" for high V_{TH}) and ("1" for low V_{TH}), in conventional 2D planar topologies. Electrons are injected into or released from the floating gate to change the threshold voltage (V_{TH}). Such systems employ basic peripheral circuits, such as voltage pulse generators and sensing amplifiers, to achieve microsecond-level response times, as Micheloni noted in their book [11]. Multi-level voltage partitioning makes multi-bit storage possible for Multi-Level Cell (MLC), Triple-Level Cell (TLC), Quad-Level Cell (QLC); for instance, MLC requires exact control over four windows, corresponding to 2-bit combinations. The threshold voltage distribution in MLC NAND flash memory was illustrated by DSSC of Carnegie Mellon University (2013). MLC's programming-verification circuits require incremental step pulse programming (ISPP) to iteratively approach target voltages, which results in 3-5× higher write latency than Single-Level Cell (SLC), according to characterization, analysis, and modeling [12].

With thousands of layered memory cells, 3D NAND (e.g., TLC/QLC) uses vertically stacked charge-trap structures (e.g., 3D-CTF, Charge Trap Flash). In 3D NAND Technology: Implications for Enterprise Storage Applications [13], IBM emphasized that substituting charge trap layers (such as silicon nitride, SiN) for floating gates causes electrons to be localized within insulating layers, significantly lowering inter-cell interference. For instance, TLC distinguishes 3-bit data through 8 states, requiring high-precision analog-to-digital converters (ADCs) and dynamic voltage compensation circuits to mitigate temperature drift and read noise—a design approach frequently reported at ISSCC conferences (e.g., Samsung's 2021 adaptive read compensation architecture). QLC divides into 16 narrow windows, integrating deep-learning DSPs and LDPC error correction codes into its peripheral circuits. As predicted in the University of California, San Diego's foundational study [14], QLC relies on real-time voltage calibration and soft-decision decoding to enhance reliability.

Comparatively, SLC's simple structure (single polysilicon floating gate) and low interference limit peripheral circuitry to ~15% of total area, whereas QLC's complex voltage management and error correction demand >50% peripheral overhead [11]. The shift from 2D floating-gate to 3D charge-trap architectures fundamentally prioritises density through vertical stacking, while relying on circuit-level intelligence to compensate for physical-layer reliability degradation—a trend validated and ISSCC 2022 reports on 4-bit/cell QLC advancements [15].

In conclusion, developing NAND bitcells requires balancing storage density, cost, and reliability. Although 3D NAND leads the current technological innovation, future designs still need to address the limitations of QLC and explore new materials. Continuous research on cell architectures and error management will lay the foundation for next-generation high-density storage solutions.NAND Flash technology is currently the most popular integrated method for non-volatile storage of large amounts of data. Its success can be attributed to the continuous improvement and miniaturization process that started in the late 1980s [11]. NAND Flash has recently overcome the 1-Tb/in^2 barrier in volumetric and planar storage density, surpassing magnetic recording on hard disk drive (HDD) platters, marking a significant milestone [11].

3 Emerging Non-Volatile Memory Bitcells Circuit Configurations and Characteristics

3.1 Spin-Transfer Torque Magnetoresistive Random Access Memory (STT-MRAM)

STT-MRAM is a promising option for next-generation storage systems due to semiconductor technology's ongoing search for high-density, low-power non-volatile memory solutions. The bitcell of STT-MRAM, which is the basic unit for non-volatile data storage and retrieval, significantly impacts key performance measures, including write speed, durability, and power consumption. Several exemplary STT-MRAM bitcell architectures are presented below.

Diverse Structures, Characteristics, and Cutting-Edge Achievements of STT-MRAM Bitcells. The traditional 1T1J-based STT-MRAM bitcell has a simple structure with one Magnetic Tunnel Junction (MTJ) and one NMOS transistor, depicted in Fig. 10 [16], offering high integration. It has low write current and good scalability, making it suitable for future technology nodes. A thin oxide barrier layer divides the two ferromagnetic layers comprising the MTJ, the primary data storage component. The reference layer's magnetic field direction is fixed, whereas a magnetic force can alter the free layer's magnetic field direction. The NMOS transistor manages the MTJ's access. The transistor conducts when the word line (WL) is set high, enabling read and write operations on the MTJ.

Fig. 11 depicts the 2T2MTJ STT-MRAM static gain cell, a memory cell comprising two transistors and two magnetic tunneling junctions (MTJs) [17]. A thin tunneling oxide layer sits in the center of the two ferromagnetic layers (a free layer and a pinned layer) that comprise the MTJ portion. The complementary states of the two MTJs are

coupled in sequence. The polarity of the free layer can be altered by varying the current's direction and magnitude via the MTJ, which will result in the MTJ exhibiting either an antiparallel state (Rap) or a parallel state (Rp) for data storage. This complementary MTJ state setup increases data reading and storage reliability in the 2T2MTJ structure.

Southeast University use a 4T2MTJ bitcell, which consists of four transistors and two MTJs [18]. As illustrated in Fig. 12, MTJ1 and its partner MTJ2 are situated between BL and SL. Upon receiving a read voltage from WL, M1 and M2 establish a latching structure. While columns in the array share BL and BLB, rows share SL, SLB, and WL. The benefits of this construction are numerous. Only a single capacitor may be charged during each read cycle thanks to the latch structure created by the bitcell's cross-coupled transistors (M1 and M2). This not only lowers the energy cost of the read operation because the energy is mainly used to charge and discharge a single capacitor, but it also simplifies the circuit components involved in charging the capacitor, makes the circuit design and operation less complicated, and increases the circuit's stability and dependability.

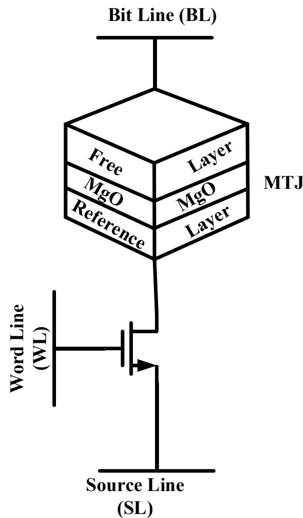

Fig. 10. The bitcell structure of 1T1MTJ.

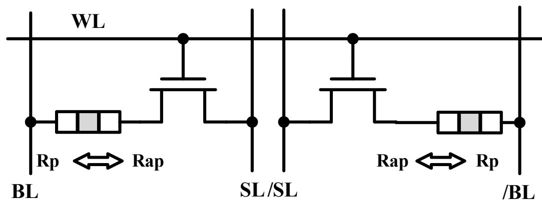

Fig. 11. 2T2MTJ Dual bitcell structure [17].

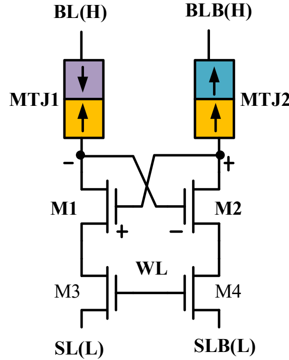

Fig. 12. Construction of the 4T2MTJ bitcell. Adapted from [18].

In 2021, at the IEEE/ACM International Symposium on Nanoscale Architectures, a computing-in-memory scheme of Series Bitcell in STT-MRAM (SBC-IM) based on STT-MRAM was mentioned [19]. The bitcell construction of this method consists of one MTJ and three transistors. The intrinsic low switching ratio issue of MTJ in computing-in-memory can be solved by connecting several bitcells in series in a column. The development of bitcell structures in STT-MRAM technology has been continuous at the International Solid-State Circuits Conference (ISSCC). A pseudo 2T-2MTJ bitcell has been built by Southeast University's School of Electronic Science and Engineering. The transistor as a whole is activated while writing. The area is decreased when the computing-in-memory (CIM) feature is activated because the input data on the word lines (WLs) activates half of the transistors. This bitcell has a twofold readout margin as compared to the 1T-1MTJ cell. These developments show how STT-MRAM technology constantly evolves and emphasize how crucial bitcell structure innovation is to boosting performance and broadening application scenarios.

3.2 Resistive Random Access Memory (ReRAM)

Resistive Random Access Memory (ReRAM) has become a prominent contender for next-generation non-volatile storage because of its low power consumption, high density, and circuit integration compatibility. Drawing on new findings, this section examines several ReRAM bitcell architectures and their uses.

Diverse Structures, Characteristics, and Cutting-Edge Achievements of ReRAM Bitcells. Because of its exceptional benefits, ReRAM has garnered much interest in contemporary storage technology. The architecture of its bitcell structure primarily determines its performance. The 1T1R ReRAM bitcell, as shown in Fig. 13(a), (b), (c), consists of an NMOS access transistor and a resistive memory device based on HfO_X [20]. Bit lines, source lines, and word lines control it. The read operation has two modes: voltage mode and current mode. The SET and RESET operations accomplish the transition between high and low resistance states and are depicted in Fig. 11 b, c. However, design difficulties exist because of the NMOS transistor's less-than-ideal

properties. The voltage drop during the RESET operation affects the lower limit of the LRS value and the increase of the WL voltage, thereby influencing the device performance and reliability.

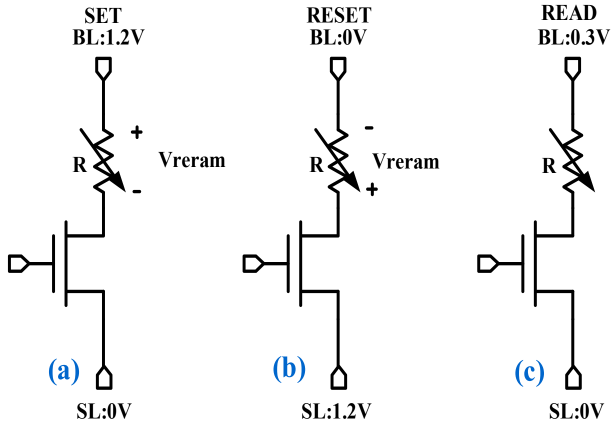

Fig. 13. 1T1R The essential functions of a ReRAM bitcell are (a) set, (b) reset, and (c) read [20].

In comparison, Fig. 14 [21] displays the 4T2R ReRAM bitcell. Bipolar ReRAM devices are combined with two N-type transistors and two ReRAM devices to form a differential 2T2R bitcell. Two more access transistors are also included to realize the column bit-line pair. As illustrated in Fig. 15a, b, it reverses the SET and RESET procedures and supports two-dimensional read operations to prevent read disturbances. Compared to the conventional 1T1R ReRAM, its 2D access capabilities can lower energy usage by up to 82% and memory access latency by up to 88% in various matrix operations.

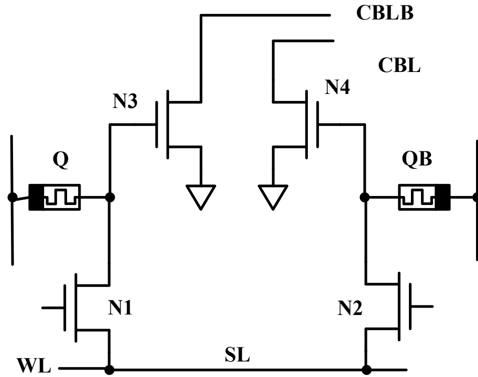

Fig. 14. 4T2R ReRAM bitcell structure. Adapted from [21].

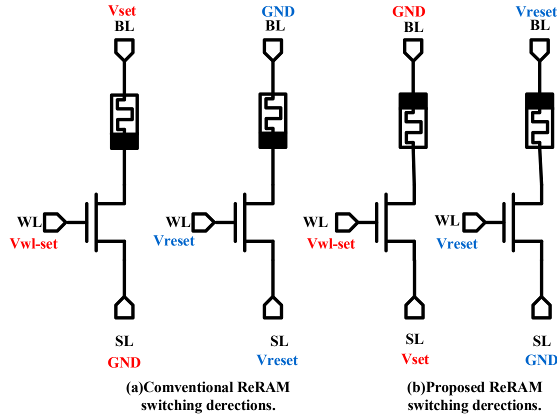

Fig. 15. (a) Conventional ReRAM switching directions. (b) Proposed ReRAM switching directions [21].

Resistive Random-Access Memory (ReRAM) has advanced significantly recently and attracted much attention worldwide. Samsung Electronics demonstrated a 1T4R ReRAM array based on a 14nm FinFET at ISSCC 2023 [22]. This creative design achieved an excellent write performance of 8GB/s by using a time-voltage multiplexing architecture for parallel writing. These developments demonstrate how quickly ReRAM technology is evolving and how it can potentially transform the storage sector completely.

3.3 Ferroelectric Random Access Memory (FeRAM)

As semiconductor technology advances, FeRAM has become crucial in electronic systems. The design of its bitcell, the basic data-storage unit, affects performance in ways such as stability and power consumption. Here are several classic FeRAM bitcell designs.

Diverse Structures, Characteristics, and Cutting-edge Achievements of FeRAM Bitcells. The several architectures of FeRAM bitcells are described in relevant papers. As per the research conducted by Infineon [23], the 1T1C FeRAM bitcell, seen in Fig. 16, comprises a single NMOS transistor and a ferroelectric capacitor. The transistor switches for read/write operations, and the capacitor uses polarization state switching to store data. As illustrated in Fig. 17 [24], the 2T2C bitcell extends the 1T1C architecture with an extra transistor and capacitor and two ferroelectric capacitors for storing complementary data for differential read operations. 3D-Feram overcomes planar density limitations by vertically stacking bitcell layers and connecting them via TSVS and inter-layer technologies. The fin-shaped channel of the FinFET, which improves current drive and switching speed, is combined with ferroelectric materials in the FinFET-FeRAM design, which is based on FeRAM and uses anti-ferroelectric capacitors for high-speed and high-density embedded memory [25].

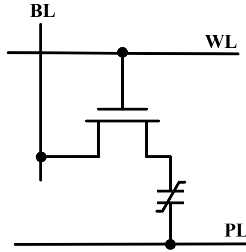

Fig. 16. ITIC FeRAM bitcell structure [24].

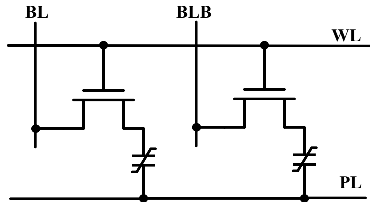

Fig. 17. 2T2C FeRAM bitcell structure[24].

In summary, each FeRAM bitcell type has distinct advantages and drawbacks. The 1T1C bitcell offers simplicity, fast read-write speeds, and low write power, but faces challenges in scalability and density due to ferroelectric property degradation at smaller scales. The 2T2C bitcell enhances read reliability and enables limited parallel operation, yet sacrifices area and increases power consumption with additional components. 3D-FeRAM provides a significant density boost, ideal for high-capacity applications, but comes with complex manufacturing requirements. The 1T bitcell stands out for its ultra-compact design and CMOS compatibility, though it suffers from weak signal strength and noise susceptibility. Finally, the FinFET-FeRAM offers high performance and scalability, but its integration complexity due to precise ferroelectric deposition on 3D fin surfaces raises manufacturing costs.

Future designs should improve speed, stability, and anti-interference capabilities while reducing power consumption and minimizing chip area.

4 Conclusion

The bitcell designs used in standard memory technologies are carefully examined in this work. Performance and circuit design constrain conventional memories like SRAM, DRAM, and NAND Flash. Although they encounter difficulties, emerging non-volatile memories like STT-MRAM, ReRAM, and FeRAM exhibit promise. Future studies should concentrate on increasing noise immunity, lowering power consumption, optimizing area, and boosting stability to develop next-generation memory technologies.

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