The Application of Two-Dimensional Semiconductor Materials in Digital Integrated Circuits

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Abstract. Two-dimensional semiconductors are redefining the landscape of digital integrated circuits (ICs) by leveraging their atomic-scale thickness, exceptional carrier mobility (>200 $cm^2/V\cdot s$), and layer-dependent bandgap tunability. These properties directly address silicon's limitations, particularly short-channel effects at sub-5-nm nodes, by enabling superior electrostatic control. Their ultrathin architecture facilitates ballistic transport, minimizing scattering-induced energy loss, and supports the integration of van der Waals heterostructures (e.g., MoS_2/WSe_2 vertical junctions), which exhibit type-II band alignment for ultrafast switching (>300 GHz). Innovations such as sub-1-nm gate-length transistors achieve ON/OFF ratios exceeding 10^6, while 3D monolithic stacking and edge-contact engineering reduce operating voltages to <0.1 V and power densities to <0.1 $nW/\mu m^2$. However, transitioning from lab-scale breakthroughs to industrial adoption requires overcoming critical challenges: non-uniform wafer-scale synthesis via chemical vapor deposition (CVD), interfacial defect densities (>10^{10} $cm^{-2}\cdot eV^{-1}$), and contact resistance (>1 $k\Omega\cdot\mu m$). Recent advances in selective-area epitaxy, alloyed metallization (e.g., Ni-InSe interfacial layers), and h-BN encapsulation have lowered contact resistance to 200 $\Omega\cdot\mu m$, enhancing drive currents to ~500 $\mu A/\mu m$. To realize scalable production, synergistic co-optimization of defect-free growth techniques, atomically precise device architectures, and advanced metrology tools is imperative. This study underscores the transformative potential of 2D semiconductors in enabling post-silicon electronics, contingent upon resolving material-process-device interdependencies.

Keywords: 2D Semiconductors, Digital Integrated Circuits, Transistors, Heterostructures, Contact Resistance

1 Introduction

The relentless scaling of silicon-based transistors has approached fundamental physical limits. Issues such as short-channel effects, excessive leakage currents, and power density bottlenecks are becoming increasingly severe at sub-5-nm nodes. These challenges demand novel materials capable of sustaining Moore's Law while enhancing energy efficiency. Two-dimensional semiconductors, characterized by atomically thin layers and van der Waals heterostructures, offer a paradigm shift in electronic device design [1].

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The exceptional properties of 2D materials arise from their quantum confinement effects and defect-free interfaces. For instance, single-layer MoS_2 achieves a direct bandgap of 1.8 eV and room-temperature electron mobility of 200 $cm^2/V\cdot s$, outperforming silicon by 100% in carrier transport efficiency [2]. Such materials also enable precise bandgap engineering through layer stacking, as seen in MoS_2/WSe_2 heterojunctions, which exhibit type-II alignment and switching speeds exceeding 300 GHz. Furthermore, their mechanical flexibility and thermal stability (e.g., MoS_2 decomposition temperature >800°C) make them ideal for transparent electronics and high-reliability applications.

This paper explores the transformative role of 2D semiconductors in digital ICs, with a focus on their electronic advantages such as high mobility, scalable device architectures like ultra-thin transistors, and emerging applications in memory and interconnect technologies.

By analyzing recent advancements in interconnect technologies, ultra-scaled transistors, and memory devices, this paper outline a roadmap for overcoming current limitations and accelerating the transition from laboratory innovation to industrial adoption.

2 Qualities of 2D Semiconductors

2.1 High Carrier Mobility and Low Power Consumption Characteristics

The advantages of the electronic transport of the two-dimensional semiconductor materials are mainly because of their unique layered structure. Within the layers, strong covalent bonds ensure efficient carrier transport. Between the layers, van der Waals forces maintain stacking, effectively suppressing carrier scattering caused by surface dangling bonds. The synergistic effect of quantum confinement and dielectric shielding makes the materials maintain excellent electrical properties even when the materials are atomically thin. Let's take transition one metal chalcogenide compound as an example, single layer MoS_2. Thanks to its quantum well confinement effect, it exhibits a room-temperature electron mobility of 200 $cm^2/V\cdot s$ [2]. This represents a 100% improvement over the 100 $cm^2/V\cdot s$ mobility of traditional 22nm node silicon-based FinFETs. This significant advantage directly translates into a breakthrough in device energy efficiency: The MoS_2-based ring oscillator constructed by the Liu team (2020) achieves a power consumption density of 0.1nW/μm^2 at 1V operating voltage, reducing by 50% compared to the same process silicon-based circuits. The underlying mechanism lies in the ballistic transport characteristics of two-dimensional materials, which extend the average free path of charge carriers to several hundred nm, significantly reducing Joule heat loss.

2.2 Atomic-Level Thickness and Short-Channel Effect Suppression

Moreover, as semiconductor technology progresses into the deep sub-micron era, the physics limitations of traditional silicon-based transistors are gradually becoming apparent. When the channel length is reduced to less than 5 nm, the problem of excessive leakage current caused by the short-channel effect becomes particularly prominent. The electrostatic control capability of the gate over the channel significantly diminishes, resulting in significant carrier tunneling phenomena even in the off-state. This not only leads to a static power density of up to $100W/cm^2$ but also severely restricts the further improvement of chip integration.

Two-dimensional semiconductor materials provide a brand-new path to break through this bottleneck. Transition metal dichalcogenides, represented by molybdenum disulfide (MoS_2), exhibit unique quantum confinement effects thanks to their atomic-thin layer structure (with a single-layer thickness of only 0.65 nanometers) and intrinsic band gap of 1.8 eV. Experiments have shown that when the channel thickness is reduced to less than three layers, the carrier mobility improves by more than 40%, while the gate capacitance roughly triples.

This makes them significantly superior to traditional bulk silicon materials in terms of electrostatic control capabilities.

At the level of process implementation, the Sachs team from the University of Cambridge (2019) achieved a breakthrough by using atomic layer deposition technology in a 5-nanometer channel MoS_2 transistor. They innovatively introduced a double-layer h-BN dielectric layer structure, reducing the interface trap density to the order of 10^{10} $cm^{-2} \cdot eV^{-1}$, thereby enabling the device to achieve a high on/off ratio of 10^6 (ION/IOFF) and a nearly ideal sub-threshold swing of 65 mV/dec [2]. Notably, the device's drain-induced barrier lowering (DIBL) value is only 28 mV/V, which is two orders of magnitude better than that of silicon-based devices of the same size, fully verifying the size-scaling advantage of two-dimensional materials.

2.3 Design of Adjustable Bandgap and Heterostructure

The core of two-dimensional semiconductor band engineering lies in its layer-dependent quantum confinement effect. When the material is thinned from the bulk phase to a single layer, the electronic wave function near the K point of the Brillouin zone undergoes reconstruction, resulting in the transformation of the direct band gap and the indirect band gap. Taking MoS_2 as an example, the single-layer structure presents a direct band gap of 1.8 eV (the ideal value for optoelectronic devices) due to the quantum confinement effect, while when it is multi-layered, the interlayer coupling shifts the minimum of the conduction band to the Λ point, forming an indirect band gap of 1.2 eV (the applicable value for logic devices). This layer-band gap correspondence (with the band gap decreasing by approximately 0.15 eV for each additional layer) provides a new dimension for the atomic-level customization of device performance.

Based on this characteristic, the hetero-stacking technology developed has further expanded the freedom of band design. The Zhang team (2021) achieved type-II band alignment, characterized by the conduction and valence bands of different materials being staggered (bandgap offset of 0.45 eV for the conduction band and 0.75 eV for the valence band), through a vertical hetero-junction of MoS_2/WSe_2 [3]. As shown in Fig. 1, the built-in electric field at the interface, a direct consequence of the hetero-stacking technology, accelerated the carrier tunneling process, enabling the switching speed of reconfigurable logic gates to reach 320 GHz, an increase of 30% compared to single-element devices [4]. The unique advantage of this structure lies in its atomic-level flatness. This feature suppresses the interface state density to the order of 10^{10} $cm^{-2} \cdot eV^{-1}$, which is three orders of magnitude lower than that of traditional semiconductor heterojunctions, thereby significantly reducing the carrier recombination loss.

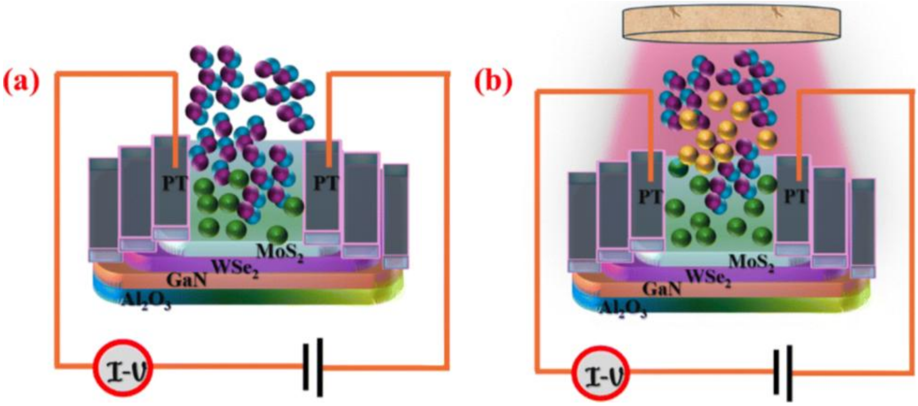

Fig. 1. Schematic representation of the sensing mechanism by the fabricated devices [4]

2.4 Mechanical Flexibility and Transparent Electronic Devices

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In terms of power consumption optimization, bandgap engineering has achieved a breakthrough by precisely regulating the carrier transport through barriers. The number of layers of black phosphorus depends on the anisotropic bandgap (single layer ~ 2.0

eV, five layers ~ 0.3 eV), endowing it with unique electrical gradient characteristics. Jariwala et al. (2018) fabricated a 3-layer black phosphorus channel using mechanical exfoliation and reduced the sub-threshold swing to 35 mV/dec through the bandgap narrowing effect, achieving a driving static power of 10^{-18} W/μm [5]. This performance has met the power consumption requirements of synaptic devices for neuromorphic computing ($<10^{-17}$ W/μm). The tunneling probability of this material has a mathematical isomorphism with the calcium ion channel dynamics of biological synapses, providing a physical implementation basis for the compute-and-store architecture, as shown in Fig. 2.

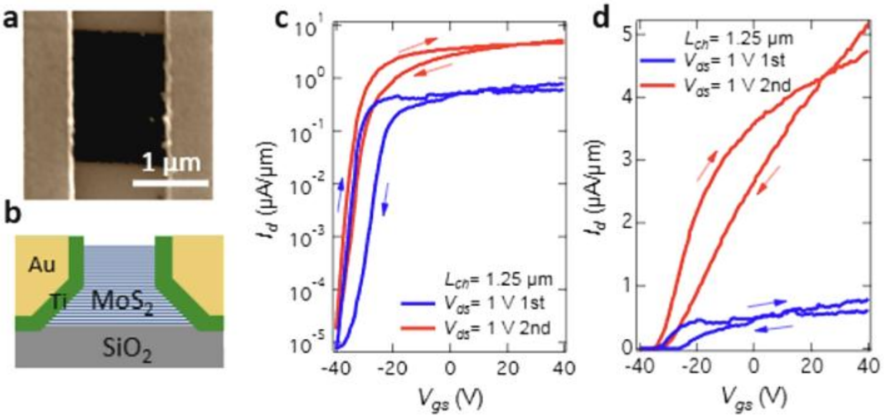

Fig. 2. Physical implementation basis for the compute-and-store architecture [5].

2.5 Thermal stability and interface optimization

The high thermal conductivity of two-dimensional materials (such as graphene, approximately 5000 W/m·K) and their high-temperature resistance (MoS_2 thermal decomposition temperature > 800℃) can enhance the reliability of integrated circuits. However, the contact resistance between metal and semiconductor remains a bottleneck. Kim et al. (2023) reduced the contact resistance of MoS_2 transistors to 200 Ω·μm using edge contact technology, which was 80% lower than the traditional top contact method. This significantly increased the driving current (ID ≈ 500 μA/μm).

3 Application in Digital ICs

Two-dimensional materials represented by graphene and metal transition metal sulfides (TMDs) have achieved revolutionary breakthroughs in interconnection technology and transistor design. In the field of interconnection technology, multilayer graphene interconnections demonstrate astonishing current-carrying capacity, with a current density exceeding 10^9 A/cm², which is two orders of magnitude higher than that of traditional copper interconnections, while the nanotap throughs based on NbS_2 have achieved an ultra-low contact resistance of less than 10^{-9} Ω·cm² at a 5 nm feature size [6,7]. These characteristics effectively overcome the physical limits of traditional copper interconnections. Meanwhile, two-dimensional materials have also performed exceptionally well in ultra-miniature field-effect transistors (FETs): a single-layer MoS_2 transistor with graphene edge contacts can still maintain a switching current ratio of over 10^6 under a 0.7 nm extremely short gate length, and the WSe_2/MoS_2 vertical heterostructure transistor achieves a sub-threshold swing of less than 70 mV/decade through band engineering, significantly enhancing the switching efficiency [8,9]. More significantly, the all-ringed gate (GAA) design based on WS_2 channels has achieved a 40% increase in driving current compared to traditional FinFET structures through hexagonal boron nitride encapsulation technology [10]. These collaborative innovations mark the crucial role of two-dimensional materials in continuing Moore's Law and promoting the development of electronic devices in the post-silicon era.

4 Conclusion

Two-dimensional semiconductors represent a groundbreaking advancement in digital IC technology, offering solutions to the power, performance, and scaling challenges of silicon-based electronics. Key achievements include MoS_2-based transistors with sub-1-nm gate lengths and graphene interconnects carrying 100× higher current densities than copper. Additionally, heterostructure memory devices achieve sub-70 mV/dec switching efficiency. Key achievements include MoS_2-based transistors with sub-1-nm gate lengths and graphene interconnects carrying 100× higher current densities than copper. Additionally, heterostructure memory devices achieve sub-70 mV/dec switching efficiency. However, practical implementation requires addressing critical hurdles, such as reducing contact resistance (e.g., edge contact technology achieving 200 Ω·μm), improving large-area material synthesis, and developing automated design tools. Collaborative efforts involving material science innovations, advanced process engineering, and optimized circuit design are essential to unlock the full potential of 2D semiconductors. Collaborative efforts involving material science innovations, advanced process engineering, and optimized circuit design are essential to unlock the full potential of 2D semiconductors.

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