Exploring Low Power Parallel Prefix Adder using Non-Conventional Logic Styles in Terms of Scaling Parameters

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Abstract. The demand for faster and energy- efficient arithmetic circuits continues to grow with the rise of modern VLSI applications. This paper explores a 4-bit Ladner-Fischer Parallel Prefix Adder (LF-PPA) implemented using non- conventional logic techniques such as Pass Transistor Logic (PTL), Double Pass Transistor Logic (DPTL), and Gate Diffusion Input (GDI). The proposed designs are analyzed in terms of power usage, silicon area, and layout efficiency, with simulations performed using DSCH3 and layouts generated in Microwind 3.1. Simulation outcomes demonstrate that the GDI-based approach yields the most compact area, whereas DPTL achieves the lowest power dissipation. These findings underline the trade-offs between compactness and energy efficiency. Although the prototype is limited to a 4-bit design, the results provide useful insights into how these logic styles may be extended to wider adders in large-scale integration, DSP units, and energy-conscious VLSI architectures. Overall, this study highlights comparative design perspectives for developing optimized prefix adders in advanced digital systems.

Keywords: Low Power VLSI, Ladner-Fischer Adder, Pass Transistor Logic (PTL), Double Pass Transistor Logic (DPTL), Gate Diffusion Input (GDI), Energy- Performance-Area (EPA), Parallel Prefix Adders, DSCH3, Microwind 3.1

1 Introduction

In modern Very Large Scale Integration (VLSI) design, achieving high speed, low power consumption, and minimal silicon area has become a crucial challenge, especially in portable and battery-operated devices. Arithmetic circuits, particularly adders, are the fundamental building blocks in processors, digital signal processing units, and communication systems. The overall performance of these systems is significantly influenced by the efficiency of the adder architecture used.

Parallel prefix adders (PPAs) are among the fastest adder structures because of their logarithmic delay characteristics and high degree of parallelism. However, as technology scales down to deep sub-micron and nano regimes, power dissipation and layout

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area become equally important as speed. Traditional CMOS implementations, though reliable, often result in higher power and area overhead.

To overcome these limitations, non-conventional logic styles such as Pass Transistor Logic (PTL), Dual Pass Transistor Logic (DPTL), and Gate Diffusion Input (GDI) have gained attention for their ability to reduce transistor count, minimize dynamic power, and optimize performance. By integrating these logic styles with efficient PPA architectures such as Ladner-Fischer adders, it is possible to achieve better trade-offs between speed, power, and area.

This research work focuses on analyzing and implementing different logic styles in the design of a low-power parallel prefix adder. The main objectives include reducing power consumption, optimizing area, and improving the efficiency of the adder architecture under scaling parameters. The design is modeled using DSCH3 and simulated in Microwind 3.1 to evaluate performance metrics such as propagation delay, power, and layout area.

2 LITERATURE REVIEW

Recent studies in Parallel Prefix Adders (PPA) show that architectural and logic optimizations can improve both speed and power efficiency. Approximate computing applied to Kogge–Stone Adders (KSA) reduces delay with minimal accuracy loss, making them suitable for multimedia applications. Sklansky adders offer lower power and hardware cost for digital filters compared to KSAs.

Optimizations of Ladner–Fischer Adders (LF-PPA), particularly 16-bit designs in 32 nm CMOS, demonstrate notable reductions in power and area, highlighting their relevance for low-power VLSI systems. Comparative studies suggest LF-PPA achieves superior energy efficiency relative to KSA and Brent–Kung structures.

In logic styles, techniques such as Pass Transistor Logic (PTL) and Gate Diffusion Input (GDI) reduce circuit area and dynamic power, while approximate PPA frameworks show that small accuracy trade-offs can yield significant power savings.

3 Design Methodology

The proposed design methodology focuses on optimizing 4-bit LF-PPA for low power and high speed, comprising three stages:

1. Architecture Selection: LF-PPA is chosen after comparing Kogge-Stone, Sklansky, and Ladner-Fischer structures for delay, area, and power trade-offs.

2. Logic Style Optimization: PTL, DPTL, and GDI are employed to reduce transistor count, propagation delay, and power dissipation. Approximate computing is applied in non-critical paths to further optimize energy efficiency.

3. Hardware Implementation: Designs are simulated in DSCH3, and layouts generated in Microwind 3.1. Metrics such as propagation delay, power, and area are evaluated for performance comparison.

3.1 Non-Conventional Logic Styles

- **Pass Transistor Logic (PTL):** Reduces transistor count and capacitance, improving speed, but may require buffering due to voltage degradation.
- **Double Pass Transistor Logic (DPTL):** Extends PTL using both n-type and p-type devices to maintain full voltage swing and lower static power.
- **Gate Diffusion Input (GDI):** Assigns signals to both gate and source, minimizing transistor usage and power while enabling multiple logic functions.

3.2 Ladner-Fischer Adder Design

- **Stages:** Pre-processing (generate Pi/Gi), carry generation (using black and gray cells), and sum computation.
- **Black Cells:** Compute both generate and propagate signals for carry computation.
- **Gray Cells:** Compute generate signals only, reducing area and delay.
- **4-bit Implementation:** Designs built using CMOS, PTL, DPTL, and GDI logic; simulations evaluate **area, power, and layout efficiency**.

4 Results and Analysis

The designed 4-bit Ladner–Fischer Parallel Prefix Adder (LF-PPA) was implemented using four logic styles—CMOS, Pass Transistor Logic (PTL), Double Pass Transistor Logic (DPTL), and Gate Diffusion Input (GDI)—and simulated using DSCH3 and Microwind 3.1. The evaluation parameters considered are power consumption and silicon area.

The Schematic of the CMOS-based 4 bit LF-PPA is shown in Fig.1, and simulation waveform is illustrated in Fig.2. The CMOS-based LF-PPA occupied an area of 272.6 μm^2 with a power dissipation of 6.167 µW.

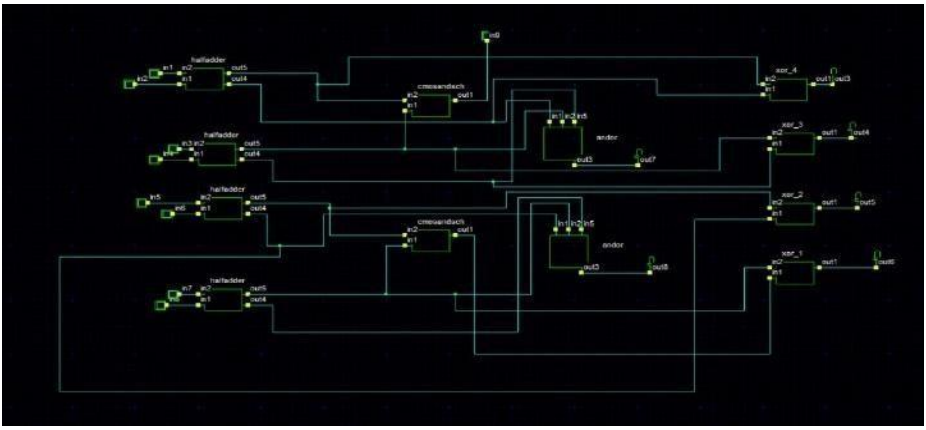

Fig. 1. Schematic of a CMOS-Based 4-Bit Ladner- Fischer Parallel Prefix Adder

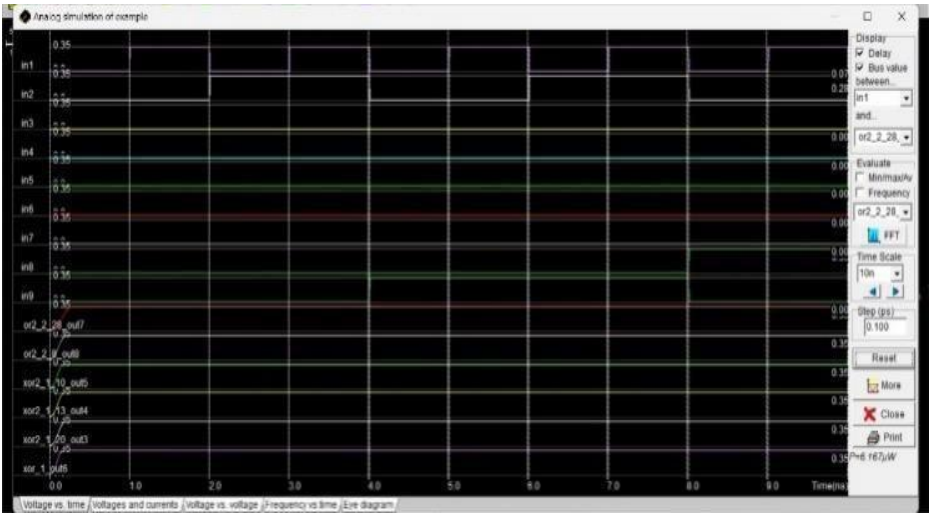

Fig. 2. Detailed Simulation Results of CMOS-Based 4- Bit Ladner-Fischer Adder

The PTL-based design reduced area to 198.9 μm² and power to 3.925 μW due to fewer transistors but experienced minor voltage degradation.The Schematic and transient simulation results of PTL-based design are depicted in Figs. 3 and 4, respectively

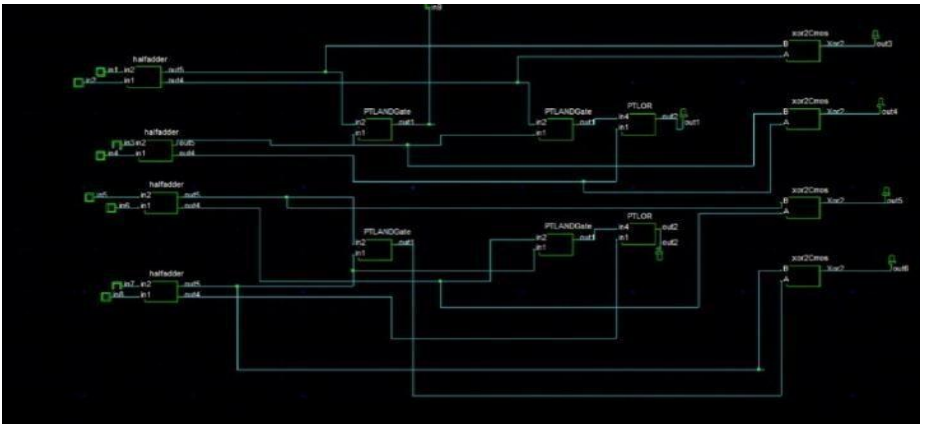

Fig. 3. Schematic of a PTL-Based 4-Bit Ladner- Fischer Parallel Prefix Adder

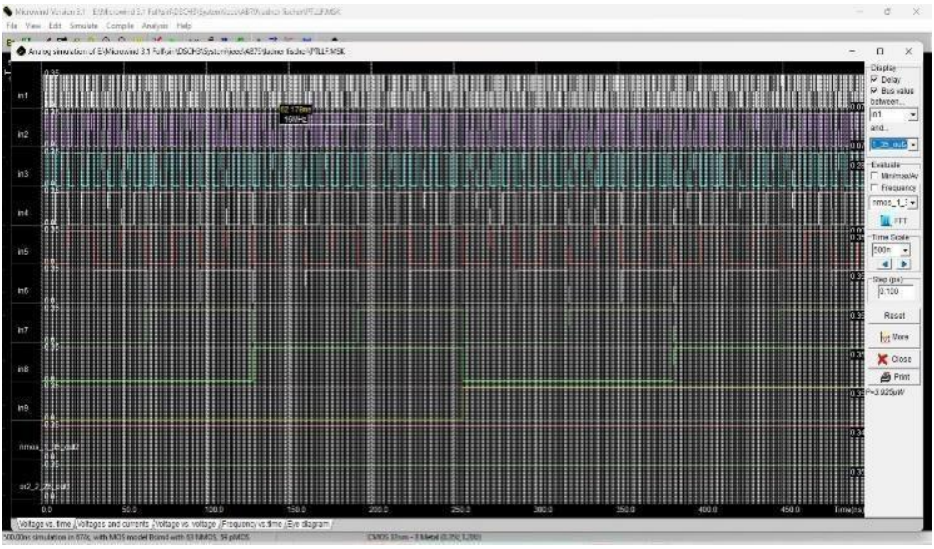

Fig. 4. Transient Simulation Results of PTL-Based 4-Bit Ladner-Fischer Adder

The DPTL-based design maintained full voltage swing and achieved the lowest power consumption of 0.830 µW, although its layout area increased to 370.1 µm².The schematic represent and transient simulation of the DPTL-Based LF-PPA are shown in Fig. 5 and 6, respectively

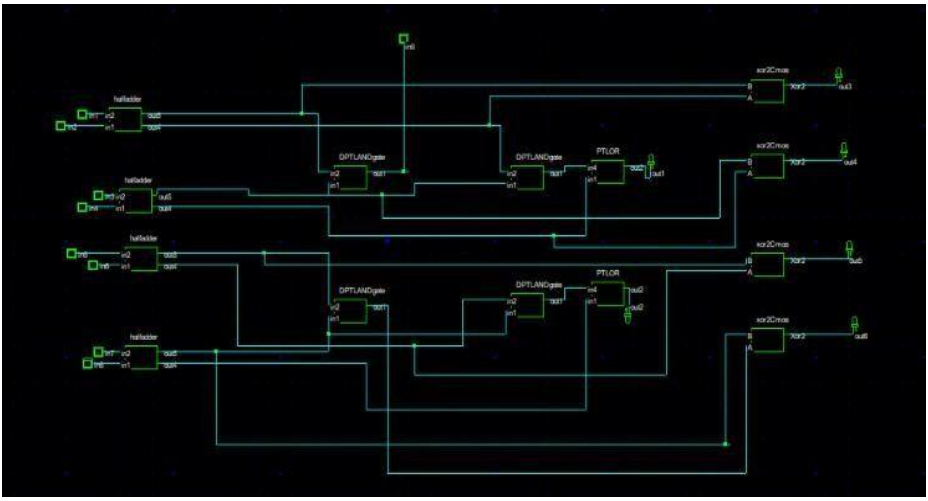

Fig. 5. Schematic of DPTL-Based Parallel Prefix 4-Bit Ladner-Fischer Adder

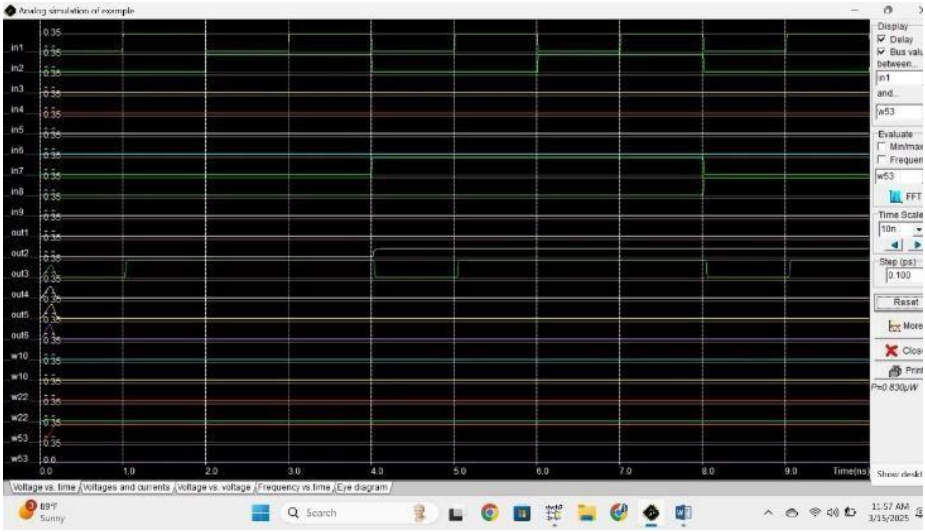

Fig. 6. Transient Simulation Waveform of DPTL- Based 4-Bit Ladner-Fischer Adder

The GDI-based implementation produced the most compact layout, occupying only 166.6 μm², and achieved a power of 0.794 μW. The schematic of GDI-based design anf its transient simulation waveform are displayed in Figs. 7 and 8, respectively.

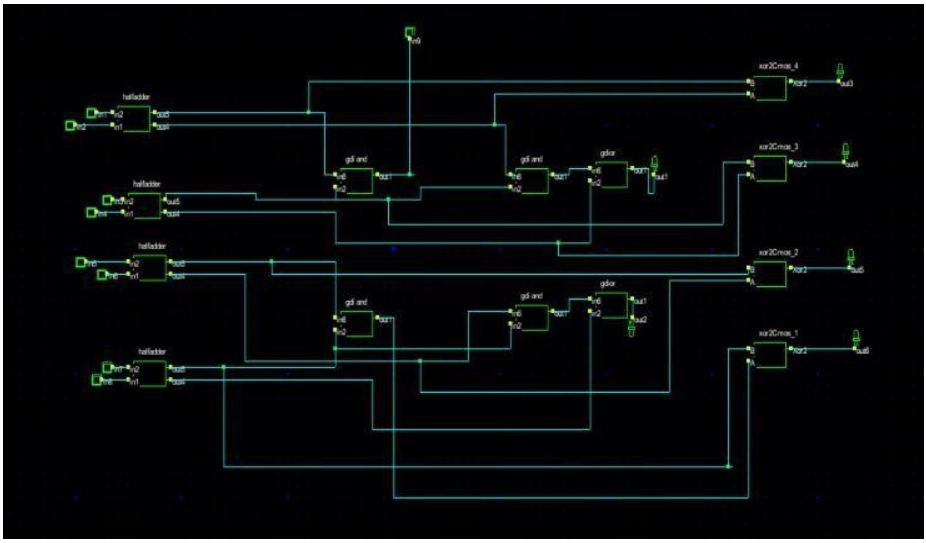

Fig. 7. Schematic of GDI-Based Parallel Prefix 4-Bit Ladner-Fischer

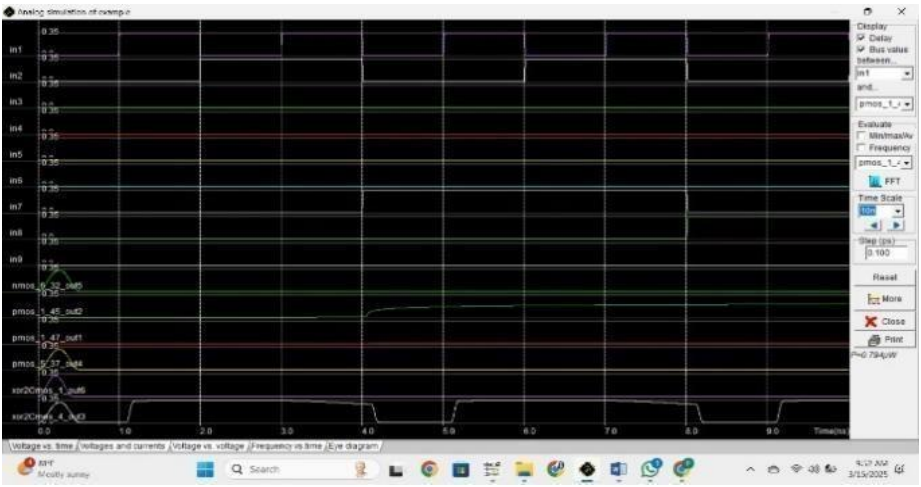

Fig. 8. Transient Simulation Waveform of GDI-Based Parallel Prefix 4-Bit Ladner-Fischer Adder

These observations show a clear trade-off between area and power. DPTL is preferred for power-critical designs, whereas GDI is better suited for area-constrained applications.

A detailed comparison of power and area for all four logic styles—CMOS, PTL, DPTL, and GDI – is summarized in Tabel 1. These observation show a clear trade-off between area and power. DPTL is preferred for power-critical designs, whereas GDI is better suited for area-constrained applications.

The experimental findings validate that non-conventional logic styles can significantly improve arithmetic efficiency compared to traditional CMOS logic.

Table 1. Comparison of CMOS, PTL, DPTL, and GDI implementation

S.NO	Parameters	CMOS	PTL	DPTL	GDI
1.	Power	6.167 µw	3.925 µw	0.830 µw	0.794 µw
2.	Height	8.3 µm	5.5 µm	9.2 µm	5.8 µm
3.	Area(surf)	272.6 µ m²	198.9µm²	370.1µm²	166.6µm²

5 Conclusion

This paper presented the design and analysis of a 4-bit Ladner–Fischer Parallel Prefix Adder (LF-PPA) implemented using four different logic styles—CMOS, Pass Transis- tor Logic (PTL), Double Pass Transistor Logic (DPTL), and Gate Diffusion Input (GDI). The comparative evaluation, performed in terms of power consumption and area utilization, reveals that the GDI-based design achieves the most compact layout, while the DPTL implementation demonstrates the lowest power dissipation.

Each logic style exhibits distinct advantages: DPTL is highly suitable for power-con- strained applications, whereas GDI offers superior area efficiency for compact VLSI systems. The study highlights the practical design trade-offs between energy and area optimization in arithmetic circuits.

Furthermore, scalability analysis indicates that these findings remain consistent for higher-bit adders, such as 8-bit and 16-bit configurations. Future work can focus on extending these techniques to larger architectures, integrating them with emerging low-power design methodologies for high-performance digital systems.

6 References

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