Simulation of Electrical Parameters of MOSFET with Different Gate Dielectric Layers and Substrate Combinations

Zijie Yin

Electronics and Computer Science, Southampton, SO17 1BJ, Southampton, United Kingdom
yzjyzj915@outlook.com

Abstract. In the field of power electronic devices, MOSFET, as a core switching component, is of great significance for improving energy conversion efficiency. Wide bandgap semiconductor substrates (such as SiC and GaN) are taking a dominant position in high-power and high-frequency applications due to their excellent voltage resistance and thermal conductivity. In this paper, the effects of different combinations of gate dielectric layers (HfO_2, Al_2O_3) and substrate materials (Si, SiC, GaN) on the electrical parameters of MOSFETs are investigated by the Sentaurus simulation system. The study adopts the control variable method to comparatively analyze the key performance indexes such as breakdown voltage, on-resistance, threshold voltage, transconductance, cutoff frequency and gate charge. The study reveals the importance of material synergistic optimization for device performance enhancement and provides a theoretical basis for MOSFET design in different application scenarios. In addition, the simulation deviation of the breakdown voltage of GaN devices suggests that the existing model needs to be further improved, and subsequent studies need to be combined with experimental verification to enhance the reliability.

Keywords: Transistor, Wide bandgap material, High-k material, Composite material simulation.

1 Introduction

Integrated circuits are now the hardware foundation of the electronics industry and the information society [1]. Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is the basic device structure of current integrated circuits. As a core component of modern electronic devices, it exists in almost all electronic devices, such as cell phones, computers, automotive electronic systems, etc. Therefore, it is important to study the basic working principle and performance optimization of MOSFETs to improve the performance and reduce the power consumption of electronic devices.

Since MOSFET devices entered mass production, size minimization has been the most important means of performance improvement for integrated circuits [2]. As the feature size of integrated circuits continues to shrink, the traditional gate dielectric layer

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suffers from problems such as leakage current surge due to the quantum tunneling effects, while the limitations of traditional silicon-based materials in terms of mobility and thermal management also constrain devices performance [3, 4]. Adopting the combination of high dielectric constant (high-k) dielectrics (e.g., HfO2) and novel substrate materials (e.g., SiC, GaN) becomes the key path to break through the bottleneck of power consumption and speed.

Currently, the high-k material HfO2 has been widely used in production, and its use as a gate dielectric layer can effectively increase the physical thickness of the gate dielectric layer and reduce the leakage current due to quantum tunneling effect [5, 6]. However, its high density of interfacial states with silicon substrate leads to degradation of mobility; SiC and GaN substrates, as wide-band materials, have the advantages of high breakdown voltage and high temperature resistance, especially GaN, has excellent physical and chemical properties. Recent years, based on the fourth generation of semiconductor manufacturing power electronics and radio frequency electronic devices have sprung up. Representative devices include AlN Insulated Gate Bipolar Transistor (IGBT), AlN Metal Semiconductor Field Effect Transistor and so on. However, the use of wide-band devices is not mature enough, and the price of these devices has no advantage compared with traditional Si substrate devices. The market for the acceptance of new wide-band materials is not high, security and other aspects need to be verified, therefore, it is expected that Si devices will continue to dominate the power electronics market in the coming years [7].

This research aims to systematically analyze the issues of quantum tunneling effect and performance bottleneck of silicon-based materials that MOSFET devices encounter during the continuous miniaturization process of integrated circuits. It explores the potential for enhancing device performance through the collaborative optimization of high-k dielectrics (such as HfO2) and wide bandgap semiconductor materials (such as SiC and GaN). It evaluates key challenges including interface state control, cost-effectiveness, and market adaptability. Furthermore, it provides a theoretical basis for the material selection and structural design of next-generation low-power and high-performance electronic devices.

2 Literature review

2.1 Advances in gate oxide layers of high-k materials

Benefits and challenges of HfO_2. HfO_2 is the mainstream choice to replace SiO_2 due to its high dielectric constant and compatibility with CMOS processes. Kim and his team realized a 2 nm HfO2 gate dielectric by atomic layer deposition to reduce the EOT to below 0.5 nm [8], this demonstrates great potential in terms of integration enhancement of MOSFET. Lee's team found that there is a high density of oxygen vacancy defects at the HfO2/Si interface, which resulted in a degradation of mobility by 30%

[9]. Therefore, although HfO_2 materials can significantly reduce EOT but cause mobility degradation, how to minimize the electron mobility degradation is an important topic for the future of HfO_2 dielectric layer MOSFETs.

Interfacial optimization potential of Al2O3. Compared with HfO2 (k≈25), Al2O3(k ≈9) can control the density of states at the interface with the Si substrate to an order of 1011 eV-1 cm-2 though the dielectric constant is lower [10]. It has been shown that Al2O3 as an interfacial passivation layer (e.g., HfO2/ Al2O3 stacked structure) can significantly suppress the leakage current [11], which provides an idea to enhance the performance of HfO2 dielectric layer.

2.2 Wide-band materials development and challenges

Development of SiC substrate. In the 1970s, single-crystal growth technology for silicon carbide (SiC) was developed, which is an important prerequisite for SiC semiconductor applications. In particular, the advancement of liquid phase epitaxy (LPE) technology has laid the foundation for subsequent device fabrication [12]. Since then, SiC substrate has been widely used in high-voltage MOSFETs by virtue of its wide bandwidth and high breakdown field strength. Smith et al. reported that the on-resistance of SiC-based MOSFETs was 60% lower than that of Si-based devices at 600 V operating conditions [13], but Tanaka et al. found that the presence of a high defect density at the SiO2/SiC interface of the gate dielectric can lead to threshold voltage drift, which affects the device performance [14]. It can be seen that SiC is now widely used, but still has shortcomings under certain conditions.

High frequency advantages and integration challenges of GaN. GaN, also a broadband material, exhibits excellent device performance in radio frequency (RF) applications with two-dimensional electron gas (2DEG) mobility up to 2000 $cm^2/(V \cdot s)$ [15]. However, the interface between GaN and high-k medium is thermally unstable, and high-temperature annealing is prone to trigger interfacial reactions (e.g., Ga-O bond breaking), limiting the device lifetime [16]. In addition, GaN, as one of the new wideband materials, its reliability and long-term stability need to be tested by experiment, application and time. GaN's advantages lie in high frequency, low loss and miniaturization (e.g. fast charging, 5G base station), while SiC is more competitive in high voltage, high power and high temperature scenarios. Competition between the two is more reflected in the application of complementary rather than alternative, with the technology iteration GaN disadvantage may gradually improve, but its differentiation with SiC competition pattern will exist in the future for a long time.

3 Objective

MOSFET is the core component of modern integrated circuits, which can be improved by optimizing the substrate material and gate dielectric layer, and there has been a great deal of progress in the research for single material optimization, but less systematic research on the synergistic effect of the two. This paper focuses on exploring the electrical parameters of different gates and substrates under different gate and substrate material combinations through a simple simulation by the TCAD using the control variable method. This paper aims to explore the electrical parameters under different gate and substrate material combinations by simple simulation using the control variable method with TCAD, and evaluate device performance.

4 Simulation

Considering that the simulation requires a simple MOSFET model and the output parameters are mostly electrical, so the Sentaurus software was chosen for the simulation. The core idea of the simulation is to control the variables and compare the electrical parameters of different combinations by varying the materials of the gate dielectric layer and the substrate for the combinations. Therefore, three devices, Si, SiC and GaN substrate, are modeled in the simulation, and two gate dielectric layers, Al2O3 and HfO2, are set for each device, which have identical parameters except for different substrate materials and gates. The figure illustrates the modeling interface for Si substrate of Sentaurus 2018.

4.1 Basic parameters setting

Considering that SiC and GaN are mainly used for power devices in practical applications and are not used for small MOSFET with high integration, the MOSFET dimensions for the simulation are set to be 1 μm for the substrate, 0.4 μm for the depth, 0.6 μm for the channel length, 10 nm for the thickness of the gate dielectric layer, and 0.8 um for the gate length. In addition, in order to make the simulation consistent with the actual situation, the area factor is set to 1e5 in Sentaurus physics function, which extents 1e5 um in the z-axis direction, to complete the 3D modeling. The 2D interface fig 1 in the X-Y direction is shown below.

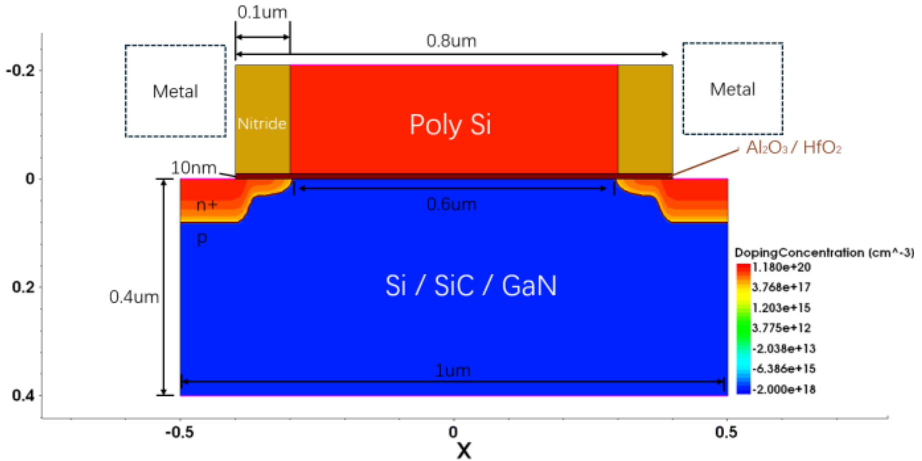

Fig. 1. 2D interface figure in the X-Y direction.

In order to optimize the device structure and make it close to the actual application production, spacer with the thickness of 0.1um is added between the metal and polysilicon to isolate the gate and source-drain region, regulate the parasitic resistance, and optimize the doping distribution and stress. In addition, the model incorporates lightly doped drain (LDD), which serves to reduce the electric field strength near the drain, suppress the hot carrier effect (HCE) and short channel effect (SCE), and enhance the reliability and long-term stability of MOSFETs, which is also a key technology for modern MOSFETs [16][17]. A section is made in the y-axis direction from between the source and drain to show the doping concentration as follow. (Fig.2).

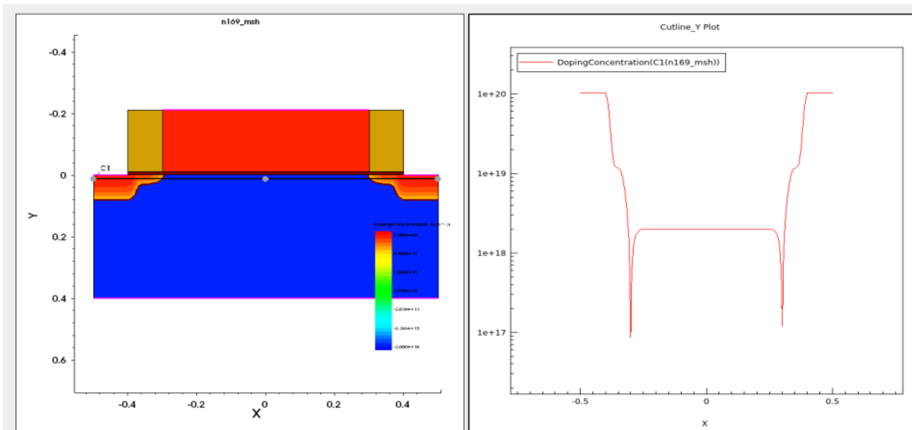

Fig. 2. Doping concentration cross section.

4.2 Simulation result

The simulation explores the voltage withstand capability of the MOSFET by comparing the reverse voltage and drain current curves, explores device saturation current and on-resistance through forward voltage and drain current curves (I-V), explores device threshold voltage (Vth) and transconductance (gm) by gate voltage and drain current curves, explores the device high-frequency signal processing capability by Gate voltage and cutoff frequency (ft) curves, explores device driving power consumption and switching speed by gate charge (Qg) and gate voltage curves. It is hoped that by comparing the above parameters, the performance of the device will be analyzed in the front.

Reverse voltage and drain current curve. The voltage withstand capability of a MOSFET is mainly determined by its drain-source breakdown voltage, a parameter that reflects the maximum voltage that the device can withstand in the off state [18]. Breakdown voltage (BV) can be found by applying a reverse voltage to the device and observing the sudden change in its leakage current. In the simulation of Sentaurus software, there is a significant deviation in the BV prediction of GaN devices, while the simulation results of the same methodology for Si/SiC devices are in good agreement with the experiments. This discrepancy may stem from the unique physical properties of GaN materials and the limitations of existing TCAD models. Therefore, this section only discusses the devices with Si and SiC substrates and the result is shown below. (Fig.3).

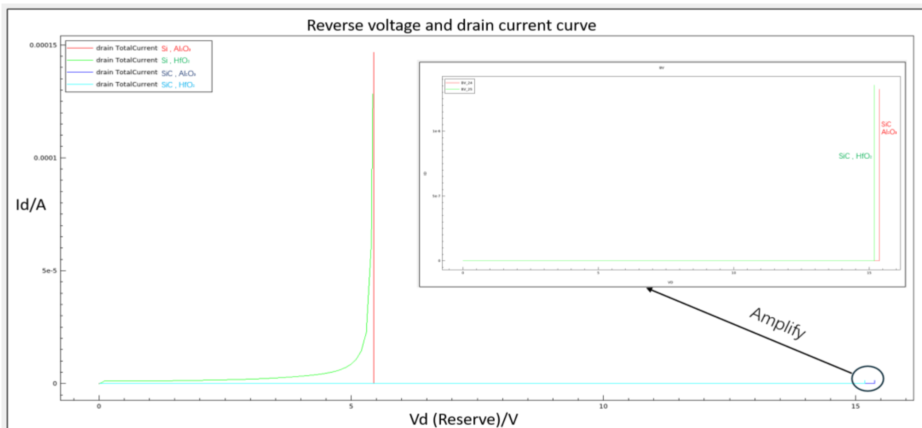

Fig. 3. Break down voltage for Si and SiC device.

It can be seen from the results that no matter what material is used for the gate dielectric layer, the device with SiC substrate has better voltage withstand capability than that with Si substrate, and the device with HfO2 gate dielectric layer combined with Si substrate has leakage current, which can be solved after replacing it with SiC substrate,

which is due to the advantage of wide-bandwidth substrate, Al2O3 gate dielectric layer material exhibits improved withstand capability.

Forward voltage and drain current curve. I-V curve of MOSFET can react to the device's on-resistance, saturation current, and other parameters. The IV curve can assess the performance of the device, and it can be divided into the linear and saturation regions. In the linear region, Vd is small, Id will increase linearly with Vd, through the slope of the device, in linearly can get the on-resistance of the device. When Vd increases to a certain degree, Id will tend to saturation, no longer with the Vd significant change, at this point, the saturation current of the device can be obtained, the on-resistance is obtained by analyzing the image in simulation software, the result is shown in fig 4.

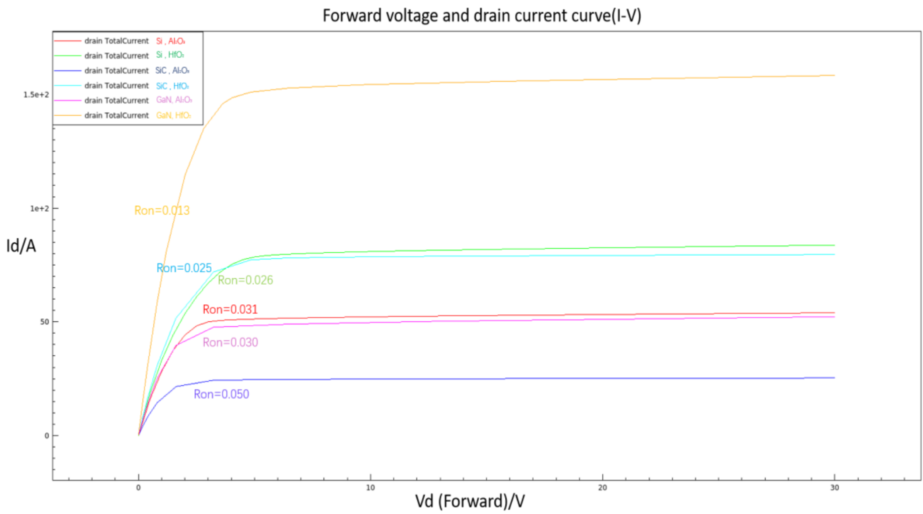

Fig. 4. I-V cure.

From the figure, it can be seen that HfO2 as the dielectric layer possesses higher saturation current, and lower on-resistance, and the substrate material has less influence on these two parameters, in which GaN is used as the substrate and HfO2 as the dielectric layer possesses the smallest on-resistance and the largest saturation current.

Gate voltage and drain current curve. Id-Vg curves provide a good assessment of gate control and switching characteristics of the device. The two parameters, threshold voltage and transconductance, are mainly discussed here, and the simulation results for different combinations are shown as fig 5.

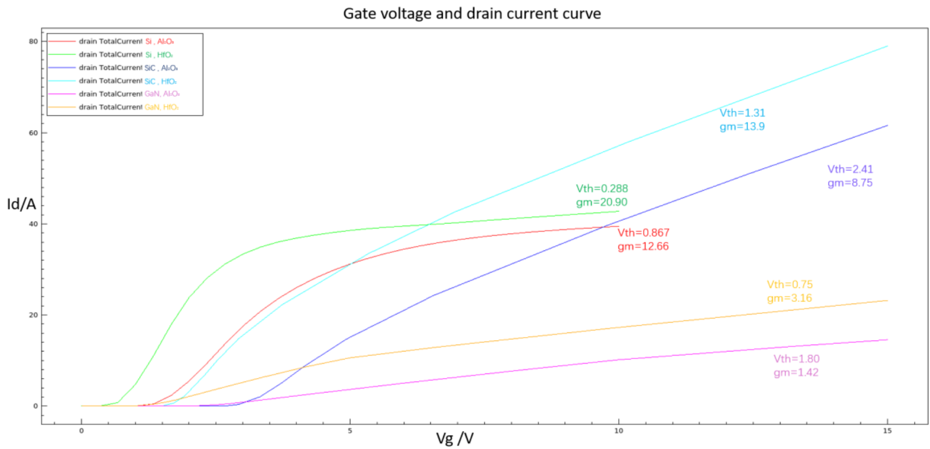

Fig. 5. Gate voltage and drain current curve.

The transconductance is a parameter that measures the ability of the gate voltage to control the drain current [19]. A high transconductance means that a small change in the gate voltage causes a large change in the drain current, which is advantageous for certain applications, such as when an amplifier requires high gain. Low transconductance, on the other hand, possesses high stability and is suitable for applications in anti-jamming scenarios.

From the simulation results, the HfO2 dielectric layer has a smaller threshold voltage compared to Al2O3 and is more suitable for low voltage devices. The effect of the substrate material on the threshold voltage is less compared to the effect of the dielectric layer. Si+ HfO2 has the lowest threshold voltage while SiC+Al2O3 has the highest threshold voltage. From the figure, it can be seen that the GaN device has the smallest transconductance, followed by SiC, then the Si substrate. HfO2 dielectric layer transconductance is higher than that of Al2O3, so the combination of GaN+ Al2O3 achieves the smallest transconductance, while Si+ HfO2 achieves the largest transconductance. In addition, it can be obtained from the simulation results that the linear region of the wide forbidden band material is longer and the saturation current is larger.

Gate voltage and cutoff frequency curve. The cutoff frequency is a parameter that reacts to the high-frequency performance of the transistor, reflecting the device's ability to respond to fast-changing signals; the higher ft is, the stronger the device's ability to amplify and process high-frequency signals [20]. The simulation result is shown as Fig 6.

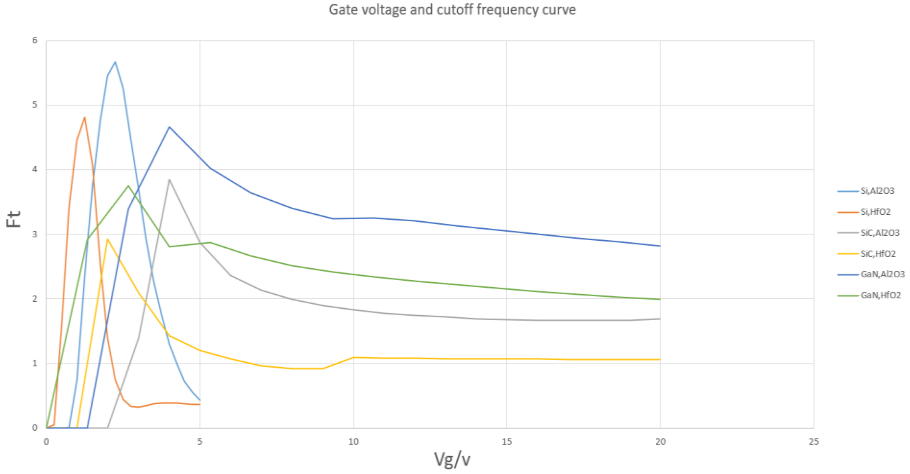

Fig. 6. Gate voltage and cut-off frequency curve.

Through the results, the Si substrate material and Al2O3 gate material have the highest peak cutoff frequency, in addition, the cutoff frequency of the wide-band substrate material varies more gently with the gate voltage, whereas the Si substrate material varies drastically, and the saturation region cutoff frequency is lower than that of the wide-band material.

Gate charge and gate voltage curve. The drive charge of a MOSFET describes the total amount of charge required to charge the gate capacitance of the MOSFET during the switching process, which is a key parameter that affects the switching speed and switching losses of the MOSFET. When driving a MOSFET, the gate capacitor needs to be charged to a certain voltage in order to conduct. This charging process is divided into several stages: first charging to the threshold voltage Vth, forming a conducting channel; then entering the Miller plateau region, where the charging of the gate-drain capacitance dominates, resulting in Vg temporarily remaining constant; and finally continuing to charge to the final drive voltage. The gate charge is measured in Coulombs, the larger the total charge, the longer the capacitor charging time required to turn on the MOSFET and the switching losses will increase, conversely, the smaller the value, the lower the losses, thus realizing high speed switching. The driving charge of the device can be obtained by making a difference between the charges before and after the Miller plateau. The following fig 7 shows the Vg-Q curves obtained by simulation for different gate dielectric layer and substrate combinations.

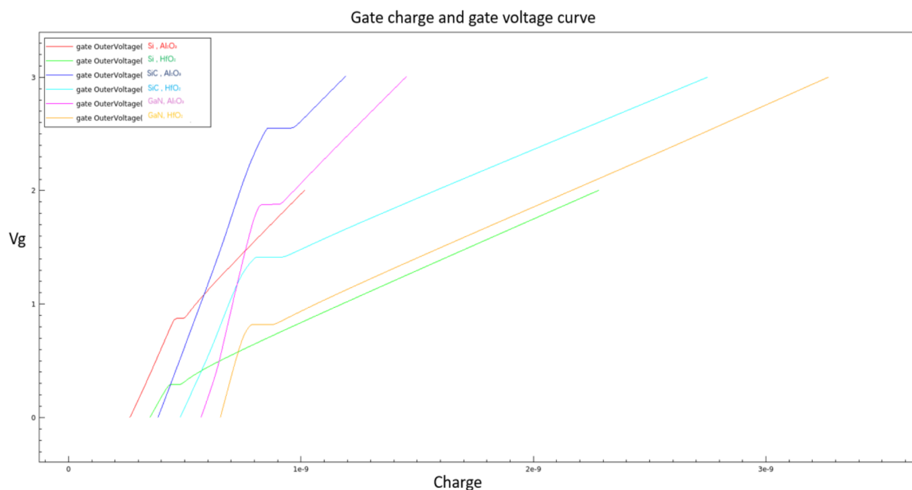

Fig. 7. Gate charge and gate voltage curve.

From the simulation results, the total charge of the wide-band material in conduction is larger than that of the Si substrate, and the effect of the gate material on the conduction charge is not significant.

4.3 Discussion

In this simulation, MOSFETs with Si, SiC, and GaN substrate materials combined with Al2O3 and HfO2 gate dielectric layers were modeled and simulated by Sentaurus 2018 software, it was found that the different materials have their own advantages and disadvantages in the performance of different electrical parameters. There does not exist a combination that is superior to other materials in all aspects. Table 1 shows the possible suitable application scenarios matched to the characteristics of the different combinations.

Table 1. Possible suitable application scenarios matched to the characteristics of the different combinations.

Substrate	Gate dielectric	Advantageous Parameters	Application
Si	Al_2O_3	Low threshold voltage, high transconductance	Low voltage, high gain devices
Si	HfO_2	High cut off frequency, low gate charge	High frequency switches
SiC	Al_2O_3	High break down voltage, low on-resistance	High voltage power devices
SiC	HfO_2	High stability, high temperature resistance	High temperature and reliability scenarios
GaN	Al_2O_3	Low on-resistance, high saturation current	High frequency, high-power applications

Substrate	Gate dielectric	Advantageous Parameters	Application
GaN	HfO_2	Low transconductance, high interference immunity	Stable switching in high noise environment

Therefore, the selection of materials and structures according to different application scenarios is an important idea for the future development of MOSFETs

5 Conclusion

Aiming at the bottleneck of traditional silicon-based MOSFETs in terms of power density and high-frequency performance, this paper integrates the synergistic optimization strategy of high-k gate dielectrics (HfO2/ Al2O3) and wide-bandwidth substrates (SiC/GaN), and validates the differentiated advantages of different combinations in conjunction with the TCAD simulation system: SiC + HfO2 performs excellently in terms of high-voltage withstanding voltage and low on-resistance; GaN + HfO2 is suitable for high-frequency and high-power scenarios; while Si + Al2O3, with its high cut-off frequency and low gate charge characteristics, offers a good opportunity for RF communication and low-frequency MOSFETs. GaN + HfO2 is suitable for high-frequency and high-power scenarios, while Si + Al2O3 provides an optimization path for RF communication and low-power logic circuits by virtue of its high cutoff frequency and low gate charge characteristics. The study provides theoretical support for device performance breakthroughs and scenario-based design from the perspective of material synergy.

In the model about the GaN device breakdown voltage simulation due to the GaN material is relatively new, the relevant data collection is not comprehensive enough, the software for the material model is not perfect, so failed to successfully simulate the collection of data, which led to this part of the study lack of data support, in the follow-up research need to continue to improve.

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