Analysis and Process Optimization of SiC MOSFET High-Temperature Region Characteristic Degradation Based on Silvaco Atlas

Shengxuan Ni [1], Zihao Yuan[2] , Cheng Zhu [3]

[1] School of optoelectronic and Communication Engineering, Xiamen University of technology, Xiamen, Fujian, China
[2] School of Electronic and Information Engineering, Tongji University, Shanghai, China
[3] School of Microelectronics, South China University of Technology, Shenzhen, Guangdong, China
202264681227@mail.scut.edu.cn

Abstract. With the increasing competition in the international semiconductor industry, SiC MOSFET has become a research focal point in the power semiconductor field due to its material advantages as pivotal role. However, its reliability issues under extreme temperature conditions severely hinder practical applications. This study focuses on analysing the characteristic degradation of SiC MOSFETs in high-temperature zones through Silvaco Atlas simulations. For a start, theoretical analysis was conducted to investigate temperature-dependent variations in transistor threshold voltage, carrier mobility, and device leakage current. The subsequent software simulations confirmed the theoretical analysis and provided insights into the failure mechanisms. Finally, a process optimization method of gate oxygen nitrogen annealing (NO) was proposed to address the issue of interface state traps, and its improvement effect was verified through theoretical analysis and comparison with traditional structures. Although the analysis of optimized device characteristics only stays at the theoretical level, this study has preliminarily completed the simulation analysis of the high-temperature characteristics of SiC MOSFET, laying a theoretical foundation for future high reliability power device design and opening up new directions for interface engineering optimization.

Keywords: SiC MOSFET, High-Temperature Electrical Characteristics, Silvaco ATLAS Simulation, High-Temperature Reliability Optimization.

1 Introduction

Contemporary society is undergoing rapid development, with semiconductor technology playing a pivotal role in the electronic power sector. However, the domestic chip industry is encountering substantial challenges due to technological blockades stemming from a tense international landscape. In response, the government is increasing its support for the semiconductor sector to stimulate its growth. Within the current chip

S. Zhang (ed.), *Proceedings of the 2025 International Conference on Electronics, Electrical and Grid Technology (ICEEGT 2025)*, Advances in Engineering Research 292,
https://doi.org/10.2991/978-94-6463-986-5_22

industry, power semiconductor devices are in high demand, primarily due to their efficiency in transmitting and utilizing electrical energy. Among these devices, metal-oxide-semiconductor (MOS) components serve as fundamental elements of modern electronic systems; however, they are vulnerable to reliability degradation under extreme temperature conditions, which poses a substantial barrier to progress in various fields, including aerospace, new energy vehicles, industrial automation, and quantum computing [1]. Presently, commercially available integrated circuit MOSFET devices typically operate within a temperature range of -40 to 125°C, or even more restricted limits. In certain specialized applications, the temperature requirements often exceed these parameters. For example, in the oil exploration industry, devices utilized in monitoring systems must operate for prolonged periods at elevated temperatures of 150°C. Similarly, in aerospace applications, equipment designed for planetary exploration may reach operating temperatures of up to 200°C [2-4]. The International Roadmap for Semiconductors (IRDS) indicates that the electrical characteristics of MOSFETs become unstable at extreme temperatures ranging from -200°C to 300°C. This instability is primarily characterized by threshold voltage drift, reduced mobility, and exacerbated hot carrier injection (HCI) effects, which can lead to a direct reduction in device lifespan by 30% to 70% [5].

It has been observed that extreme temperature conditions negatively impact the electrical performance of conventional MOSFETs. In contrast, silicon carbide (SiC) materials possess a wider bandgap, enhanced breakdown field strength, and superior thermal conductivity compared to traditional silicon materials [6-10]. However, there exists a notable deficiency in reliability research specifically addressing SiC MOSFETs. Consequently, this paper investigates the reliability of SiC MOSFETs by examining their electrical characteristics and lifespan predictions under extreme temperature conditions, while also proposing optimizable structural processes.

This study first analysed the effects that would influence the device characteristics at extreme temperatures. Then, through multi-scale modeling and Silvaco Atlas software simulation, it revealed the performance degradation of SiC MOSFET in extreme temperature environments, analysed their failure mechanisms, and proposed structural optimization schemes for SiC MOSFETs to reduce the impact of temperature on their characteristics.

2 Electrical characteristic analysis on temperature

2.1 Threshold voltageV_{th}

The threshold voltage V_th of a MOSFET refers to the gate voltage at which the device transitions from the cut-off region to the weak inversion region. It is usually defined as the condition where the surface electron concentration is equal to the doping concentration in the body region. Its mathematical expression is:

$$V_{th} = \Phi_{ms} + 2\phi_B + \frac{Q_{ox}+Q_{it}}{C_{ox}} \tag{1}$$

where $\Phi_{ms}$is the difference in work functions between metal and semiconductor; $\phi_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$is the barrier potential of the body region, which is related to the doping concentration and temperature; $Q_{ox}$is the charge of the oxide layer of the body; Q_{it} is the trap charges at the interface, which vary with temperature andC_{ox} is the gate oxide layer capacitance [7].

Due to the large number of interface traps in SiC MOSFETs, when the temperature rises, some traps release electrons, causing the effective threshold voltage to decrease [8]. Under high-temperature conditions, the concentration of thermally excited carriers increases, making the inversion layer easier to form. Moreover, the acceptor impurities in the SiC bulk region are more easily activated, reducing the barrier of the bulk region. All these effects will lead to a decrease as the temperature rises.

Taking all these effects into account, the empirical relationship for the threshold voltage of SiC MOSFET as a function of temperature is

$$V_{th}(T) = V_{th}(T_0) - \alpha(T - T_0) \tag{2}$$

where α is the temperature coefficient of the threshold voltage (typical value is approximately -2 ~ -4 mV/K); T_0 is the reference temperature (usually taken as 300K) and T is the current temperature [7]

2.2 Carrier mobility μ

Ion impurity scattering. At low temperatures, the thermal excitation energy is relatively low, and the carrier kinetic energy is small. During the movement process, it is affected by the Coulomb force in the Coulomb potential field generated by ionized impurities, resulting in scattering. The temperature dependence of impurity scattering mobility is as follows:

$$\mu_{imp} \propto T^{\frac{3}{2}} \tag{3}$$

From the formula (3), it can be seen that as the temperature rises, the mobility increases. This is because high temperature causes the energy of charge carriers to increase, resulting in faster movement. Therefore, they are less likely to be captured by impurities, and the scattering probability decreases. Moreover, at high temperatures, the concentration of charge carriers rises, and the plasma effect intensifies, which shields the Coulomb potential field and reduces the scattering effect [9].

Because impurity scattering gradually intensifies with the increase in doping concentration, this mechanism is particularly evident in high-doped SiC MOSFET

Phonon scattering. Phonon scattering is mainly caused by the vibration of the semiconductor lattice. Thermal-excited phonons interact with charge carriers, causing the trajectories of the charge carriers to deviate and affecting the mobility. Phonon scattering mainly includes acoustic phonon scattering and optical phonon scattering.

As the temperature rises, the lattice atoms undergo local electric field disturbances due to thermal vibration, which affect the movement of charge carriers and lead to acoustic phonon scattering. The mechanism of optical phonon scattering is that at high temperatures, the high-energy optical phonons of SiC material are excited and strongly interact with the charge carriers, resulting in a decrease in mobility. Optical phonons have a relatively high energy threshold (the energy of optical phonons in SiC is approximately 100 meV), so their influence is mainly in the high-temperature region. The temperature dependence of the phonon scattering mobility is as follows:

$$\mu_{ph} \propto T^{-m}, \quad m \approx 2.2 - 2.5 \tag{4}$$

From the formula (4), it can be known that due to the increase in the number of phonons excited by heat at high temperatures, scattering is enhanced, and the mobility decreases as the temperature rises. SiC materials have a higher optical phonon energy, so the rate of their mobility decrease at high temperatures is slower than that of traditional silicon materials. And high doping will affect the phonon shielding effect, resulting in a weakened influence of optical phonon scattering ［10］

Total migration rate model. In SiC MOSFETs, the carrier mobility μ is influenced by multiple scattering mechanisms, and the scattering processes follow the Matthiessen rule:

$$\frac{1}{\mu} = \frac{1}{\mu_{imp}} + \frac{1}{\mu_{ph}} \tag{5}$$

where μ_{imp} is the mobility dominated by impurity scattering and μ_{ph} is the mobility dominated by phonon scattering ［7］.

At low temperatures (less than 150K), impurity scattering dominates and the mobility increases with the rise in temperature; at moderate temperatures (150K - 300K), both compete, but acoustic phonon scattering gradually strengthens; at high temperatures (greater than 300K), phonon scattering completely dominates and the mobility decreases sharply with the increase in temperature.

2.3 Leakage current I_{Leak}

Due to its wide bandgap property（Eg≈3.26eV for 4H-SiC）, SiC MOSFET exhibits superior electrical performance in high-temperature environments. However, its leakage current still significantly increases with the rise in temperature. The main influencing factors include the thermal excitation of intrinsic carrier concentration, the leakage current caused by interface trap states, the Poole-Frenkel effect, and the parasitic BJT effect.

Phonon scattering

Ion impurity scattering. Under high-temperature conditions, the intrinsic carrier concentration ni increases exponentially with temperature, causing the leakage current to rise rapidly. This effect is particularly pronounced when the temperature exceeds 250°C.

$$n_i = N_c N_v \exp\left(-\frac{E_g}{2kT}\right), \quad I_{leak} \propto n_i^2 \tag{6}$$

where N_c and $N_v$represent the effective state densities of the conduction band and the valence band, and they change relatively little with temperature; k is the Boltzmann constant and E_g is the band gap of SiC (3.26 eV, which has a lower leakage current compared to Si's 1.12 eV)

Interface state traps and Poole-Frenkel effect. Since SiC MOSFET has an oxide-semiconductor interface, and the trap density at the SiO_2/SiC interface is relatively high (with Dit reaching 1012cm-2)，at high temperatures, the trap-state charges are easily released by thermal excitation. The thermal-excitation carriers may be released through the interface states and enter the drain, resulting in an increase in leakage current. This mechanism is dominated by the Poole-Frenkel effect.

The Poole-Frenkel effect is a trap-assisted conduction mechanism, which describes the phenomenon where, under the influence of an electric field, charge carriers are released from traps (such as lattice defects, interface states), thereby increasing the leakage current. Its physical essence is that the applied electric field lowers the potential barrier for electrons to transition from the trap state to the conduction band, making it easier for the carriers to pass through the insulating layer or semiconductor material [11]. The current density (J) is usually given by the following exponential relationship:

$$J \propto \exp\left(-\frac{q(\Phi_B - \beta\sqrt{E})}{kT}\right) \tag{7}$$

where q is electric charge; Φ_B is the trap state ionization energy (barrier height); k is the Boltzmann constant; T is absolute temperature; E is the additional electric field strength; and β is the Poole-Frenkel coefficient, defined as:

$$\beta = \sqrt{\frac{q^3}{\pi \epsilon_r \epsilon_0}} \tag{8}$$

where ϵ_r is the dielectric constant and ϵ_0 is the vacuum dielectric constant [12].

Parasitic BJT effect. Under high-temperature conditions, the number of thermally excited carriers in the drift region of SiC MOSFET significantly increases, and the parasitic BJT (Bipolar Junction Transistor) is activated. The thermally induced process enhances the injection of minority carriers (holes) in the P-body region, making the parasitic BJT easier to conduct, resulting in a sharp increase in leakage current. When the temperature is below 150°C, the influence of the parasitic BJT is relatively small; when the temperature is above 200°C, the parasitic BJT conducts, the leakage current increases sharply, and even causes the device to fail [13].

$$I_{leak} \propto \frac{n_i^2}{N_D} \tag{9}$$

3 Construction of the simulation model

This study utilizes the Silvaco Atlas simulation platform to model and analyze the electrical characteristics of 4H-SiC MOSFET devices. The extraction of threshold voltage and saturation drain current values is achieved through a systematic approach that includes mesh division, material specification, doping distribution, and the selection of appropriate physical models.

3.1 Definition of mesh

The division of the mesh serves as a critical foundation for device simulation, significantly influencing both computational accuracy and efficiency. In this simulation, a non-uniform mesh division strategy is employed, with particular emphasis on refining the mesh in the gate region (X direction: 0.05 μm) and the interface region (Y direction: 0.05 μm). This refinement enhances the resolution of the channel electric field and carrier transport. In contrast, other regions are assigned medium or sparse mesh configurations to optimize computational efficiency.

3.2 Material and regional definition

The specification of material parameters is crucial in determining the characteristics of the simulated device. The primary region is composed of 4H-SiC material, characterized by a bandwidth of 3.26 eV. This property is essential for calculating the intrinsic carrier concentration at elevated temperatures. The dielectric constant of 4H-SiC is set at 9.7, which influences the capacitance characteristics of the device and its gate control capabilities. The gate oxide layer is constituted of SiO_2, which has a bandwidth of 9.0 eV. The SiO_2 layer is distinctly defined in the region where $y \leqslant 0$, utilizing the region command to isolate it and mitigate numerical oscillations at the SiC/SiO_2 interface.

3.3 Electrode and doping configuration

In defining the electrodes, the gate is constructed from polysilicon (PolySi) and must adequately cover the channel region (x = 2.3 - 2.5 μm) to ensure precise alignment, accounting for potential errors in photolithography. The source and drain electrodes are composed of nickel silicide (NiSi), with the source extending to x = 2 μ m to encompass the entire n^+ source region, thereby mitigating the risk of current crowding phenomena.

Regarding the doping configuration, it is crucial to maintain a p-type base region doping concentration that is sufficiently high to ensure effective channel control while simultaneously preventing an excessively elevated threshold voltage. The peak concentration within the n^+ source region should attain a specific threshold to minimize contact resistance and facilitate the formation of ohmic contact with the NiSi electrode.

3.4 Physical model and solution settings

In the selection of the physical model, careful consideration must be given to temperature settings, as subsequent simulations will depend on electrical characteristic curves obtained at various temperatures. Furthermore, the implementation of a carrier velocity saturation model (CVT) is essential for accurately simulating the characteristics within the saturation region.

For the solution methodology, this study adopts the Newton method in conjunction with a trap model, which incorporates automatic step size control (autonr) to enhance convergence efficiency.

4 Analysis of simulation results

4.1 Simulation outcomes of conventional SiC MOSFET

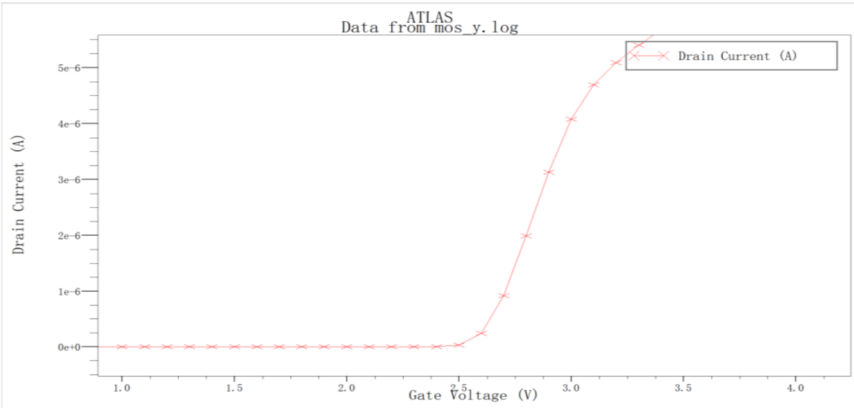

Fig. 1. Threshold Voltage Characteristics of MOSFET at 300K.

Figure 1 illustrates the threshold voltage characteristic curve of silicon carbide (SiC) MOSFETs at a temperature of 300 K. In this experiment, the gate and drain terminals are interconnected to ensure that the MOSFET operates within the saturation region. The drain voltage (V_D) is incrementally increased from 0.01 V to 5 V while maintaining a constant temperature of 300 K. Analysis of Figure 1 reveals that the drain current initiates at a voltage of 2.5 V, which is identified as the threshold voltage. The operational characteristics of the MOSFET are influenced by the presence of the metal-oxide-semiconductor (MOS) structure located in the upper region of the device. In particular, within the P-type region situated beneath this structure, holes serve as the majority carriers, whereas electrons function as minority carriers. The establishment of a conductive channel is predominantly dependent on the migration behavior of electrons. Upon the application of an external bias voltage to the drain, the MOSFET transmits the electric field effect to the surface region of the P-type material. This process is facilitated by the positive potential, which promotes the accumulation of electrons at the interface.

As the drain-source voltage increases, this accumulation effect becomes more pronounced. Once the drain-source voltage surpasses the critical threshold voltage, a conductive electron channel is formed at the surface, thereby enabling the conduction mechanism and resulting in a significant increase in drain current.

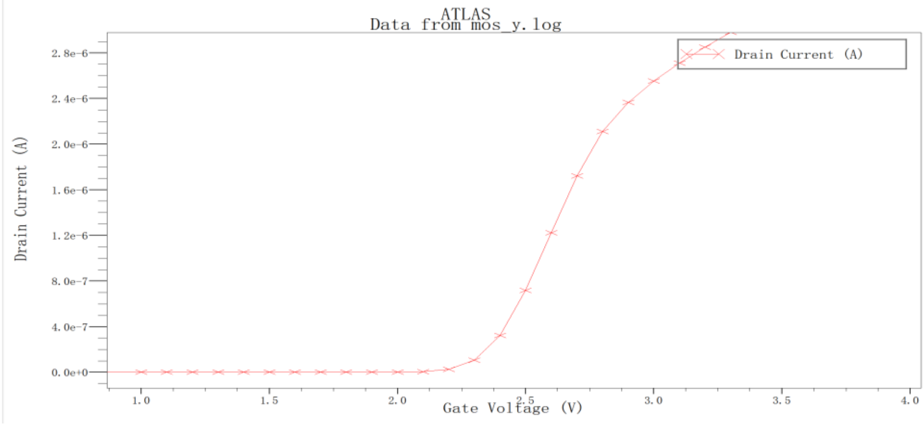

Fig. 2. Threshold Voltage Characteristics of MOSFET at 500K.

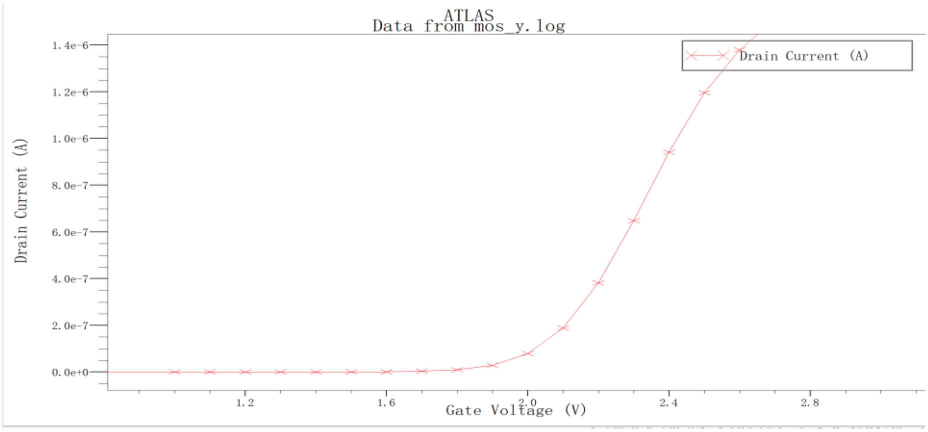

Fig. 3. Threshold Voltage Characteristics of MOSFET at 700K.

Figure 2 illustrates the threshold voltage characteristic curve of the SiC MOSFET at a temperature of 500 K, while Figure 3 presents the corresponding characteristic curve at 700 K. A comparative analysis reveals a decline in the threshold voltage from 2.5 V to approximately 2.0 V, and subsequently to 1.6 V. This observation leads to the conclusion that the threshold voltage exhibits a decreasing trend as the temperature increases.

4.2 Analysis of failure mechanism

Hot carrier injection. Under high-temperature and high-electric-field conditions (especially when the VDS is high and the gate voltage bias remains for a long time), the charge carriers (primarily electrons) in the channel region acquire high energy. At the position close to the gate contact area, "shock ionization" or impact on the oxide layer occurs, which may lead to ionization or decomposition within the oxide layer, causing electron injection. Some high-energy electrons may be injected into the gate oxide layer, forming fixed charges or interface traps [14].

Over time, these traps accumulate, leading to a shift in the threshold voltage of the device, and even causing an increase in the gate leakage current Ig, a decrease in Ids in the output characteristics, and a deterioration in the switching capability of the MOSFET. After long-term operation, the driving voltage window becomes smaller, affecting logic recognition, increasing the rate of oxide layer degradation, and reducing reliability. HCL is one of the main starting points for the failure of gate oxide at high temperatures.

Interface state and trap enhancement. The SiC/SiO_2 interface itself has a relatively high defect density. As the temperature rises, the originally "frozen" or unactivated interface traps (D_{it}) are thermally activated. These trap states can capture and release charge carriers. At high temperatures, the generation of interface traps intensifies, enhancing the exchange effect with channel electrons, interfering with the formation and maintenance of the inversion layer, and affecting the static and dynamic characteristics of the device [15].

As the number of interface traps increases, the threshold voltage Vth becomes unstable, and its drift often intensifies with the increase in operating temperature, increasing sub-threshold current. The increase in these traps leads to logic errors, level abnormalities, or misoperation at high temperatures, affecting the switching characteristics of the device and reducing the voltage stability and reliability of the system.

Oxide layer degradation and increase in tunnel current. High temperature will accelerate the degradation of the oxide layer, reducing the structural stability within the gate oxide layer. The generation and recombination rates of electron-hole pairs in SiO_2 become unbalanced, leading to an increase in conductivity. The atomic vibrations within the gate oxide layer intensify, resulting in an increase in defects and microcracks in the oxide layer. Eventually, this causes the thinning of the oxide layer or "breakdown", forming an electrical conduction channel and inducing tunnel current. The Fowler-Nordheim tunneling effect is enhanced [16].

As the gate oxide layer deteriorates, the gate leakage current significantly increases, and leakage jumps occur within a small voltage range (possibly indicating the initial sign of oxide breakdown simulation), which may lead to gate failure. The degradation of the gate oxide layer also affects the switching speed of the device, making the MOSFET unreliable and reducing the device's withstand voltage capability.

Thermal generation enhancement. Under high-temperature conditions, the carrier density of semiconductor materials increases, especially the thermally excited carriers. In SiC MOSFETs, high temperatures accelerate the generation of electron-hole pairs and enable these carriers to generate a larger current at a lower bias voltage, resulting in more minority carriers in areas outside the inversion channel (such as the junction region and the bulk region), thereby affecting the leakage current and breakdown mechanism of the device [17].

The simulation results under high-temperature conditions usually show a significant increase in leakage current, especially in the sub-threshold region. The increase in leakage current directly leads to an increase in the power consumption of the device, which affects the energy efficiency of the system. The increase in leakage current at high temperatures can also cause thermal runaway, especially under high current density, further exacerbating the degradation of the device.

5 Construction of the simulation model

According to the previous theoretical analysis of the degradation of the electrical characteristics of SiC MOSFET under high temperature conditions, it can be found that there are too many reasons for the degradation, and only one of them is specifically analyzed and optimized in this article.

Due to the presence of C element in SiC material, there is a large amount of 4H-SiC/Si interface in SiC MOSFET, which is about 2-3 orders of magnitude higher than that in Si MOSFET [18], leading to undesirable results in terms of mobility and reliability. All current commercial SiC MOSFET suffers from significant threshold voltage instability, which is caused by traps near the gate 4H-SiC/SiO2 interface and is manifested by threshold voltage degradation with prolonged voltage stress at high temperatures. When a positive voltage stress is applied, the threshold voltage positively drifts, resulting in a larger chip conduction loss. And when a negative voltage stress is applied, the chip threshold voltage decreases, which can easily cause the chip to turn on incorrectly, and in severe cases, the chip will be normally open [19].

In order to solve the threshold voltage instability caused by traps near the gate 4H-SiC/SiO2 interface at high temperatures, the method of gate oxygen-nitrogen annealing (NO) is introduced here.

The NO annealing process plays a key regulatory role in optimizing the carrier transport characteristics in the channel region of semiconductor devices.The mechanism originates from the decomposition of NO at high temperatures during thermal processing. The decomposition product, nitrogen (N), diffuses and penetrates into the gate oxide interface region, which effectively passivates silicon dangling bonds (Si–). The thermally activated process promotes the decomposition of residual carbon (C) clusters, leading to the formation of a new, more chemically stable bonding structure (Si–). However, it is crucial to control the annealing time and temperature during this process[20].

Based on the correlation analysis of thermal annealing process parameters and interfacial properties, as well as based on theoretical data, the effect that can be achieved by gate oxygen and nitrogen annealing is that the interfacial density of states shows a trend of attenuation when the heat treatment temperature is rising in a gradient, and the synchronous channel-induced carrier mobility shows a positive trend of enhancement to alleviate the electrical degradation under high-temperature conditions.

6 Construction of the simulation model

This study conducted simulation analysis on the electrical characteristics of SiC MOSFET under high temperature conditions based on Silvaco Atlas, focusing on the influence of temperature rise on key parameters such as threshold voltage, and modeling the mechanism by combining hot carrier effect and thermal excitation effect. The results show that high temperatures significantly degrade accelerator components.

To improve high-temperature performance, a gate oxygen nitrogen annealing (NO) process was proposed and simulated. Theoretical analysis shows that this process can effectively reduce the interface state density, suppress hot carrier injection, and improve indicators such as leakage current and reliability.

However, this study still has certain limitations, such as only simulating changes in threshold voltage, lacking a comprehensive analysis of more electrical characteristics such as leakage current and drain current, and the verification of optimization effects still remains at the theoretical level. In addition, the simulation uses a two-dimensional model that does not fully consider non ideal factors and complex material properties in actual processes, which may result in differences from reality.

In the future, research will further expand the scope of electrical parameter analysis, improve model accuracy, introduce three-dimensional structure and electric thermal coupling simulation, and enhance the engineering applicability of simulation results. At the same time, more interface optimization solutions will be explored, such as fluorination treatment, ONO process, and introduction of high - k media, and combined with experimental methods to verify the simulation conclusions, providing stronger support for high-temperature reliability design.

Authors Contribution. All the authors contributed equally and their names were listed in alphabetical order.

References

1. IRDS, International Roadmap for Devices and Systems (IEEE, 2022)
2. D. M. Ke, J. N. Chen, Principles and Implementation of High-Temperature CMOS Integrated Circuits, Univ. Sci. Technol. China Press, Hefei, (2000)
3. D. M. Ke, Q. Y. Tong, High-temperature microelectronics-Part I: Research on high-temperature characteristics of silicon devices. Microelectronics 3 (1990)
4. D. M. Ke, Q. Y. Tong, High-temperature microelectronics-Part II: Research on high-temperature characteristics of silicon integrated circuits. Microelectronics 4 (1990)
5. L. M. Zheng, X. F. Wang, Reliability analysis of power MOSFETs under extreme temperatures. IEEE Trans. Electron Devices 68(5), 2101-2108 (2021)

6. J. Millan et al., A survey of wide bandgap power semiconductor devices. IEEE Trans. Power Electron. 29(5), 2155-2163 (2013)
7. S. M. Sze, K. K. Ng, Physics of Semiconductor Devices, 3rd ed. (Wiley, 2007), pp. 320-325
8. J. B. Baliga, Fundamentals of Power Semiconductor Devices (Springer, 2008), pp. 420-430
9. M. S. Shur, Low-temperature electronic transport in semiconductors. J. Appl. Phys. 54(1), 1-13 (1983)
10. T. P. Chow, S. H. Kim, Electrical and thermal performance of SiC power MOSFETs. IEEE Trans. Electron Devices 57(1), 70-76 (2010)
11. J. Frenkel, On pre-breakdown phenomena in insulators and electronic semiconductors. Phys. Rev. 54(8), 647-648 (1938)
12. D. A. Neamen, Semiconductor Physics and Devices, 4th ed. (McGraw-Hill, 2012), pp. 315-320
13. K. J. Neuhour, K. Shenai, Analysis of parasitic BJT latch-up in SiC MOSFETs. In: Proc. IEEE ISDRS, 1-4 (2016)
14. H. Tsuno et al., Hot-carrier-induced degradation in 4H-SiC nMOSFETs under high-temperature operation. IEEE Trans. Electron Devices 64(11), 4568-4573 (2017)
15. Z. Cheng et al., Temperature dependence of interface state density and mobility in 4H-SiC MOSFETs. IEEE Trans. Electron Devices 61(5), 1213-1218 (2014)
16. K. Fukuda et al., Reliability of gate oxides for SiC power MOSFETs and its improvement with nitridation. IEEE Trans. Electron Devices 60(2), 561-567 (2013)
17. B. J. Baliga, Silicon Carbide Power Devices (World Scientific, 2005), Chap. 6.
18. P. Fiorenza et al., Temperature-dependent Fowler-Nordheim electron barrier height in SiO_2/4H-SiC MOSFET capacitors. Mater. Sci. Semicond. Process. 11, 24-28 (2017)
19. T. Kimoto, Defect engineering in SiC technology for high-voltage power devices. Appl. Phys. Express 13, 120101 (2020)
20. H. Li et al., Interfacial characteristics of N_2O and NO nitrided SiO_2 grown on SiC by rapid thermal processing. Appl. Phys. Lett. 70(15), 2028-2030 (1997)