Silicon Carbide MOSFET Short-Circuit Protection Strategies

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Abstract. Silicon carbide metal-oxide-semiconductor field-effect transistors, or SiC MOSFETs, have been widely used in high-voltage, high-temperature, and high-frequency power electronic applications due to their superior properties, which include low power loss, high switching frequency, and excellent thermal conductivity. However, compared to conventional silicon-based components, SiC MOSFETs have a substantially shorter short-circuit sustain time. The devices' dependability is also gravely threatened by the increased electrothermal stress they experience during short circuits, which can result in irreparable damage like gate-source or drain-source short circuits. This paper provides a systematic review of the research advancements in short-circuit protection technologies for SiC MOSFETs: clarify the types and failure mechanisms of short-circuit faults; compare the detection methods based on V_{DS}、$dvDS/dt$、I_D 、diD/dt、I_G. This paper provides references for the practical application and subsequent research of short-circuit protection technology for SiC MOSFETs. This comprehensive analysis not only enhances the understanding of failure dynamics but also guides the design of more robust protection circuits, thereby improving the reliability and longevity of SiC-based power systems.

Keywords: SiC MOSFET, Short-circuit protection technology, Fault detection.

1 Introduction

Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistors (SiC MOSFETs), as representative devices of the third-generation wide-bandgap semiconductors, have gained extensive application in power electronic conversion equipment due to their remarkable properties, which include high operating frequency, superior thermal conductivity, low switching and conduction losses, and high breakdown field strength [1]. When contrasted with conventional silicon counterparts, these advanced semiconductor devices demonstrate enhanced suitability for deployment in environments demanding elevated voltage tolerance, extreme thermal conditions, high-frequency operation, and stringent reliability requirements [2]. The strategic implementation of these devices contributes significantly to improving energy conversion performance, increasing power handling capacity per unit volume, and strengthening operational reliability in modern electronic systems [3]. For instance, in the field of electric

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vehicles, SiC MOSFET devices can reduce power consumption during driving, increase charging speed and efficiency, and decrease the size and weight of converters [4][5].

Although SiC MOSFETs have many advantages, these advantages also determine that their short-circuit withstand time is significantly shorter than that of traditional silicon-based power devices [6]. The short-circuit withstand time of current commercial SiC MOSFETs is as low as 2 μs [7], whereas that of alternative Si IGBTs typically exceeds 10 μs [2]. The reduced chip area and increased current density of SiC MOSFETs result in their exposure to more intense electrothermal stress under short-circuit conditions.

Temperature-sensitive parameters including carrier mobility and threshold voltage undergo significant variations during fault events. Rapid thermal escalation at the junction during short circuits induces characteristic degradation that accelerates device failure. Experimental data confirms an inverse relationship between operational parameters (ambient temperature, gate drive voltage, and DC link voltage) and fault tolerance duration [8]. Consequently, protection mechanisms necessitate sub-microsecond response capabilities to ensure system reliability.

Short-circuit faults are one of the important reasons for the failure of SiC MOSFETs, seriously hindering their application. The loop current quickly increases to a level significantly higher than the rated value during a short circuit, ruining the device severely. Even if the electronic device is speedily protected and shut off, its reliability may still be considerably reduced as its electrical characteristics may deteriorate dramatically. Furthermore, SiC MOSFETs have a relatively thin gate oxide layer, which increases their vulnerability to dielectric breakdown and performance worsening in the event of a short circuit [9].

Consequently, developing high-performance protection circuitry capable of rapid fault detection and precise current interruption has emerged as an essential technological prerequisite for ensuring secure operation and facilitating broader adoption of SiC MOSFET-based power systems.

Considering the issues mentioned above, numerous researchers have been committed to enhancing SiC MOSFETs' short-circuit protection technology. They have studied short-circuit fault types, failure modes, detection methods, protection strategies, etc. This article analyzes different types of faults and the failure mechanisms that generate them, compares and evaluates various detection techniques, and discusses the benefits and drawbacks of each. It also summarizes and evaluates the state of development of short-circuit protection technology. This offers a guide for choosing techniques in real-world application situations and for technical improvements in further study.

2 Short circuit fault

2.1 Types of faults

Based on the working state of the device at the time of the short circuit, the short circuit faults of SiC MOSFET can be mainly classified into two types: Hard Switching Fault (HSF) and Fault Under Load (FUL). HSF describes scenarios where a pre-existing short-circuit path activates simultaneously with device switching. In such cases, the MOSFET's drain terminal becomes effectively bridged to the busbar potential. Upon activation, the drain-source voltage rapidly escalates to match busbar levels while the conduction current initiates from zero before surging beyond operational limits. FUL is the term used to describe the circumstance in which a short circuit defect on the load side happens during a SiC MOSFET device's typical conduction operation. The conduction current quickly climbs from the load current value to the maximum short-circuit current value, and the drain-source voltage value quickly rises from the conduction voltage drop to the bus voltage. In addition, there are some other types of faults, such as Fault in Freewheeling Mode (FWM), where the SiC MOSFET device turns on and short-circuits during the forward conduction of the diode in parallel with it [10]. Different researchers sometimes adopt different classification methods for short-circuit faults, but the two types of faults, HSF and FUL, have been widely accepted as an important basis for analyzing short-circuit characteristics and designing short-circuit protection.

2.2 Failure mode

Excessive short-circuit current and voltage can result in irreversible damage to SiC MOSFET devices during a short-circuit fault, which can lead to certain typical failure modes. These failure modes do not represent independent fault categories, but rather constitute specific manifestations of device degradation. Typical failure modes predominantly include gate-source short circuit (G-S short) and drain-source short circuit (D-S short, also referred to as thermal runaway failure). The above two failure modes are respectively also known as fail-to-open (FTO) and fail-to-short (FTS).

When the first failure mode occurs, the gate and source are permanently short-circuited, and the device is locked in the off state, which can prevent system-level damage [11]. This type of failure is seen to be a relatively safe occurrence. The cause of the G-S short is usually due to the thermal mechanical stress resulting from the high-temperature changes during the short-circuit process, as well as the different coefficients of thermal expansion of the polysilicon gate, silicon carbide, the gate-source insulator, and the source metallization layer [12]. High-temperature thermal stress causes the aluminum source metal to melt and seep into the cracks of the gate oxide layer [13], progressively elevating leakage currents until dielectric breakdown initiates a low-resistance conduction path [14], resulting in a short circuit. Increasing the gate oxide thickness helps to avoid short circuit failures related to the breakdown of the gate oxide layer, significantly improving the short-circuit tolerance [15].

The second failure mode is an uncontrollable failure phenomenon. When it occurs, the device is completely out of control, often accompanied by burning or explosion, which poses a threat to the safety of the system. The occurrence of thermal runaway failure is an electrothermal positive feedback process. During short-circuit conditions, the SiC MOSFET experiences rapid temperature escalation, which amplifies charge carrier excitation and precipitates exponential leakage current growth. Extra power is consumed, and the junction temperature rises further. This excessive energy dissipation drives further temperature elevation, activating the parasitic bipolar transistor (BJT) and establishing an unregulated current pathway. The formation of electrothermal positive feedback may cause the threshold voltage to become negative, and the channel may also conduct under negative gate-off voltage. The leakage current remains high and cannot be normally turned off [8][14]. Devices that have undergone thermal runaway failure may exhibit significant degradation in electrical characteristics and a substantial reduction in reliability, even if they are promptly shut down and recover from the short-circuit condition.

The main influencing factor of the failure mode during the device conduction is the bus voltage. The higher the bus voltage is, the more likely the thermal runaway failure will occur [15]. Under low bus voltage conditions, enlarged drive voltage may induce failure mode transitions from gate-source circuit failures to thermal runaway failure. Extended short-circuit exposure durations have been empirically shown to proportionally elevate thermal runaway risks [8]. Overall, large short-circuit energy corresponds to thermal runaway failure, while small short-circuit energy corresponds to gate-source failure. The specific energy size division still needs further research.

3 Short-circuit Detection Technology

3.1 Based on V_{DS}, dv_{DS}/dt

Desaturation protection originates from a protection method for IGBT devices. During short-circuit events, the collector current experiences rapid escalation until reaching saturation. The operating point of the device exits the saturation region and moves to the active region, and the collector-emitter voltage rises significantly. Therefore, the occurrence of a short circuit fault can be indirectly determined based on the change in the collector-emitter voltage. Due to the similarity in characteristics between SiC MOSFETs and IGBTs, the desaturation protection method for IGBTs can be analogized to design a desaturation protection method for SiC MOSFETs. Common desaturation protection circuits can be classified into voltage source type and current source type. The principles of the two are similar, but the structure of the former (as shown in Fig. 1.) is simpler [14][16]. The design of the voltage divider resistors and the comparator threshold voltage ensures that the threshold voltage consistently remains below the divided voltage under normal operating conditions. When a short circuit occurs, the voltage on both sides of the device under test rises sharply. The diode connected to the drain turns off in reverse direction, and Vdesat exceeds the threshold, triggering the protection action. The MOSFET device at the lower right in the figure needs to be controlled in coordination with the device under test (DUT). When the DUT is off, this MOSFET conducts to discharge; when the DUT is on, this MOSFET is off. It should be mentioned that the blanking time between the occurrence of a short circuit and the voltage surpassing the threshold and activating the comparator must be considered in this protection method. The device's normal turn-on will likewise be turned off if the blanking time is not configured to be longer than the protected device's turn-on time. However, the early state of this system was quite awkward because the common SiC

MOSFET components' turn-on time and short-circuit withstand time are both in the microsecond range.

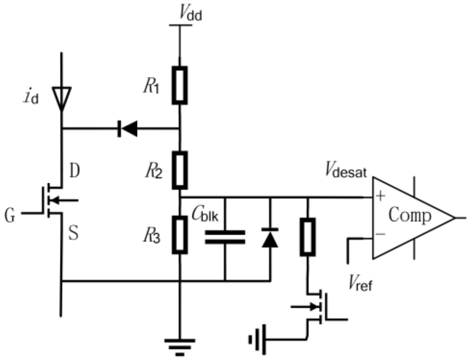

Fig. 1. Voltage Source Type Desaturation Protection Circuit [17].

Li et al. proposed a fast short-circuit detection method based on the swing of the drain-source voltage [10]. They utilized the existing RC buffer circuit to suppress high-frequency oscillations and voltage spikes. By combining a negative peak detector and a reset MOSFET, the maximum voltage drop Vdip on Rs was obtained throughout the entire switching transient of the device. Vdip is proportional to dvDS/dt, and it becomes negative when the drain-source voltage drops. The high-speed comparator is utilized to perform a comparison with the threshold voltage. The scheme does not require additional blanking time and has a negative temperature coefficient characteristic, responding faster at high temperatures. The detection time for HSF and FUL has been reduced to 150 ns and 24 ns respectively, resulting in a significant enhancement in detection speed. Furthermore, this solution exhibits robust noise immunity, a streamlined architecture, high integration density, and cost-effectiveness, positioning it as one of the most superior options among contemporary alternatives of its kind. The proposed scheme's circuit diagram, which is primarily composed of four components—the device being tested, the current RC circuit, the detection circuit, and the logic judgement circuit—is depicted in Fig. 2.

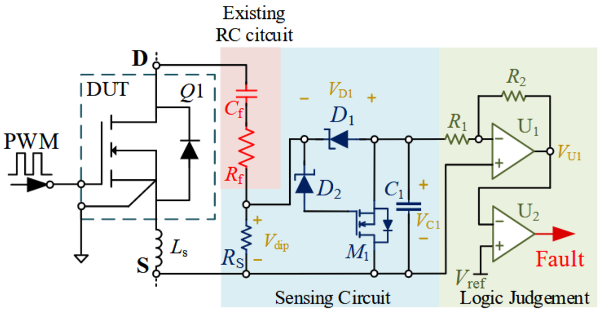

Fig. 2. Schematic diagram of the fast short-circuit detection method based on the drain-source voltage swing [10].

3.2 Based on I_D

This current-monitoring SC protection technique identifies electrical faults by precisely tracking real-time current flow through components, thereby avoiding the blanking time problem of early drain voltage detection.

The short-circuit detection based on ID typically utilizes the high bandwidth and accuracy of Rogowski current sensors (RCS) to directly determine the actual current passing through the SiC MOSFET's instantaneous rate of change. and integrate it back into a current signal. Once the current signal exceeds the preset fault threshold, the protection circuit will quickly trigger the gate driver to switch the SiC MOSFET off thereby achieving rapid protection within the short-circuit withstand time of the SiC device. The conventional RCS circuit comprises a Rogowski coil and an integrator, as illustrated in Fig 3a. The voltage induced in the Rogowski coil is directly proportional to the rate of change of the measured current. This induced voltage is subsequently integrated to generate an output waveform that corresponds to the waveform of the measured current.

To address sensing errors, Lee et al. proposed a three-stage RCS circuit architecture (Fig. 3b) [18] , comprising an input filter, an integrator, and an output filter. This configuration effectively attenuates high-frequency noise at the integrator input, reduces noise at the integrator output, operates away from the gain reduction region, and consequently minimizes both sensing errors and output noise. The RCS circuit is connected to a comparator, which compares the processed induced voltage from ID with a preset threshold. When ID is too high, a fault signal is sent out to control the gate driver to turn off the device. The detection times for HSF and FUL in this scheme are 100 ns and 90 ns, respectively.

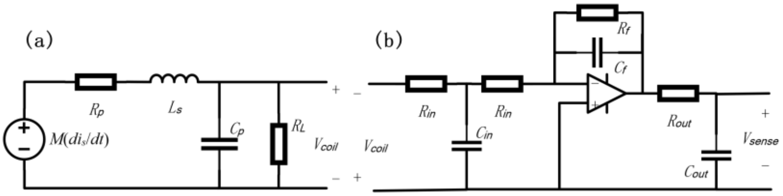

Fig. 3. (a) Equivalent circuit diagram of Rogowski coil, (b) Circuit diagram of RCS [18].

A printed circuit board (PCB) with coils was created by Rafiq et al. to carry out the previously specified detection operation [19]. The magnetic field created by the current passing through a single connector trace between the power device and the DC bus was used to sense the current by positioning a PCB coil close to the trace. The protective circuit's response time could be reduced to less than 25 ns with an improved design.

3.3 Based on parasitic parameters (di_D/dt)

The diD/dt detection technique utilizes the inherent parasitic inductance (Lss) existing between the power supply and Kelvin source connections. During fault conditions, ID experiences rapid escalation, and the negative induced voltage on Lss rises accordingly, exceeding the threshold to trigger protection [20]. However, parasitic inductance is susceptible to noise interference, leading to potential false triggering issues; during normal device turn-on, a high diD/dt may occur, causing protective measures to malfunction erroneously; when the inductance value in the short-circuit loop is substantial, diD/dt decreases, resulting in diminished measurement accuracy.

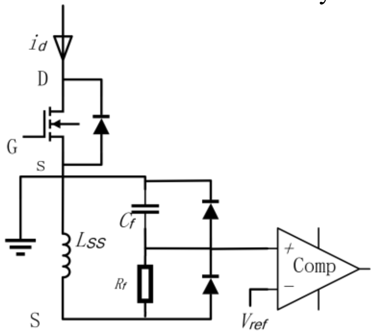

Fig. 4. Fundamental schematic diagram of di_D/dt-RC detection [7].

To address the aforementioned issues, researchers have proposed a variety of improvement schemes. The diD/dt-RC detection technique [21], presented in Fig. 4, utilizes an RC integrator to transform the voltage generated in parasitic inductance into measurable current parameters. This approach effectively mitigates the issue of false triggering caused by excessive positive rate of change in turn-on current. However, after normal conduction, if diD/dt approaches zero, the integral capacitor will discharge, making it impossible to accurately determine when FUL occurs [22]. By forming an RCD circuit (diD/dt-RCD) by connecting a diode in series in an RC circuit, the discharge of the capacitor after the current stabilizes can be prevented, thereby providing more accurate and reliable results. Especially under FUL conditions, it shows a faster detection time (100 ns for RC and 60 ns for RCD) [20][23]. In response to the significant current trigger difference between HSF and FUL, Tan Yaxiong et al. proposed a dual-threshold detection circuit [24], designing detection loops for HSF and FUL respectively on both sides of the parasitic inductance. The implementation of dual comparators facilitates the establishment of individual threshold values for two distinct circuits, while the integration of OR gates and D flip-flops enables the accurate identification and output of fault signals. The system's response time exhibits a positive correlation with the increase in bus voltage, achieving detection times of 90 ns and 29.4 ns at a bus voltage of 500 V.

3.4 Based on I_G

The gate current (IG)-based short-circuit detection methodology represents a strategic approach that identifies short-circuit faults by monitoring anomalous waveforms in the gate current. When an HSF occurs in a SiC MOSFET, the device exits the current linear region as the drain-source voltage (VDS) rapidly rises to the bus voltage (VDC) [25]. Under such conditions, the Miller plateau of the gate-source voltage (VGS) dissipates, with the gate charge being extracted and the current directed toward the source [26]. When FUL occurs, VDS will rapidly rise from its rated conduction voltage to the bus voltage [27]. This higher dVDS/dt generates displacement current through the device's Miller capacitance (CGD), which in turn causes a spike in the gate voltage [17], resulting in current flow into the gate. The two components of IG are respectively positively correlated with dVGS/dt and (dVGS/dt - dVDS/dt)。 In both HSF and FUL conditions, VDS undergoes a rapid rise, dVGS/dt is significantly smaller than dVDS/dt, and consequently, IG assumes a negative value [28].

To implement IG measurement, Ke et al. developed a monitoring circuit shown in Fig. 5 [29], which estimates the current indirectly through VR,ext measurements on external gate resistance Rg,ext applying Ohm's Law. As soon as a short circuit occurs, the high-level drive signal Vdrive concurrently satisfies the condition of being below the threshold VR,ext, thereby triggering the fault signal. The selection of Rg,ext in the scheme is of great significance. Unsuitable parameters will have adverse effects on the working performance of the device and the detection performance of the circuit. This method achieves extremely fast short-circuit detection and protection times, with the detection times for HSF and FUL being 69 ns and 50 ns, respectively. Because this type of solution is independent of the Kelvin source, it is less likely to cause false triggers. Additionally, the detection target IG shows little change in response to bus voltage, which increases dependability [30].

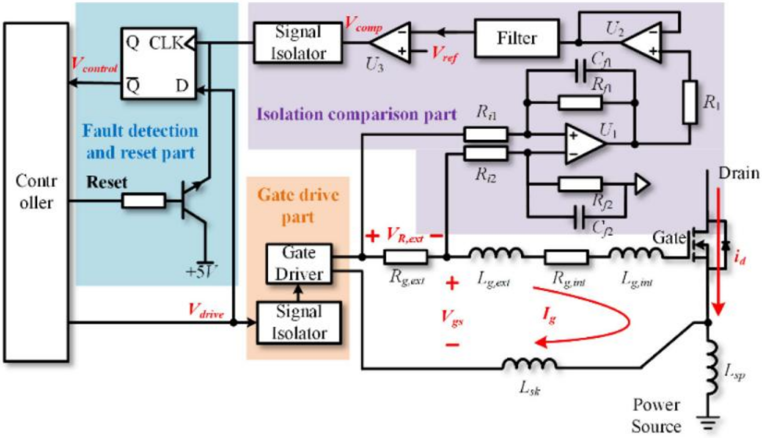

Fig. 5. SCP Circuit Based on IG Detection [29].

Table 1 compares and summarizes the benefits and drawbacks of various detection techniques.

Table 1. Comparison of Short-Circuit Detection Methods.

Methods		Advantages	Disadvantages
V_{DS}	V_{DS}	Simple structure, low cost	Blanking time, easily distracted
	dv_{DS}/dt	Anti-noise, easy integration, low cost	Parameter sensitive

	V_{DS} swing	Anti-noise, low cost, negative temperature coefficient	Parameter sensitive
I_D	Rogowski current sensor	Anti-noise, high integration density, high sensitivity, temperature stability	Complex design, parasitic parameter constraints
I_D	Rogowski current sensor (the minimum trace length)	Anti-noise, high integration density, high sensitivity	Complex design, TO-247 packaging, 3D-FEMsimulation
di_D/dt	di_D/dt-RCD double-threshold di_D/dt	High accuracy, threshold consistency, temperature stability, low cost anti-interference, high flexibility, low FUL short-circuit current peak	Kelvin source pin, high-frequency oscillation
I_G		Anti-interference, wide applicability, high reliability	High-frequency oscillation, parameter sensitive, complex design

4 Conclusion

This paper, through a comprehensive review of recent studies on short-circuit phenomena, identifies two primary fault categories: HSF and FUL. It offers a thorough explanation of the physical mechanisms and influencing factors of G-S short-circuit and D-S short-circuit, including the effects of bus voltage, drive voltage, and short-circuit duration. Furthermore, the paper conducts a comparative analysis of detection techniques based on various parameters. In recent years, many studies have effectively addressed the problem of false triggering caused by the high-speed switching characteristics of SiC MOSFETs, and the detection time has also entered the 100 ns range. However, the detection accuracy and threshold limitations caused by the significant influence of junction temperature on the electrical characteristics of SiC MOSFETs still need to be overcome; the existing methods also lack the adaptive ability to bus voltage. In the future, the development direction of short-circuit protection may tend to be integrated and intelligent. The improvement of the structure of the device itself, manufacturing process and packaging technology may also bring new leaps to short-circuit protection.

References

1. J. Chen, E. Deng, Z. Zhao, Y. Wu and Y. Huang, Failure Mechanism Analysis of SiC MOSFET under Different Aging Test Methods. Trans. Chin. Electrotech. Soc. 35, 5105 (2020)
2. J. Kang, Z. Xin, J. Chen, H. Wang and W. Li, Review and Prospect of Short-circuit Failure and Degradation Mechanism of SiC MOSFET, Proc. CSEE 41, 1069 (2021)

3. Y. Wen, Y. Yang, Y. Gao, Active Gate Driver for Improving Current Sharing Performance of Paralleled High-Power SiC MOSFET Modules, IEEE Trans. Power Electron. 36, 1491 (2021)
4. W. Wu, W. Dou, Z. Xing, G. Huang and S. Ge, Study of Wide Bandgap SiC Technology for City Driving Energy Consumption in Electric vehicle, New Energy Veh. 24, 106 (2021)
5. X. Hu, Integrated Drive Circuit Design Method for SiC MOSFET Considering Short-circuit Protection and Junction Temperature Monitoring, Master thesis, Beijing Jiaotong University, School of Electrical Engineering (2024)
6. T. Zhang, Research on SiC MOSFET Series Short-Circuit Voltage Sharing Characteristics and Short-Circuit Protection, Master thesis, China University of Mining and Technology, School of Electrical Engineering (2023)
7. Y. Wen, Y. Yang, H. Ning, Y. Zhang and Y. Gao, Review on Short-Circuit Protection Technology of SiC MOSFET, Trans. Chin. Electrotech. Soc. 37, 2538 (2022)
8. J. Meng, Research on Short-Circuit Failure Characteristics of Silicon Carbide MOSFET, Master thesis, North China Electric Power University, School of Electrical and Electronic Engineering (2024)
9. H. Wang, F. Blaabjerg, Electronics Reliability: State of the Art and Outlook, IEEE J. Emerg. Sel. Top. Power Electron. 9, 6476 (2021)
10. Z. Li, B. Ji, K. Tan, P. Yu, Z. Wang, M. Luo and W. Cao, A Fast Short Circuit Detection Method for SiC MOSFETs Based on Drain Voltage Swing, IEEE J. Emerg. Sel. Top. Power Electron. Early Access, 1 (2025)
11. F. Boigea, F. Richardeau, S. Lefebvre, J.-M. Blaquière, G. Guibaud and A. Bourennane, Ensure an original and safe “fail-to-open” mode in planar and trench power SiC MOSFET devices in extreme short-circuit operation, Microelectron. Reliab. 88-90, 598 (2018)
12. I. Kovacevic-Badstuebner, S. Race, N. Luethi, M. Nagel and U. Grossner, Fail-to-Open Short Circuit Failure Mode of SiC Power MOSFETs: 2-D Thermo-Mechanical Modeling, Solid State Phenom. 358, 121 (2024)
13. Z. Zhang, L. Liang, H. Fei, Investigation on Safe-operating-area Degradation and Failure Modes of SiC MOSFETs under Repetitive Short-circuit Conditions, Power Electron. Devices Compon. 4, 100026 (2023).
14. C. Unger, M. Pfost, Particularities of the Short-circuit Operation and Failure Modes of SiC-MOSFETs, IEEE J. Emerg. Sel. Top. Power Electron. 9, 6432 (2021)
15. J. An, M. Namai, H. Yano, N. Iwamuro, Methodology for Enhanced Short-circuit Capability of SiC MOSFETs, in 2018 IEEE 30th International Symposium on Power Semiconductor Devices and Ics (ISPSD), Chicago, May 13-17 (2018), 391
16. K. Yao, H. Yano, N. Iwamuro, Investigations of Short-circuit Failure in Double Trench SiC MOSFETs Through Three-dimensional Electro-thermal-mechanical Stress Analysis, Microelectron. Reliab. 122, 114163 (2021)
17. J. Li, Analysis and Optimization of Desaturation Protection Circuit for SiC MOSFETs, Master thesis, Huazhong University of Science and Technology, School of Electrical and Electronic Engineering (2024)
18. J.-A. Lee, D.H. Sim and B.K. Lee, Short-circuit Protection for SiC MOSFET Based on PCB-type Rogowski Current Sensor: Design Guidelines, Practical Solutions, and Performance Validation, IEEE Trans. Power Electron. 39, 3580 (2024)
19. A. Rafiq, S. Pramanick, Ultrafast Protection of Discrete SiC MOSFETs with PCB Coil-based Current Sensors, IEEE Trans. Power Electron. 38, 1860 (2023)
20. J. Xue, Z. Xin, H. Wang, P.C. Loh and F. Blaabjerg, An Improved di/dt -RCD Detection for Short-circuit Protection of SiC Mosfet, IEEE Trans. Power Electron. 36, 12 (2021)

21. Z. Wang, X. Shi, Y. Xue, L.M. Tolbert, B.J. Blalock and F. Wang, Design and Performance Evaluation of Overcurrent Protection Schemes for Silicon Carbide (SiC) Power MOSFETs, in 2013 IEEE Energy Conversion Congress and Exposition, Denver, September 15-19 (2013), 5418
22. G. Lyu, H. Ali, H. Tan, L. Peng and X. Ding, Review on Short-Circuit Protection Methods for SiC MOSFETs, Energies, 17, 4523 (2024).
23. K. Sun, J. Wang, R. Burgos and D. Boroyevich, Design, Analysis, and Discussion of Short Circuit and Overload Gate-Driver Dual-Protection Scheme for 1.2-kV, 400-A SiC MOSFET Modules, IEEE Trans. Power Electron. 35, 3054 (2019)
24. Y. Tan, Y. Liu, M. Zhang, J. Guo, Research on a Dual-threshold Detection Short-circuit Protection Circuit for SiC MOSFET, Proc. CSEE (to be published), (2025).
25. T. Wang, Z. Huang, X. Yu, M. Zhang, R. Luo, X. Li, Short-circuit Protection Method for High-voltage and High-power SiC MOSFETs, High Volt. Eng. 50, 1583 (2024)
26. M. Picot-Digoix, F. Richardeau, J.-M. Blaquière, S. Vinnac, S. Azzopardi and T.-L. Le, Quasi-flying Gate Concept Used for Short-circuit Detection on SiC Power MOSFETs Based on a Dual-port Gate Driver, IEEE Trans. Power Electron. 38, 6934 (2023)
27. W. Ouyang, P. Sun, M. Xie, Q. Luo and X. Du, A Fast Short-circuit Protection Method for SiC MOSFET Based on Indirect Power Dissipation Level, IEEE Trans. Power Electron. 37, 8825 (2022)
28. B. Hu, Z. Ke, M. He, C.Zhang, Z. Liu, J. Wang, A Gate Current Detection for Short-circuit Protection of SiC MOSFET, in 2023 IEEE 4th China International Youth Conference on Electrical Engineering (CIYCEE), Chengdu, December 8-10 (2023), 1
29. Z. Ke, J. Wang, B. Hu, X. Song, Z. Peng, Y. Dai and Z.J. Shen, An Ultrafast Universal Short-circuit Protection Technique Based on Gate Current Detection for SiC MOSFET, IEEE Trans. Power Electron. 39, 11931 (2024)
30. Z. Guo, H. Li, Dv/dt Sensing-based Short-circuit Protection for Medium-voltage SiC Mosfets, IEEE Trans. Power Electron. 38, 10554 (2022)