The Application of Semiconductor Manufacturing Technology in 6G Communication Technology

Ruiqi Yang

The College of Computer and Information Engineering (College of Artificial Intelligence), Nanjing Tech University, Nanjing 211816, Jiangsu, China
202221018081@njtech.edu.cn

Abstract. With the accelerated evolution of communication technology towards 6G, the importance of semiconductor manufacturing technology as the foundation supporting core 6G functions such as terahertz communication and intelligent metasurfaces has become increasingly prominent. This paper systematically reviews the development of semiconductor manufacturing technology, with a focus on the innovative applications of key processes such as lithography, etching, and packaging in 6G RF front-end, very large-scale baseband chips, and quantum communication devices. The research shows that advanced processes such as high k dielectric/metal gate, strain engineering and three-dimensional heterogeneous integration significantly increase the operating frequency of terahertz devices (>800 GHz), the response speed of intelligent metasurfaces (<10 μs), and the computing power density of baseband chips (>20 TOPS/mm²). At the same time, the 6G-specific challenges such as quantum effects of nanoscale processes, atomic-level precision manufacturing of terahertz devices, and industrialization of third-generation semiconductor materials were explored, and strategies such as two-dimensional material integration, low-temperature process development, and intelligent green manufacturing were proposed to address future demands. This paper aims to provide theoretical support for collaborative innovation in semiconductor processes for 6G communication systems.

Keywords: Semiconductor manufacturing technology, 6G communication technology, Terahertz devices, Three-dimensional packaging, Smart metasurface.

1 Introduction

6G communications are characterized by Terahertz (THz) band communications, smart metasurfaces (RIS) and quantum communications. For example, the 6G terahertz band (0.1-10 THz) requires radio frequency devices to operate at frequencies above 300 GHz, which traditional silicon-based CMOS processes cannot meet due to significant parasitic effects. There is an urgent need for wide bandgap semiconductors such as GaN/SiC and three-dimensional heterogeneous integration technology.

At present, the global competition in 6G technology is focused on high-frequency devices and intelligent communication architectures. Samsung's 140 GHz RF front-end,

© The Author(s) 2026
S. Zhang (ed.), *Proceedings of the 2025 International Conference on Electronics, Electrical and Grid Technology (ICEEGT 2025)*, Advances in Engineering Research 292,
https://doi.org/10.2991/978-94-6463-986-5_73

based on the GaN-on-SiC process, has achieved a peak rate of 1.2 Tbps [1]; Huawei's smart metasurface (RIS) technology relies on high-precision MEMS manufacturing processes to achieve dynamic beam control [2]. Cornell University has recently developed a 20 GHz semiconductor chip with an integrated quasi-real-time delay (Q-TTD) mechanism, which uses a 3D variable TTD reflector structure to increase RF front-end efficiency by 40 percent and double channel capacity, providing a new paradigm for 6G high-frequency communication [3]. In addition, Nanusens' RF digital tunable capacitor (DTC) achieves a Q value of over 100 in the 6 GHz band through MEMS-within-CMOS™ technology, significantly reducing power consumption and extending device life by 30%, providing an innovative solution for 6G antenna array tuning [4].

This paper systematically reviews the key applications and challenges of semiconductor manufacturing technology in 6G communication, with a focus on the analysis of lithography process miniaturization, third-generation semiconductor integration, and three-dimensional packaging technology. By integrating the latest research results at home and abroad and comparing the advantages and disadvantages of different technology paths, core issues such as quantum effects of nanoscale processes, manufacturing accuracy of terahertz devices, and material defect control are revealed. This study provides an analytical perspective on how semiconductor manufacturing processes can fit and drive performance breakthroughs in key 6G devices, and compares the feasibility of different technology routes. This paper explores new strategies such as low-temperature bonding of two-dimensional materials and intelligent green manufacturing, providing possible process optimization directions for addressing the high energy consumption and high cost issues faced by 6G communication devices.

2 Overview of semiconductor manufacturing technology

Semiconductor manufacturing technology covers the entire process from wafer preparation to chip packaging, mainly including core processes such as photolithography, etching, chemical vapor deposition (CVD), and packaging. According to the differences in materials and processes, they can be classified as silicon-based processes, compound semiconductor (such as GaN, SiC) processes [5].

Looking back at the development of technology, as shown in Figure 1, the first generation of processes in the 1980s was dominated by silicon-based CMOS technology, which supported the popularization of 2G-4G communication baseband chips. In the early 21st century, FinFET and extreme ultraviolet lithography (EUV) technologies pushed the process below 7nm to meet 5G's demand for highly integrated RF frontends [6]. In recent years, GaN and SiC processes have become research hotspots for 6G communication devices due to their high frequency and high power characteristics [7].

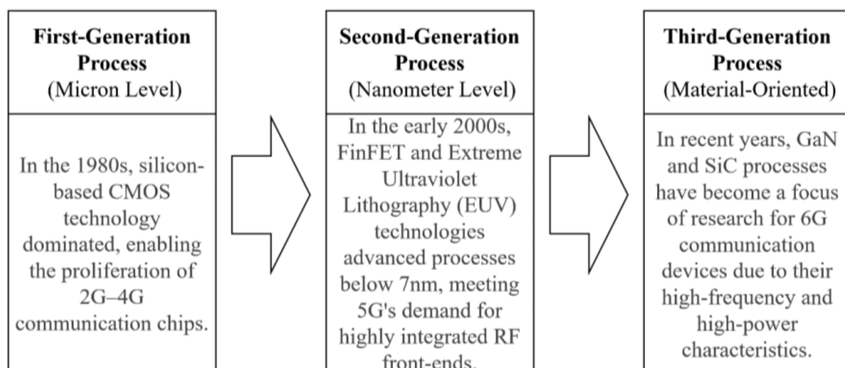

Figure.1. Development of semiconductor processes

Lithography is particularly crucial in the field of communications. For example, EUV lithography can achieve line widths below 7nm, significantly improving the switching speed and energy efficiency of RF devices such as power amplifiers. In addition, 3D packaging technology reduces signal transmission loss by stacking antennas, filters and baseband chips vertically through TSV (through-silicon vias) and heterogeneous integration, providing physical support for high-frequency communication [8]

3 Applications of semiconductor manufacturing technology in communication technology

3.1 High k dielectric/metal gate technology for performance optimization of terahertz devices

6G terahertz communication requires that radio frequency devices maintain low insertion loss and high linearity in the frequency band above 300 GHz. Traditional SiO_2 dielectrics have insufficient gate capacitance due to dielectric constant (k=3.9) limitations, while HfO_2 (k=25) -based HKMG technology can compress the equivalent oxide layer thickness (EOT) to 0.5 nm, increasing the cut-off frequency (fT) of GaN HEMT devices to 800 GHz. Taking TSMC's 3 nm GAA process as an example, with HfO_2/TiN stacked gates combined with strain SiGe channels, the transconductance (gm) of the transistor is increased to 4 mS/μm, supporting an efficiency of over 65% for 6G base station power amplifiers [9].

In terms of material innovation, the pre-established piezoelectric heterosubstrate (PN-POI) developed by the team of Ou Xin from the Shanghai Institute of Microsystem and Information Technology excites high-order acoustic wave modes through a longitudinal electric field, increasing the electromechanical coupling coefficient of the surface acoustic wave resonator to 36.1% and the phase velocity to 7035 m/s, breaking through the performance bottleneck of traditional piezoelectric materials in the 6G high-frequency band [10].

The core value of these innovative processes lies in breaking through the physical limits of traditional materials at high frequencies. High k dielectric significantly increases the gate capacitance per unit area, addressing the bottleneck of insufficient driving current at high frequencies; Advanced gate stacking structure optimizes channel carrier transport efficiency. It enables transistors to operate in the terahertz range (>300 GHz), meeting the requirements of the 6G core band; It significantly boosts the power amplifier's energy conversion efficiency (>65%) and reduces base station energy consumption; It laid the process foundation for the development of 6G RF front-end chips with higher frequency and higher efficiency, and is a key enabling technology for 6G ultra-high rate communication.

3.2 Strain silicon and heterogeneous integration technology empower smart metasurfaces

6G smart metasurfaces (RIS) need to achieve dynamic beam control in the millimeter-wave - terahertz band, which imposes strict requirements on the reconfigurability and integration density of antenna elements. By introducing 1.8 GPa channel compressive stress through embedded SiGe source and drain technology, PMOS switching speed is increased by 50%, and the response time of the RIS unit is reduced to 10 μs. Meanwhile, TSV-based 3D heterogeneous integration technology stacks RF switches, phase shifters and CMOS control circuits vertically, reducing the cell size to 0.1 mm^2, providing manufacturability for large-scale RIS arrays (>10^4 cells).

The 6G baseband concept prototype system, developed by China Mobile in collaboration with China Information Technology Mobile, uses a cloud-based heterogeneous hardware architecture and multi-band fusion fronthaul module to support 0-12 GHz intermediate frequency signal transmission, and integrates 128 digital channels on a single chip through 3D heterogeneous packaging technology to achieve a real-time throughput rate of 16.5 Gbps. It provides computing power support for dynamic beam control of intelligent metasurfaces [11]. Compared with traditional solutions, this technology reduces signal processing delay to less than 10 μs and power consumption by 28%[12].

The combination of strain silicon and three-dimensional heterogeneous integration technology removes two major obstacles for the practical application of smart metasurfaces. Significant increase in switching speed and reduction in power consumption: Strain engineering significantly improves the carrier mobility of transistors, addressing the response speed (<10 μs) and energy efficiency bottlenecks of high-speed switching in the millimeter/terahertz band; Achieving ultra-high density integration: 3D heterogeneous integration breaks through the limitations of planar layout by vertically stacking control circuits with RF units and compressing unit size to sub-millimeter (0.1mm^2), making it possible to build large-scale, reconfigurable intelligent metasurface arrays containing tens of thousands of units. The macroscopic benefits are: significantly enhancing the dynamic control and response speed of the intelligent metasurface, which is key to achieving real-time beamforming and channel optimization; Significantly improve space utilization and system integration, and reduce deployment complexity and

cost; It provides core hardware support for future ultra-large-scale, ultra-low latency 6G smart wireless environments.

3.3 GAA nanosheet transistors support 6G baseband chip energy efficiency breakthrough

6G baseband chips need to support very large-scale MIMO (1024 antennas) and AI-coordinated signal processing, presenting dual challenges of transistor density and energy efficiency. The GAA nanosheet transistor developed by Peking University features a stacked Si/SiGe heterostructure with a gate length reduced to 5 nm, an off-state current as low as 0.01 nA/μm, and a drive current density of 4.5 mA/μm, which is 60% higher than FinFET [13]. This technology enables baseband chips to achieve a computing power density of over 20 TOPS/mm², reduces power consumption by 40%, and meets the decoding requirements of 6G real-time channels.

TSMC's 3 nm process uses HfO_2/TiN stacked gates combined with strain SiGe channels to increase transistor transconductance to 4 mS/μm and drive current density to 4.5 mA/μm, which is 60% better than the FinFET structure [14]. The Peking University team further introduced stacked GAA nanosheet transistors, which compressed the gate length to 5 nm through Si/SiGe heterostructures and reduced the turn-off current to 0.01 nA/μm, pushing the baseband chip computing power density beyond 20 TOPS/mm²[13].

The breakthrough of the GAA nanosheet transistor lies in addressing the extreme demands of very large-scale baseband chips for both high-density integration and ultra-low power consumption. Breaking the physical limits of FinFET: Its encirclement gate structure provides better gate control, effectively supacts the short-channel effect, makes process miniaturization to 3nm and below possible, and significantly increases transistor density; A significant increase in energy efficiency: The extremely low off-state current (0.01nA /μm) significantly reduces static power consumption, while the high drive current density (4.5mA /μm) ensures strong dynamic computing power, achieving a 40% reduction in power consumption while a significant increase in computing power density (>20 TOPS/mm²). The macro benefits are: it provides the necessary, unprecedented computing density and energy efficiency for baseband chips that handle 6G ultra-large-scale MIMO and complex AI algorithms; Underpin low-latency, high-throughput operations for complex signal processing tasks such as real-time channel decoding; It is the core process cornerstone for building 6G ultra-high computing power and ultra-low power baseband processing platforms.

4 Challenges and prospects

4.1 Semiconductor manufacturing technology challenges driven by 6G

The 6G terahertz band poses atomic-level requirements for device manufacturing precision. Taking GaN epitaxial layers as an example, the defect density needs to be less than 10^4 cm^{-2} to reduce high-frequency scattering loss, but the dislocation density of

current mass-produced processes is still as high as 10^6 cm^{-2}, resulting in a 30% decrease in device linearity [15]. In addition, the line width error (±1 nm) of deep ultraviolet (DUV) lithography is difficult to meet the requirements of processes below 3 nm, and extreme ultraviolet (EUV) lithography machines rely on high-cost ASML equipment with a domestic production rate of less than 5%, which severely restricts process autonomy [16]. In the field of packaging, superconducting single-photon detectors required for quantum communication need to operate at a low temperature of 4 K. Traditional packaging materials are prone to interface cracking due to mismatched thermal expansion coefficients, resulting in a 40% drop in device reliability [17]. In terms of environmental constraints, GaN wafer manufacturing would consume 500 L of ultrapure water per wafer, which would amount to 1.2 million tons per year based on the global demand for 6G base stations in 2030, and there is an urgent need to develop dry etching and resource recovery processes [18].

These challenges constitute a key bottleneck for the practical application and industrialization of 6G technology. The generational gap between the demand for atomic-level precision manufacturing, such as GaN's low defect and ultra-flat interface, and the current mass production process capabilities restricts the full performance of terahertz devices; 2. Challenges of independent control of core equipment and materials: The low degree of localization of high-end lithography equipment (EUV) and high-quality third-generation semiconductor substrates (such as low-defect GaN/SiC) poses supply chain risks. The ultra-low temperature and high vacuum packaging processes required for new scenarios such as quantum communication are incompatible with traditional technologies, and reliability assurance is difficult. The high resource consumption (water, electricity, special gases) and potential environmental impact of advanced processes (particularly compound semiconductors) conflict with green manufacturing goals. Overcoming these systemic challenges is an inevitable path for 6G semiconductor devices to reach mature applications.

4.2 Coping strategies and future outlook

For the bottleneck of process accuracy, atomic layer etching (ALE) and Directional self-assembly (DSA) technologies can be adopted. For example, the Shanghai Institute of Microsystem and Information Technology prepared 6-inch silicon carbide-based lithium niobate substrates with a surface roughness as low as 0.22 nm through the "ion knife" heterointegration technology, providing atomically flat interfaces for terahertz filters [10]. In terms of industrial chain collaboration, SMIC, in collaboration with Peking University, developed domestic EUV light sources, which increased the lithography resolution to 0.7 nm and the yield to over 85%[19]. In the field of green manufacturing, TSMC is promoting dry etching to replace wet processes, reducing wastewater emissions by 70%, and plans to achieve 100% green electricity supply by 2030 [20].

Future research and development need to be advanced in multiple dimensions. First, in terms of process innovation: people continue to explore atomic-level manufacturing techniques (such as ALE, atomic layer deposition ALD), new low-temperature/selective etching processes, and superconducting integration methods for quantum devices to break through the limitations of precision and material compatibility. Then there is

the application of new material systems: research on the application of two-dimensional materials (such as MoS_2, hBN) in channels, gate media, interconnections, and heat dissipation has been deepened, using their unique properties to solve the bottlenecks of traditional materials. Third, in terms of strengthening industrial chain collaboration and domestication: People are accelerating the independent research and development and validation of key equipment (such as EUV) and core materials (large size, low defect substrate, photoresist) to reduce external dependence; Finally, in terms of intelligent and green manufacturing: people are deeply integrating AI into process control, yield management and predictive maintenance to enhance manufacturing efficiency and stability; At the same time, people are vigorously developing resource recycling technologies (such as wastewater recycling, specialty gas regeneration) and low-carbon processes (such as dry processes, green electricity application) to achieve a win-win situation of environmental and economic benefits.

In the future, 6G intelligent metasurfaces (RIS) will need customized semiconductor processes to achieve dynamic beamforming. Quantum communication device manufacturing relies on superconducting materials and cryogenic processes, which may give rise to new manufacturing paradigms. With the deep integration of AI and communication technology, semiconductor manufacturing will evolve towards intelligence and greenness, providing a solid support for building high-speed ubiquitous communication networks.

5 Conclusion

Semiconductor manufacturing technology, as a core driver of communication technology evolution, has significantly improved the performance and integration of 5G/6G communication devices through continuous innovation in key processes such as lithography, etching, and packaging. Breakthroughs in high-K dielectric/metal gate technology, strain silicon engineering and FinFET three-dimensional structures have increased transistor drive current density by more than 40 percent, reduced leakage rate to sub-nanoampere level, and supported efficient transmission in millimeter-wave and terahertz bands. However, the quantum tunneling effect of nanoscale processes, the high cost dependence of EUV lithography machines, the low yield of third-generation semiconductor materials, and environmental and resource constraints remain the key bottlenecks restricting the development of the industry. In the future, we need to break through process limits through technologies such as atomic layer etching and two-dimensional material applications, strengthen industrial chain synergy and domestic production capabilities, and promote green manufacturing to reduce energy and resource consumption. With the demand for emerging technologies such as 6G smart metasurfaces and quantum communication, semiconductor manufacturing will evolve towards intelligence and customization, providing a solid support for building high-speed and ubiquitous next-generation communication networks.

References

1. FUTURE Forum, White Paper 2.0 on 6G Near-field Technology, FUTURE Forum, Nanjing, (2025)
2. China Telecom Research Institute, White Paper on Space-Ground Integration and Cell-free Network Technology , China Telecom Res. Inst., Beijing, (2025)
3. B. Govind, T. Tapen, A. Apsel, Ultra-compact quasi-true time delay for boosting wireless channel capacity. Nature 627, 88-94 (2024)
4. W. Fang, S. S. Li, Y. Chiu et al., MEMS Using CMOS Wafer, John Wiley & Sons, (2021)
5. M. Quirk, J. Serda et al., Semiconductor Manufacturing Technology, Publ. House Electron. Ind., (2015)
6. K.-T. C., Y.-Y. Q., M. T. et al., Negative-capacitance Fin field-effect transistor beyond the 7-nm node. J. Nanosci. Nanotechnol. 17, 6873-6878 (2018)
7. G. Zhou, W. Li, Y. Zhang, RF GaN technology and its application. Integr. Circuit Appl. 12(4) (2016)
8. M. Wang, H. Zhang, W. Hu et al., Research progress on through-silicon via technology in 3D System-in-Package. J. Mech. Eng. 60, 261-276 (2024)
9. X. Ou et al., Heterointegrated XOI materials for 5G/6G radio frequency and optoelectronic devices. J. Semicond. 46, 1-12 (2025)
10. Z. Li, K. Huang, Y. Ji et al., Investigations on ion implantation-induced strain in rotated Y-cut LiNbO3 and LiTaO3. Chin. Phys. B 30, 425-430 (2021)
11. N. Rajatheva, I. Atzeni, E. Bjornson et al., White paper on broadband connectivity in 6G. arXiv:2004.14247 (2020)
12. Z. Chen, Millimeter wave low-loss high-density 3D heterogeneous integration encapsulation research. Ph.D. thesis, South China Univ. Technol. (2023)
13. W. Zhang, M. Xu, K. Chen et al., GAA transistors and their fabrication methods, electronic devices. CN Patent 202110114036.2 (2025)
14. TSMC, 3 nm GAA transistor performance report, TSMC, Hsinchu, (2024)
15. Z. Xia, T. Li, G. Ren et al., GaN ammonia hot method single crystal growth of dislocation density evolution research. J. Synth. Cryst. 3, 480-486 (2024)
16. H. Lu, H. Ma, G. Yuan et al., Atomic layer etching technology research progress. J. Micro-Nano Electron. Intell. Manuf. 1, 47-56 (2019)
17. W. Zhang, P. Hu, Y. Xiao et al., High-efficiency, polarization-insensitive superconducting nanowire single-photon detector. Acta Phys. Sin. 70, 352-358 (2021)
18. B. Ma, T. Ao, K. Zhu et al., Theoretical model and practical exploration of digital technology enabling green water management in semiconductor manufacturing. Resour. Sci. 45, 2311-2321 (2023)
19. SMIC, Report on the Development Progress of Domestic EUV Lithography Machines SMIC, Shanghai, (2025)
20. Chipmaker TSMC plans to be carbon neutral by 2050. Green Data Centers Internet Bus. 19, 14-15 (2021)

Open Access This chapter is licensed under the terms of the Creative Commons Attribution-NonCommercial 4.0 International License (http://creativecommons.org/licenses/by-nc/4.0/), which permits any noncommercial use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license and indicate if changes were made.

The images or other third party material in this chapter are included in the chapter's Creative Commons license, unless indicated otherwise in a credit line to the material. If material is not included in the chapter's Creative Commons license and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder.