Research on Defect Control Technology of Wide Bandgap Semiconductor Substrates Centered on SiC

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Abstract. This paper integrates various types of literature and describes various defects generated during the crystal growth process. Then the various defects generated were classified into the interior, surface and near-surface of the crystal, and the causes of the defects were described. Secondly, this paper expounds the three stages of SiC substrate manufacturing, namely crystal growth, epitaxial process and post processing, and introduces the defect control technology among them at the same time. Among them, the repeated a-face growth technique (RAF) can effectively reduce the dislocation density through dislocation direction conversion. The solution growth method can convert dislocations in the thermodynamic equilibrium state. Optimizing the flow rate of HCl gas in the epitaxial process can suppress the formation of triangular defects. The improvement of vertical high-speed rotating CVD equipment can enhance the epitaxial uniformity. Furthermore, femtosecond laser technology is highly efficient and low-loss, and annealing technology can indirectly reduce the formation of dislocations. This paper argues that the process equipment can be optimized to reduce defects, and at the same time, the growth rate can be precisely regulated to control the defects.

Keywords: Wide bandgap semiconductor, Silicon carbide, Defect control.

1 Introduction

Semiconductor is a material whose electrical conductivity at room temperature lies between that of conductors and insulators. With the rapid development of electronic devices towards high frequency, high temperature and high power, the third-generation semiconductor materials and devices represented by silicon carbide (SiC) are gradually becoming the focus of technological competition and demonstrating irreplaceable application potential in fields such as new energy vehicles, smart grids and 5G communications. Scholars have found through research that there are over 200 known crystal forms of SiC, and different crystal forms simultaneously possess the same chemical properties, which endows it with a relatively high bandgap width, critical breakdown electric field, thermal conductivity, and saturated electron migration velocity [1]. The

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S. Zhang (ed.), *Proceedings of the 2025 International Conference on Electronics, Electrical and Grid Technology (ICEEGT 2025)*, Advances in Engineering Research 292,
https://doi.org/10.2991/978-94-6463-986-5_17

commonly used methods for preparing silicon carbide (SiC) single crystals in industry include three growth methods: the improved Lely method (physical vapor transport method), high-temperature chemical vapor deposition (HTCVD), and the liquid-phase method. However, various defects (such as micropipes, dislocations, etc.) generated during the preparation of SiC substrates can significantly reduce the reliability and lifespan of the devices and even lead to device failure [2]. Therefore, how to effectively control substrate defects has become a key challenge for improving the performance of SiC semiconductor devices.

Current research has proposed multiple technical approaches for SiC defect control, such as optimizing the crystal growth process, improving epitaxial conditions, and introducing post processing (such as chemical mechanical polishing and high-temperature annealing), etc [3]. However, most of the existing studies focus on the local optimization of a single technology, and there are still deficiencies in the systematic comparative analysis of various technologies. Furthermore, the academic circles lack in-depth exploration of the defect formation mechanism and the comparative analysis of various defect control techniques, which limits the application effect of some techniques in practical scenarios. Therefore, the classification of defect types and the systematic comparative analysis of defect control techniques are particularly important.

Based on this, this study focuses on 4H-SiC and takes this material as the core to sort out the types and causes of defects in wide bandgap semiconductor substrates, and comparatively analyze the principles, working efficiencies and applicable scenarios of the three mainstream control technologies of crystal growth, epitaxy, and post processing. This article aims to clarify the advantages and limitations of each technology and propose application methods for different application scenarios and requirements.

2 Defect types and Cause analysis

The defects in the crystal growth process are mainly divided into two types: internal crystal defects and surface and near-surface crystal defects.

2.1 Internal defects of the crystal

Internal crystal defects are one of the most central quality issues in the preparation process of SiC substrates. Their types, densities and distributions determine the electrical and thermal properties of the materials. Table 1 summarizes the types and effects of internal defects in SiC crystals. According to the different dimensions of the defects, the internal defects of SiC crystals can be roughly classified into the following four categories.

Point defect (zero-dimensional defect). Point defects are formed by introducing local defects in the SiC epitaxial layer from carbon vacancies, silicon vacancies, interstitial atoms, etc. [4]. Studies show that during the growth process of SiC crystals, a slight deviation in the Si/C stoichiometric ratio can lead to the formation of point defects such

as carbon vacancies and interstitial atoms, thereby affecting the carrier lifetime. Meanwhile, the unbalanced atomic diffusion in a high-temperature environment will intensify the density distribution of such defects. For example, carbon vacancies can introduce deep-level traps, resulting in a reduction in carrier lifetime; While impurity atoms such as nitrogen can improve electrical conductivity, excessive doping may cause lattice distortion and intensify leakage current.

Line defects (one-dimensional defects). Line defects are mainly dislocations, including Threading Screw Dislocations (TSDs), Threading Edge Dislocations (TEDs) and Basal Plane Dislocations (BPDs). TSDs are mainly replicated from seed crystals. In addition, the closure and dissociation of micropipe defects can also lead to the occurrence of TSDs. TEDs are also mostly replicated from seed crystals, and their dislocation density is approximately ten times that of TSDs [4]. The BPDs is a common one-dimensional crystallization defect in SiC substrates, usually located on the [0001] plane of SiC crystals. Nishiguchi et al. hold that BPDs are produced by the interaction between stacking faults and helical dislocations on the growth surface [5]. Ohtani et al. believe that when 4H-SiC crystals are grown by the PVT method, BPDs will nucleate in the shoulder area, then slip into the growing crystal and extend towards the growth front through the new growth layer. Subsequently, during the cooling process, the thermoelastic stress prompts the slip of BPDs, resulting in the growth of BPDs [6].

Surface defects (two- dimensional defects). Surface defects include Stacking Faults and Low-Angle Grain Boundaries. Stacking Faults are usually caused by localized misalignments in the stacking order of the atomic layers during the crystal growth process. Low-angle grain Boundaries arise from small orientation deviations of neighboring grains. Such defects disrupt the periodic potential field of the lattice, leading to a decrease in carrier mobility [7]. For example, Basal Plane Stacking Faults (BPSFs) in 4H-SiC can cause a significant increase in the forward voltage drop of bipolar devices.

Body defects (three-dimensional defects). Body defects are mainly represented by micropipes. The formation mechanisms of micropipes can be broadly categorized into three types: first, they are induced by carbon inclusions, Stacking Faults, etc.; second, they are formed by extension diffusion of micropipes in seed crystals; and third, they are formed by merger decomposition of the original micropipes in the SiC to produce new micropipes [4]. Micropipes are essentially aggregated forms of TSDs with diameters of up to a few micrometers, capable of triggering a localized concentration of electric field, resulting in device breakdown. The inclusions, on the other hand, are mostly unreacted Si or C particles, resulting from insufficient purity of the feedstock or improper control of the growth chamber pressure. It has been shown that the reliability of SiC MOSFETs deteriorates dramatically when micropipe density exceeds a certain threshold [8].

Table 1. Types and Effects of Internal Defects in SiC Crystals.

Defect Type	Typical Forms	Main Causes	Influences On Device Performance
Point Defect	Vacancies, Interstitial Atom	Stoichiometric Ratio Deviations, Impurity Incorporation	Reduced Carrier Lifetime, And Intensified Leakage Current
Line Defects	Threading Screw Dislocations, Threading Edge Dislocations, Basal Plane Dislocations	Thermal Stress, Seed Crystal Defects	Breakdown Voltage Drop, Mobility Decrease
Surface Defects	Stacking Misalignment, Small-Angle Grain Boundaries	Atomic Stacking Misorder, Grain Orientation Deviation	Increased Forward Pressure Drop
Body Defects	Micropipes, Inclusions	Dislocation Accumulation, Insufficient Purity Of Raw Materials	Local Breakdown, Deterioration Of Reliability

2.2 Surface and near-surface defects of crystals

Crystal surface and near-surface defects mainly include triangle defects, surface step bunching, “carrot” defects, pit defects, and so on.

Triangular defects are one of the most common types of defects in the epitaxial growth of SiC, named for their triangular-like shape. It has been found that triangular defects can be broadly categorized into two types: triangular defects with no foreign material in the head and triangular defects with foreign material in the head.Triangular defects with no foreign material in the head are the result of growth interruptions that exist between the high-speed growing buffer layer and the low-speed growing epitaxial layer, and triangular defects with foreign material in the head result from substrate contamination or foreign material caused by reaction by-products interfering with step flow growth[9]. Therefore, the main determinants of triangular defects are fluctuations in process conditions and substrate cleanliness. The effect of triangular defects on the reverse leakage characteristics is more pronounced. In addition, the type and location of the triangle defects have different effects on the device, which may cause the diode leakage current to increase, the breakdown voltage to decrease, or even direct failure.

Surface step bunching is a typical morphological feature of crystal growth surfaces, generally aggregated along the <1-100> direction. A number of studies on surface step bunching have been reported. Niu Yingxi et al. believe that step bunching is formed by surface scratches, and geometric constraints are formed at the edge of scratches, forcing the step flow to be blocked and aggregated here [10]. Y. Ishida et al. hold that one reason is that the principle of minimizing surface energy prompts the steps to aggregate in a periodic arrangement [11]. Another reason is that the Schwoebel effect causes the crystal surface atoms to diffuse at the edge of the step when the atomic migration direction is impaired due to the difference in the potential energy of the upper and lower steps, which triggers the phenomenon of asymmetric aggregation of the steps in the etching process. Step bunching triggers poor interface flatness in the semiconductor junction region [4], which results in an abnormal increase in the local electric field strength, leading to a significant drop in the blocking voltage and a significant increase in the leakage current.

"Carrot" defects are one of the main types of surface morphology defects in epitaxial layers. The defect is elongated and linear, and one of the sections is thicker, named for its carrot-like shape, and is generally formed at the epitaxial-substrate interface and during epitaxial growth. The "carrot" defects are mostly transformed by screw dislocations and scratches on the substrate surface. Among several reports investigating "carrot" defects, Okada et al experimentally detected ZrO_2 clusters at the epitaxial-substrate interface. They believe that base stacking faults due to localized stress concentrations are the main cause of the "carrot" defects [12]. In addition, J. Hassan et al detected different shapes of "carrot" defects in the epitaxial layer by different experimental techniques [13]. "Carrot" defects adversely affect the reverse characteristics of Schottky diodes and PN junction diodes at low reverse breakdown voltages [14], decreasing their barrier heights, which leads to an increase in leakage current.

Pit defects are surface pits formed due to Threading Edge Dislocation (TED) and Threading Screw Dislocation (TSD) of the substrate and are a common surface morphology defect. And the size of pit defects formed by TED and TSD in the epitaxial layer is different, in general, the pit formed by TED is much smaller than the pit formed by TSD, so it is easier to observe the pit defects formed by TSD. Jichao Hu et al [15] concluded that pit defects have less effect on the reverse characteristics of the device based on the reverse I-U characteristic plots of JBS diodes with and without pit defects.

3 Defect control technology

In the semiconductor substrate manufacturing process, crystal growth, epitaxy and post-processing are three essential steps. Defects generated in these three links directly affect the performance and yield of the device, so most of the existing research discusses defect control techniques from these three aspects.

3.1 Crystal growth

During crystal growth, most of the defects originate from the seed crystals, so they can be reduced by optimizing the seed crystals and selecting seed crystals with fewer defects. The PVT method is a commonly used technique in the growth of silicon carbide crystals, but the use of this method often produces defects. Dislocations are often found in crystals grown by the PVT method. Currently, the RAF technique (Repeat a-face growth technique) is used, which realizes the dislocation direction conversion by repeating the a-face growth several times, making the dislocations inherited by the regrowth reduced dramatically, thus lowering the density of dislocations, and then finally, the traditional c-face growth is performed to discharge the dislocations. This method significantly reduces dislocation density and inhibits micropipe formation.

Another effective defect control technique is the solution-grown crystal method. Another effective technique for defect control is the solution method of growing crystals. Since the growth characteristics are close to the thermodynamic equilibrium state during the growth of SiC crystals by solution method [16], TSD and TED can be converted to BPD (basal plane dislocation) or SF (stacking fault) through dislocation reaction,

while moving forward along a certain crystallographic direction until they are discharged from the edges of the crystal growth interface, which achieves the purpose of reducing the dislocation density.

The RAF method can reduce the dislocation density by two to three orders of magnitude, making the crystal nearly dislocation-free and suppressing the clustered distribution of micropipes. However, its technological process is complex and requires precise control of temperature, pressure, polarity of seed crystals and impurity doping. Otherwise, it may lead to an increase in defects and high requirements for seed crystals.

The growth process of the solution method is close to the thermodynamic equilibrium state. Due to the dislocation-type transformation during the growth process, the solution method can significantly reduce the crystal defect density and achieve growth with lower dislocations. Compared with the high temperature above 2473K of the physical vapor transport (PVT) method, the growth temperature of the solution method is usually lower than 2173K, which can reduce the defects induced by thermal stress and lower energy consumption at the same time. Of course, the solution method also has some disadvantages. Its growth process requires multiple polishing sessions, with complex procedures and high costs. Meanwhile, the growth rate is low, usually less than 50 μm/h [16].

3.2 Epitaxy

After epitaxy, H_2 and HCl [17] are passed to the substrate and chlorine and hydrogen atoms combine with silicon to form SiHxCly intermediates. Chlorine and hydrogen atoms synergistically combine with silicon atoms at a faster rate than a single hydrogen atom combines with silicon atoms, thus playing a role in etching surface contaminants and subsurface damage layer, optimizing the surface step uniformity, and the formation of volatile chlorides can also be taken away from some of the impurities and defects. Care should also be taken to control the flow rate of HCl to balance the carbon-silicon etching rate and prevent the step flow from being blocked by residual silicon on the surface.

In addition, optimization of epitaxial growth equipment is also an effective way to control defects in the epitaxial stage. Taking the optimized vertical high-speed rotating CVD equipment by Chen Danying and others as an example[18] , it has a vertical structure and a temperature control system to ensure that the gas reaches the reaction surface of the substrate after entering at the optimal C/Si ratio, and at the same time, it can fling out the fallout by rotating the substrate at a high speed. This method is effective in minimizing triangular defects with foreign material in the head caused by dropped objects and particles.

Introducing H_2 and HCl into the substrate can reduce triangular defects, making the steps on the substrate surface more uniform and freer of silicon residue, and reducing the density of triangular defects caused by two-dimensional nucleation (when the HCl flow rate is 100mL/min, the defect density is as low as $0.85cm^{-2}$).

However, when HCl is insufficient, the etching rate of carbon atoms is still higher than that of silicon. Therefore, the residual silicon increases and leads to an increase in

defects. If the HCl content is excessive, the silicon will be etched too quickly, and carbon will accumulate on the surface, which will also increase the defects. In addition, the HCl flow rate must be strictly controlled. Otherwise, it may backfire [17].

During the process of optimizing the epitaxial growth equipment, the vertical hot-wall wafer high-speed rotation CVD epitaxial growth equipment optimized by Chen Danying et al. was able to significantly increase the growth rate up to 56 μm/h. Meanwhile, it successfully achieved mass production of 8-inch SiC epitaxial wafers, resulting in a thickness uniformity of 0.74% and a doping uniformity of 3.70%. However, when thick films (> 50 μm) are grown, the surface roughness and defect density increase slightly, and the process needs to be further optimized [18].

3.3 Post-processing

The post-processing stage, following crystal growth and epitaxy, is the final process of substrate manufacturing. It often uses physical or chemical methods to repair substrate defects. Femtosecond laser processing technology can be used in the post-processing stage [19], because the pulse width of femtosecond laser is extremely short, up to 2.6 femtoseconds, which can make the carrier temperature increase rapidly, while the lattice temperature is almost unchanged, so as to realize the cold processing and avoid the damage caused by hot processing. And because femtosecond laser technology is optical, this non-contact process effectively reduces defects such as scratches, deformation, and sub-surface damage. The use of annealing processing technology can be thermally activated, so that the atoms get enough energy for diffusion and rearrangement, thus indirectly reducing the formation of dislocations and repairing lattice defects, is an effective means of defect control. It is also important to note that different annealing temperatures will affect the warpage of silicon carbide wafers differently [20].

In the femtosecond laser precision processing of silicon carbide materials conducted by Yang Tingkai et al., the ablation threshold prediction error was measured to be low (ablation threshold error ⩽7.5%, width error ⩽7.52%), which is suitable for high-precision processing. Meanwhile, its polishing time is only 28% of that of traditional abrasive polishing, and the stripping time is 33% of that of diamond wire saw cutting. The thickness of the damage layer on its stripped surface (50μm) is much smaller than that cut by diamond wire saw (280μm), so it can effectively reduce the consumption of materials. However, the surface roughness of the stripped 4H-SiC is relatively high (Ra=203nm), and the polishing technology needs to be improved [19].

Annealing processing technology can effectively control the magnitude of thermal stress. Through constraint force compensation mechanism for eutectic bonding stations, the thermal stress is offset, making the average stress only 32MPa, and it can indirectly reduce the formation of dislocations. At the same time, it can maintain a high bonding strength and meet the requirements of subsequent processes. However, the entire process involves many steps (oxidation, plasma activation, cleaning, and stepwise annealing), and the annealing process requires precise control of temperature and pressure, with strict requirements for equipment accuracy [20]

4 Conclusion

SiC, as a representative wide-bandwidth semiconductor, is widely used in semiconductor substrate manufacturing. In this paper, internal crystal defects and surface and near-surface defects are studied in depth with SiC as the core, and the formation mechanism of these defects is described, and based on the formation mechanism of the defects, the impacts caused by them on the devices are analyzed. In addition, different defect control techniques are systematically introduced from three aspects: crystal growth, epitaxy and post-processing during semiconductor substrate manufacturing. Finally, different kinds of defect control techniques in each process step are compared and the advantages and disadvantages are analyzed, so as to propose the potential application scenarios of various defect control techniques, which provide theoretical references for the defect control of semiconductors. This paper argues that in the future, defects can be reduced and avoided by systematically optimizing the process equipment in such a way that the process equipment during substrate manufacturing can accurately regulate the various factors affecting the growth rate and the formation of defects, such as the growth temperature and the flow rate of the pass-through gas. The combination of the above defect control techniques can effectively reduce substrate defects to a certain extent, improve the performance and parameters of power devices, and promote the development of the semiconductor industry and the electrical and electronic fields.

Authors Contribution. All the authors contributed equally and their names were listed in alphabetical order.

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