Research on Digital Circuit Teaching Practice Based on EDA Technology Taking the Design of 7-Segment Display Decoder and 2-Bit Adder as Examples

Guozeng Wu[a], Naochang Cao[*]

School of Electronic and Information Engineering, Guangzhou City University of Technology, Guangzhou, China

[a]414183864@qq.com, [*]1114891562@qq.com

Abstract. This paper takes EDA (Electronic Design Automation) technology as the core and, through the design practices of a 7-segment display decoder and a 2-bit adder, explores a new teaching model for digital circuits. By introducing EDA tools, students can gain a more intuitive understanding of the working principles of digital circuits, enhancing their practical abilities and innovative thinking. The research findings indicate that EDA technology offers significant advantages in digital circuit teaching, effectively improving students' design efficiency and circuit performance.

Keywords: EDA technology; digital circuit teaching; 7-segment display decoder; 2-bit adder; practical research

1 Introduction

With the rapid advancement of electronic technology in recent years, digital circuit design has emerged as a pivotal course in disciplines such as electronic engineering, computer science and technology, and related fields. This course plays a crucial role in equipping students with the fundamental knowledge and skills required for modern electronic system development[1-2]. However, traditional teaching methods in digital circuits have often placed a heavy emphasis on theoretical explanations, while neglecting the essential practical components. This imbalance has resulted in a significant challenge for students, who frequently find it difficult to bridge the gap between theoretical concepts and their practical application in real-world design scenarios.The advent of EDA (Electronic Design Automation) technology has introduced a transformative approach to digital circuit teaching, offering innovative strategies and tools to overcome these limitations. EDA technology leverages sophisticated software tools to facilitate the modeling, design, verification, and implementation of electronic systems[3-4]. By utilizing these tools, students can engage in a more hands-on learning experience, enabling them to visualize and interact with digital circuits in a virtual environment. This not only enhances their understanding of complex circuit behaviors but also significantly improves design efficiency and reduces overall design costs.In this context, this

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paper presents a comprehensive practical research study on digital circuit teaching based on EDA technology, using the design of a 7-segment display decoder and a 2-bit adder as illustrative examples. The 7-segment display decoder is a fundamental component in various digital display systems, converting binary-coded decimal (BCD) inputs into signals that drive the segments of a 7-segment display to show decimal digits. On the other hand, the 2-bit adder serves as a basic building block in arithmetic logic units (ALUs), performing addition operations on binary numbers. By focusing on these two specific designs, the study aims to provide students with a solid foundation in digital circuit design principles while also exposing them to the practical applications of EDA tools.Throughout the research, students are guided through the entire design process, from initial concept formulation to final circuit implementation and verification. They learn how to use EDA software to create circuit schematics, simulate circuit behavior under different conditions, and optimize designs for performance and efficiency. Additionally, the study emphasizes the importance of critical thinking and problem-solving skills, encouraging students to explore alternative design approaches and troubleshoot potential issues that may arise during the design process.This practical research study demonstrates the significant advantages of incorporating EDA technology into digital circuit teaching. By providing students with a more engaging and interactive learning experience, EDA-based teaching methods not only enhance their understanding of digital circuit design but also prepare them for the challenges and opportunities that lie ahead in their future careers as electronic engineers or computer scientists[5-6].

2 An Overview of EDA Technology

2.1 Definition and Development of EDA Technology

EDA (Electronic Design Automation) technology refers to the technology that utilizes computer-aided design software to automate the design process of very-large-scale integrated circuits (VLSI) and related electronic systems. It originated from the development of computers and semiconductor technologies in the latter half of the 20th century, undergoing a transformation from manual design to automated design. With the rapid expansion of integrated circuit scales, EDA technology has gradually become an indispensable core supporting technology for electronic design, earning the reputation as the "mother of chips."

2.2 Characteristics of EDA Technology

EDA technology boasts several notable characteristics:

Software-Based Design Approach: Designers can independently complete various design stages through design input methods such as waveforms, schematic diagrams, and VHDL (VHSIC Hardware Description Language), without the need for hardware equipment.

Automated Design Process: EDA tools are capable of automatically performing processes such as logic simplification, partitioning, synthesis, placement and routing, as well as logic optimization and simulation testing.

High Design Efficiency: By leveraging advanced hardware description languages and IP (Intellectual Property) cores, designers can swiftly complete the design and verification of complex circuits.

2.3 Application of EDA Technology in Digital Circuit Teaching

In digital circuit teaching, EDA technology provides a virtual experimental environment, enabling students to complete circuit design, simulation, and verification on computers. This not only reduces experimental costs but also enhances students' design capabilities and innovative thinking. By introducing EDA technology, students can gain a more intuitive understanding of the working principles of digital circuits and master the methods and techniques of circuit design.

3 Design Practice of a 7-Segment Display Decode

3.1 Principle of the 7-Segment Display Decoder

The 7-segment display decoder is a commonly used electronic display device for showing digits (0-9) and some letters (such as A, b, C, d, E, F). It consists of seven independent luminous segments (usually LED light-emitting diodes) arranged in an "8"-shaped pattern. By lighting up different combinations of segments, various digits or characters can be displayed. The decoder receives a set of binary input codes (such as 4-bit BCD codes) and, based on this input, selects a specific output line among its multiple output lines to be set to an active state, thereby driving the corresponding segments on the 7-segment display to turn on or off.

3.2 Design of the 7-Segment Display Decoder Based on EDA Technology

This design adopts Quartus Prime 18.1 as the development environment and uses VHDL for circuit description. Quartus Prime 18.1 is a powerful EDA tool that supports the entire process from circuit design to simulation verification.The truth table for the 7-segment decoder is shown in Table 1.

Table 1. Truth Table for the 7-Segment Decoder

Input Code	Input Code	Displayed Data
0000	1000000	0
0001	1111001	1
0010	0100100	2
0011	0110000	3
0100	0011001	4
0101	0010010	5
0110	0000010	6
0111	1111000	7

1000	0000000	8
1001	0010000	9
1010	0001000	A
1011	0000011	B
1100	1000110	C
1101	0100001	D
1110	0000110	E
1111	0001110	F

This design implements a 7-segment display decoder using VHDL. The 4-bit BCD input A is mapped to a 7-bit LED7S output via a CASE statement, driving the 7-segment LED to display corresponding digits or characters (e.g., "0000" → "1000000" for "0"). The B port remains permanently low. The algorithm employs a lookup table method: pre-storing segment codes for 16 input combinations and directly outputting results through conditional checks. The code features a clear structure and concise logic, enabling efficient automatic synthesis and simulation verification via EDA tools, demonstrating the scalability and effectiveness of digital circuit design. The VHDL description of the decoder is as follows:

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY DECL7S IS
  PORT(A : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
       B : OUT STD_LOGIC;
       LED7S : OUT STD_LOGIC_VECTOR(6 DOWNTO 0));
END;
ARCHITECTURE ONE OF DECL7S IS
BEGIN
  PROCESS(A)
BEGIN
   CASE A IS
     WHEN "0000" => LED7S <= "1000000";
     WHEN "0001" => LED7S <= "1111001";
     WHEN "0010" => LED7S <= "0100100";
     WHEN "0011" => LED7S <= "0110000";
     WHEN "0100" => LED7S <= "0011001";
     WHEN "0101" => LED7S <= "0010010";
     WHEN "0110" => LED7S <= "0000010";
     WHEN "0111" => LED7S <= "1111000";
     WHEN "1000" => LED7S <= "0000000";
     WHEN "1001" => LED7S <= "0010000";
     WHEN "1010" => LED7S <= "0001000";
     WHEN "1011" => LED7S <= "0000011";
     WHEN "1100" => LED7S <= "1000110";
     WHEN "1101" => LED7S <= "0100001";
     WHEN "1110" => LED7S <= "0000110";
```

```
    WHEN "1111" => LED7S <= "0001110";
    WHEN OTHERS => NULL;
  END CASE;
END PROCESS;
B <= '0';
END;
```

After successfully compiling the developed code, conduct simulation to obtain the timing diagram as shown in Figure 1.

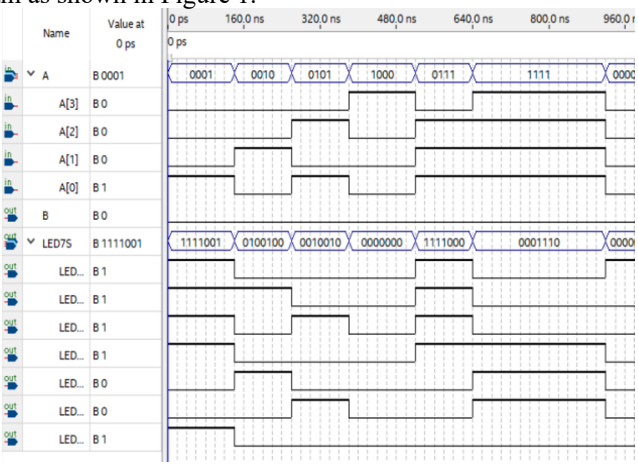

Fig. 1. Simulation Diagram

By analyzing the simulation logic timing diagram, it is confirmed that the design requirements are met. Next, configure the pin mappings between the chip and the program's input/output ports, followed by downloading the program for testing and verification.The pin configuration is shown in Figure 2.

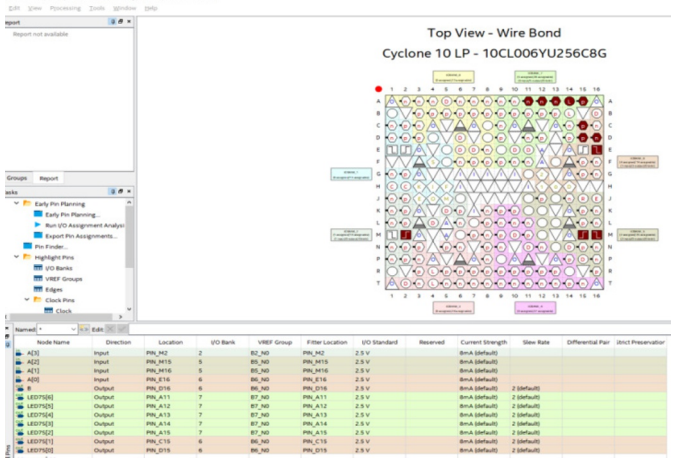

Fig. 2. The pin configuration

On the experimental board, the positions of switches SW1-SW4 are arranged from left to right, representing the low to high order of hexadecimal digits. When a switch is flipped upward, it corresponds to a binary '1'; when flipped downward, it corresponds to '0'. These four switches collectively represent a 4-bit binary number, with the seven-segment display providing real-time display of the corresponding hexadecimal value. As shown in Figure 3, when all switches (SW1-SW4) are in the downward position, indicating "0000", the decoder outputs "1000000", causing segments a-f of the seven-segment display to illuminate and show the digit "0".

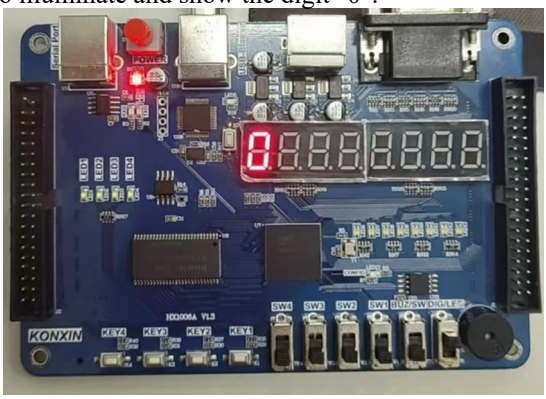

Fig. 3. Download the test diagram

Through simulation verification, the 7-segment display decoder can correctly display digits from 0 to 9, confirming the correctness of the design. Compared with traditional hardware experiments, the design method based on EDA technology offers greater flexibility and repeatability, significantly reducing experimental costs.

4 Design Practice of a 2-Bit Adder

4.1 The Principle of a 2-Bit Adder

Principle of a half adder: A half adder is a logic circuit that adds two single-bit binary numbers, producing a sum and a carry. It serves as the fundamental building block for constructing full adders. The logical expressions for a half adder are:

Sum (S) = $A \oplus B$

Carry (C) = $A \cdot B$

In Quartus Prime 18.1, the circuit schematic of a half adder can be implemented using basic logic gates such as AND gates, NOT gates, and XOR gates. For example, an AND gate is used to generate the carry output, while a NOT gate combined with an XOR gate produces the sum output.Composition of a 2-bit full adder: A 2-bit full adder can be constructed by connecting two half adders and an OR gate. Specifically, the LSB half adder adds the inputs A0 and B0, generating the LSB sum (S0) and carry (C0). The carry C0 then serves as the carry-in for the MSB half adder, which adds A1, B1, and C0 to produce the MSB sum (S1) and an intermediate carry (C1). Finally, the carry outputs C0

and C1 from the two half adders are combined using an OR gate to produce the final carry-out (Cout).

4.2 Schematic Design of a 2-Bit Adder

This design adopts a schematic-based drawing approach, accurately connecting the invoked components according to the logical functionality of a full adder to create a complete 2-bit full adder schematic. It thoroughly considers complex logical relationships such as carry propagation to ensure the correctness of the circuit structure. If employing a bottom-up design methodology, the process involves first designing foundational modules like half adders, followed by constructing higher-level modules (e.g., full adders) by invoking these lower-level modules. This requires correctly generating and utilizing custom module symbols to achieve a hierarchical circuit design.

The half-adder circuit design is shown in Figure 4.

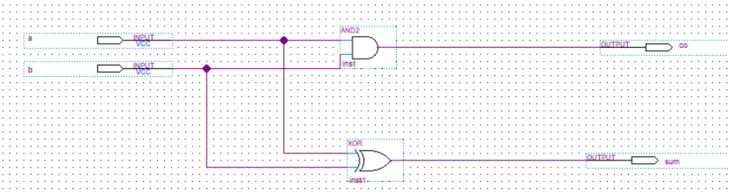

Fig. 4. Half Adder Schematic Diagram

The full-adder circuit design is shown in Figure 5.

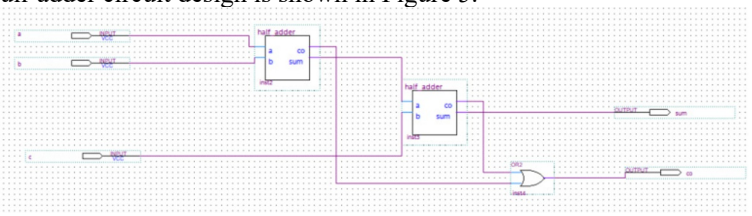

Fig. 5. Full Adder Schematic Diagram

The 2-bit adder circuit is depicted in Figure 6.

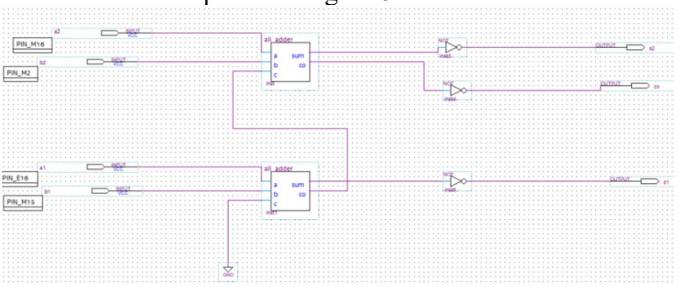

Fig. 6. 2-Bit Adder Schematic Diagram

The timing diagram of the 2-bit adder simulation is shown in Figure 7. By analyzing the timing diagram, it is confirmed that the design requirements are met, followed by pin configuration as depicted in Figure 8.

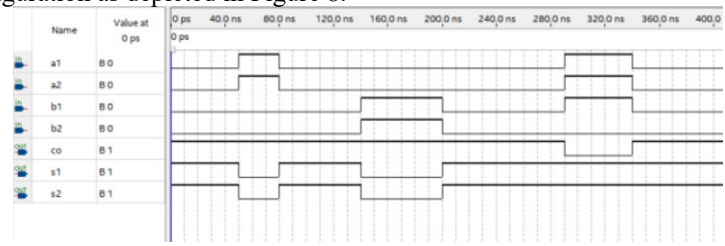

Fig. 7. 2-bit Adder Simulation Diagram

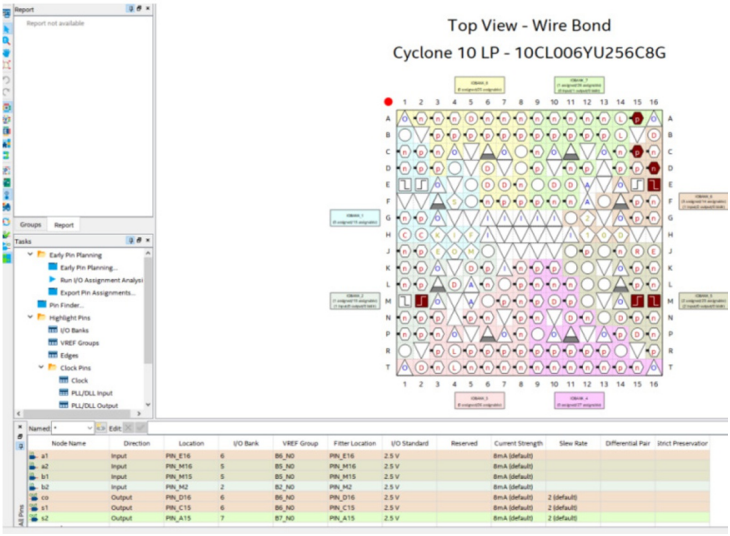

Fig. 8. Download the test diagram

Based on the pin configuration, the three upper LEDs correspond as follows: the leftmost green LED represents the highest carry-out (CO), the middle red LED represents the lower-order sum bit (S1), and the rightmost red LED represents the higher-order sum bit (S2). When switches SW2-SW4 are all flipped upward, it indicates that a2, b1, and b2 are set to 1, where b1 is the lower-order bit, while a2 and b2 are higher-order bits.From the pin assignments, the left green LED signifies the highest carry-out, and the middle red LED (S1) corresponds to the lower-order sum. Since the lower-order bit b1 = 1 and b0 = 0, their sum equals 1, causing the middle red LED (S1) to illuminate. Meanwhile, both a2 and b2 are 1, and their sum equals 2 (binary 10), generating a carry-out of 1. Thus, the green carry-out LED lights up, while the right red LED (S2) remains off because the higher-order sum bit is 0 in this case.The download test process is illustrated in Figure 9.

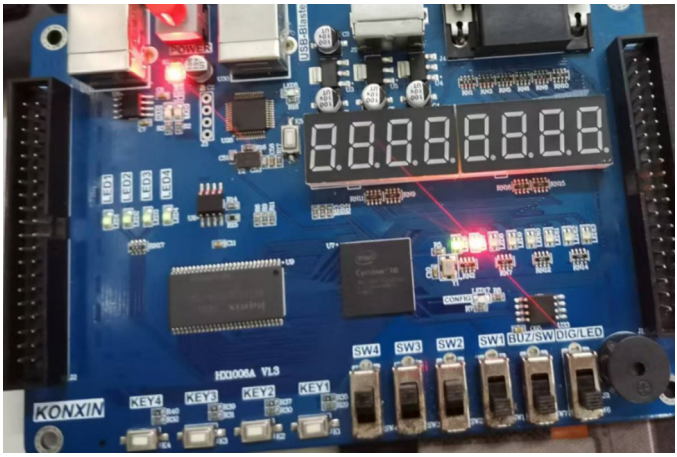

Fig. 9. Download the test diagram

By analyzing the actual measurement results of the download test, it can be observed that the circuit design meets the design requirements.

After introducing VHDL language design by understanding students' learning conditions, students have gained a deeper understanding and improvement in the logicality of digital circuits.

5 Conclusion

EDA technology significantly enhances design efficiency through its automated design process. Designers can swiftly complete circuit design, simulation, and verification using software tools, reducing the time and errors associated with manual design. Traditional digital circuit experiments require a large amount of hardware equipment and experimental materials, resulting in high costs. In contrast, the virtual experimental environment based on EDA technology can significantly reduce experimental expenses, enabling students to complete circuit design and verification on computers. By introducing EDA technology, students can gain a more intuitive understanding of the working principles of digital circuits and master the methods and techniques of circuit design. The virtual experimental environment offers more practical opportunities, allowing students to continuously improve their design capabilities and innovative thinking through hands-on practice. EDA technology provides new ideas and methods for digital circuit teaching. Teachers can design more virtual experimental projects by introducing EDA tools, stimulating students' interest and enthusiasm for learning. Meanwhile, EDA technology also supports remote teaching and online learning, offering more possibilities for digital circuit instruction.This paper takes the design of a 7-segment display decoder and a 2-bit adder as examples to explore the practical research on digital circuit teaching based on EDA technology. The research results indicate that EDA technology has significant advantages in digital circuit teaching, substantially improving design

efficiency, reducing experimental costs, enhancing students' practical abilities, and promoting teaching innovation. In the future, with the continuous development and refinement of EDA technology, its application in digital circuit teaching will become more extensive and in-depth. We can further explore the application of EDA technology in complex digital system design, embedded system design, and other fields, providing more support and assistance for the teaching of majors such as electronic engineering and computer science and technology.

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