SST-Aware 11-Level Multilevel Converter PIDD2 Control Tuned via Hybrid Metaheuristic Optimization

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Abstract. The increasing demand for high-efficiency power conversion in grid-connected systems has driven the development of advanced converter architectures. This paper proposes a novel grid-integrated power enhancement framework based on an 11-level cascaded H-bridge converter integrated with a Solid-State Transformer (SST)-aware -aware multi-level converter. The system is designed to address critical challenges, including voltage regulation, harmonic suppression, power factor correction, and dynamic stability, in high-power applications. A hybrid metaheuristic optimization strategy combining the Golden Eagle Optimizer (GEO) and Firefly Algorithm (FA) is employed to fine-tune the converter parameters for improved efficiency, reduced power losses, and optimal control response. A Proportional-Integral-Derivative Double Derivative (PIDD2) controller is incorporated to ensure robust load balancing and transient stability under varying load conditions. MATLAB/Simulink-based simulations validate the proposed system's effectiveness in maintaining low Total Harmonic Distortion (THD), improved power factor, and enhanced voltage quality, demonstrating its suitability for modern grid-interfaced power conversion systems.

Keywords: PIDD2 controller, EV, Metaheuristic optimization, SST.

1 Introduction

Solid-state transformers (SSTs) are transformers that exclusively use solid-state technology to achieve what conventional transformers have done in terms of cutting costs [1]. SSTs offer functionality, efficiency, and size. SST based on multilevel converters can produce efficient voltage regulation and flow control, in conjunction with benefits such as better performance, reduced harmonics, modularity, and larger-scale design options for high voltage processes [3]. In addition to these benefits, utilizing sophisticated control techniques like integral-proportional-Resonant (PIR) and MPC (Model Predictive Control) offers the further advantage of reducing circulating current and balancing capacitor voltages. Energy-based control leveraging common-mode currents provides avenues for improving stability and reducing, in particular, sub-

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synchronous instability. The high-frequency switch control will not only allow for a compact build but will also improve its efficiency [4].

SST multilevel converters are advantageous over conventional multilevel systems, but together with a complete control system, they also present a number of disadvantages. The first is the complexity, size, and power loss associated with the general necessity to have full power processing [5]. Complexity in modelling and control of these devices arises because of the large number of submodules and capacitor voltage balancing [7]. For cascaded H-bridge (CHB) cases, power imbalances between the DC-link in each cell led to threats of grid current distortion as well as stability implications associated with voltage [8].

A hybrid metaheuristic-optimized repetitive control virtual impedance is applied to SST multilevel converters, addressing asymmetric capacitance effects, minimizing circulating harmonics, and enhancing dynamic stability [6], to and MPC, or Model Predictive Control technique for MMC-based DC/DC SST systems, making it possible to decouple converter dynamics and optimize independent cost functions [9]. A Hybrid Low Capacitance MMC horizontal connections between submodules were used to minimize voltage rippling while operating under low frequencies [11]. The combined mode currents were used to provide a decoupled energy control as well as minimize sub-synchronous oscillations, thus maximizing reliability and efficiency.

The motivation of this research is rooted in the increasing need for high-efficiency and high-reliability power conversion in today's grid-connected systems [10]. Standard converters often face challenges in voltage regulation, harmonics suppression, and power factor correction. The study modernizes the standard approach identified in industry, utilising an 11-level cascaded H-bridge presents the consideration of SST [2]. Applying a PIDD2 controller, the stability of the system is improved along with load balancing. Fine-tuning of the system parameters is accomplished via a hybrid optimization approach combining GEO and FA, resulting in reduced power losses and control performance improvements.

2 Literature Surveys

Some of the recent existing works related to our work are reviewed in this section.
In 2023, Patel et.al., presented a three-stage Field-oriented controlled (FOC) induction motor drive fed by a solid-state transformer (SST) for use in high-frequency applications like marine propulsion systems. Si-IGBT and Sic devices are used in the SST-fed drive to reduce expenses and electrical losses. Based on a Si-IGBT-based Cascaded H-Bridge (CHB) inverter coupled in series with a Sic-based 2L-VSI, the authors suggest a novel hybrid modulation approach for the MV stage. The stator frequency is used to switch the CHB inverter. to provide the necessary voltage [1].

In 2024, Siemaszko & Carpita determined that Medium-voltage DC (MVDC) technology is becoming popular because power electronics devices dominate many

grids. However, developing a detailed simulated MVDC grid that consists of numerous connected devices can take a lot of time. Continuous-time model simulation is beneficial for developing system-level control models. This paper describes a case study of obtaining continuous-time modelling of a +/−10 kV MVDC grid that incorporates an SST and a modular multilevel converter-based active front end. It also provides some educational content about continuous-time simulation [2].

In 2023, Nardoto et.al., presented that the SST offers a lot of advantages for new power systems to make a great technology. The advantages include smaller weight and volume, compensation for power factor, precise control of output voltage, limited harmonics, limited current in a short circuit, and immunity to voltage dip. This study investigates and analyzes an entire SST Model Predictive Control (MPC) strategy regarding its performance during power system transients [3].

In 2023, Motwani et.al., proposed three new hybrid-MMC (HMMC) for high-AC/low-DC voltage operating regimes in electric cars and energy storage systems. The new hybrid-MMCs generate multilayer AC voltage using fast-switching, low-voltage (LV) switch-based submodules and low-frequency, high-voltage (HV) switches. for efficient operation with lower submodule capacitance values. The HMMC solutions also consider practicalities affecting the development and roll-out of commercial solutions, such as snubber and DC split capacitor requirements [4].

In 2023, Hassanifar et.al., examined that the modular multilevel converter (MMC) is a promising topology for hybrid grids such as medium and low-voltage AC and DC grids. In MVDC applications for an AC-DC hybrid grid, MMCs provide the capability to break the DC and operate in buck mode. MMCs may be employed as a front-end bidirectional AC-DC converter or a DC-DC converter, providing potential for different levels of LVDC and realizing SSTs in the form of hybrid grids [5].

In 2022, López-Rodríguez et.al., proposed that Power semiconductor devices have evolved into SSTs that enable the connection of energy storage, renewable energy, and distributed generation to the current electrical infrastructure. A dual active bridge (DAB), which permits bidirectional power flow, is the basic building block of SSTs. In order to control power flow in a DAB while guaranteeing system stability, preserving passive characteristics, and simplifying PI controller performance and robustness, this work suggests a current control strategy based on PI passivity [6].

In 2022, Malik et.al., presented a new SST using topology for hybrid microgrids at a quantity scoped at medium voltage and low graduations of low voltage. The Modes of control are established, and self-sufficient power sharing diagram for Regulation of AC frequency and DC voltage. The proposed topology supports AD and DC interconnections across different levels of voltage and frequency and helps lower the cost of the system while also establishing electrical isolation [7].

In 2024, Marca et.al., proposed that Modular multilevel converters provide non-linear ac voltage waveforms and therefore can save costs and footprint in certain electric vehicle battery charging applications. Full-bridge submodules will facilitate

single-stage AC/DC conversion, contributing to efficiency and power density maximization. This paper discusses and models a modular multilevel converter topology, proposes a single control scheme to output voltage waveforms, and demonstrates that it is appropriate for a high-power bidirectional battery charger application [8].

In 2023, Ke et.al., suggested a novel multimodal attention fusion (MAF) model for high voltage direct current (HVDC) transmission projects in order to diagnose faults in modular multilevel converters (MMCs). The suggested model transforms three-phase internal circulating currents into two-dimensional time-frequency images, paying attention to discriminative regions of the image containing information about the fault features, and exploiting intrinsic relationship between time series and visual characteristics to facilitate a combined fault feature extraction process [9].

In 2023, Jiang et.al., proposed that the modular multilevel converter (MMC) is challenged by substantial circulating currents, leading to increased overall losses and making the design of the heat-sink complicated. Conventional controllers are sensitive to parameters and model uncertainties, while model predictive control (MPC) enables simple design and better robustness but struggles when it comes to tuning weighting factors. This paper discusses using a hybrid control approach using the MPPIC method, which has no complex mathematical operations, is easier to implement, and reduces the circulating currents for all modulation ratios. Table 1 shows the aim, method, and findings from the existing works. Table 1 shows the Review of the existing works [10].

2.1 Research Gap

The exciting possibilities of the SST technology and Modular Multilevel Converter (MMC) control techniques are being considered in applications such as electric transportation, renewable energy systems, and hybrid microgrids. The current SST architectures include a hierarchy of devices that comprise the CHB inverter, DAB, and MMC topologies, a range of methods of control like Field-Oriented Control, PI control, passivity, and Model Predictive Control. These strategies still have their limitations in terms of multivariable tuning, transient response, and robustness to disturbances. To overcome these issues, the researcher focuses on using new hybrid topologies and high-frequency switching components that incorporate innovative control techniques to help reduce circulating currents and energy imbalances while improving fault detection and resilience. The future of a scalable and modular SST architecture that offers low-cost, compact, and advanced bidirectional energy capability is promising for practical implementation in the smart grid, electric transport, and energy storage systems.

3 Proposed Methodology

The proposed methodology consists of algorithms in an 11-level multilevel converter. The converter architecture layer improves modularity and scalability, while the control layer implements a PIDD2 controller for stability and responsiveness. The optimization layer uses a hybrid Golden Eagle Optimizer and Firefly Algorithm to minimize switching losses and reduce harmonic distortion. The integration layer links optimized control converter hardware for interoperability and power factor correction. The validation and performance layer conducts simulations to measure system reliability and efficiency. Fig. 1 shows the block diagram for SST.

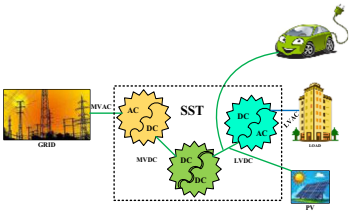

Fig. 1. Block diagram for SST

3.1 System Architecture and Modeling

The proposed framework uses Solid-State Transformer (SST) modules and 11-level medium-voltage cascaded H-bridge multilevel converter grid applications. It aims for high conversion efficiency, modular scalability, and galvanic isolation. The converter provides fine voltage steps, reduces switching stress, and improves harmonic performance. Every H-bridge cell makes a contribution. a discrete voltage level.

$$\boldsymbol{V_{out}(t)} = \sum_{i=1}^{N} \boldsymbol{V_{dc,i}} \cdot \boldsymbol{S_i(t)} \quad (1)$$

Where $\boldsymbol{V_{dc,i}}$ is the DC connection voltage of the i[th] H-bridge cell, $\boldsymbol{S_i(t)}$ represents the switching function, and N is the number of cascade cells in each phase. Embedding SST modules in this topology enables adaptive.

The voltage of the DC-link of an H-bridge cell is determined by the number of cascaded cells per phase, the switching function, and the number of cascaded cells. The presence of SST modules ensures voltage adaptability and redundancy, using a high-frequency transformer and series and shunt converters.

A switching function-based model is proposed to represent system dynamics by connecting discrete switching states from H-bridge cells to output voltage and current waveforms. This modeling helps represent nonlinear relationships between voltage

regulation, current harmonics, and power factor, providing a mathematical framework for controller and optimizer development

.

$$S_i(t) = \begin{cases} +1, & \textit{if upper switch is ON, lower is OFF} \\ -1, & \textit{if upper switch is OFF, lower is ON} \end{cases} \quad (2)$$

The phase voltage becomes, $v_{ph}(t) = \sum_{i=1}^{N} \frac{V_{dc,i}}{2} . S_i(t)$

Enable the symbols for the synthesis 11-level waveform reduced harmonic content. The grid side current dynamics are described.

$$L\frac{di(t)}{dt} + R_i(t) = v_{ph} - v_{grid}(t) \quad (3)$$

Where L and R represent the filter inductance and resistance, ensuring smooth current injection into the grid.

The model scenario includes constraints for stability and compliance with grid code requirements, allowing unperturbed current injection into the grid. These constraints support tuning and optimization of the controller, ensuring operations remain within limits due to load and grid variation.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \times 100\% \leq 3\% \quad (4)$$

Where I_n denotes the nth harmonic element of the current and I_n is the fundamental current.

The SST-aware 11-level converter uses a multi-layered architecture and mathematical models to achieve equal voltage stress sharing throughout each cell cascaded. It also has switching stress limits to protect against semiconductor overvoltage and overcurrent limits. The converter provides a robust analytical framework for effective controller optimization, improved harmonic mitigation, and safe grid integration. Fig. 2 shows the architecture for the proposed methodology.

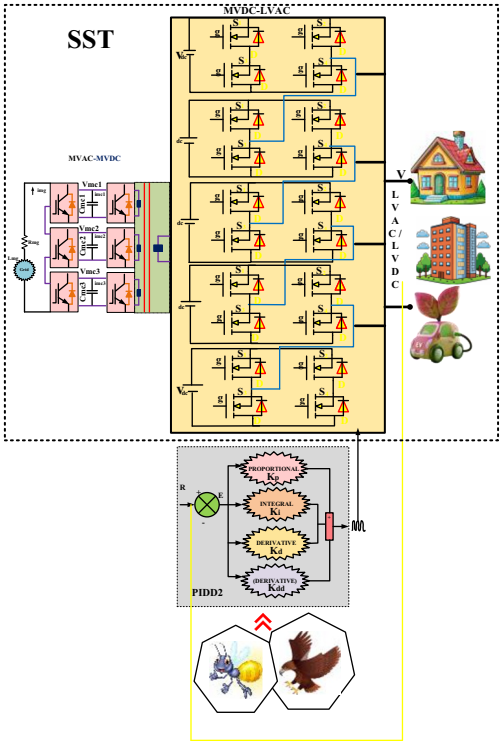

Fig. 2. Architecture for SST

SSTs, or solid-state transformers, are a new electrical power device that could swap out low-frequency transformers in modern grid use. SSTs replace the iron core of conventional transformers with high-frequency power converters and smaller high-frequency transformers, making them smaller, lighter, and more flexible. They correct power factor, filter harmonics, and provide precise voltage and frequency regulation. SSTs are useful for adding renewable energy sources and modern DC loads onto existing AC grids. They involve three major steps: converting high-voltage grid AC electrical energy to high-voltage DC, converting DC to high-frequency AC, and converting the output back to the required voltage and frequency for the final electrical load. This technology is essential for smarter, more resilient, and highly efficient power grids. Fig.3 shows structure for PIDD2 controller.

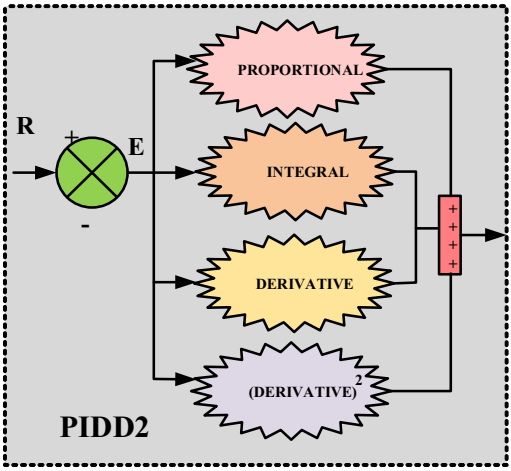

Fig. 3. Structure for PIDD2 controller

The adaptive framework for PIDD2 combines fast transient management and long-term optimization, ensuring grid codes meet THD < 3% and near-unity power factor while maintaining system stability and resilience to uncertainty.

3.3 Firefly Algorithm (FA)

FA is based on flashing and attraction behavior ↓ 'reflies, where brightness presents fitness. Fireflies move toward brighter individuals while maintaining stochastic diversity:
Attractiveness Function:
The attraction between fireflies $\boldsymbol{i}$ and $\boldsymbol{j}$:

$$\boldsymbol{\beta}(\boldsymbol{r}_{ij}) = \boldsymbol{\beta}_0 \boldsymbol{e}^{-\gamma r_{ij}^2} \quad (5)$$

Where $\boldsymbol{\beta}_0$ is maximum attractiveness, $\boldsymbol{\gamma}$ is the absorption coefficient, $\boldsymbol{r}_{i,j}$ is Euclidean distance.

Brightness (Fitness):

Brightness $\boldsymbol{I}$, of firelly $\boldsymbol{i}$ is proportional to its fitness value:

$$\boldsymbol{I}_i \propto \boldsymbol{f}(\boldsymbol{x}_i) \quad (6)$$

Movement Rule

Firefly $\boldsymbol{i}$ approaches a firefly that is brighter. $\boldsymbol{j}$

$$x_i^{t+1} = x_i^t + \beta_0 e^{-\gamma r_{i,j}^2}\left(x_j^t - x_i^t\right) + \alpha \cdot \varepsilon_i^t \quad (7)$$

The proposed hybrid framework integrates GEO's exploration strength and FAs' exploitation ability to optimize converter and PIID2 control parameters.

4 Results and Discussion

The study developed a new grid-connected power enhancement system, such as an 11-level cascaded H-bridge converter and a hybrid GEO-FA algorithm. The system outperformed conventional multilevel topologies and single algorithm optimization methods in various metrics. The optimized PIDD² controller was the most affected component. The system delivers reliability, stability, and improved power quality for sustainable grid-interfaced renewable energy and industrial use cases. Fig.4 displays the Simulink diagram.

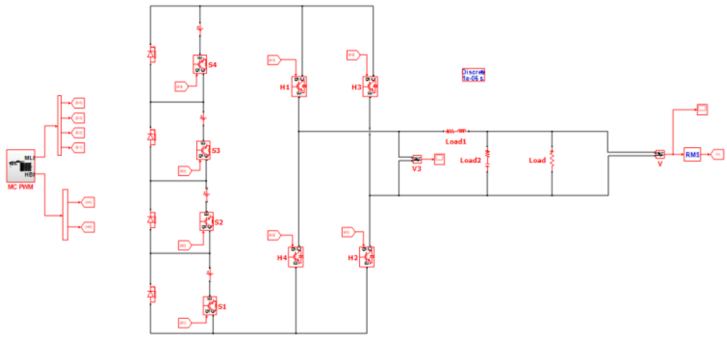

Fig. 4. Simulink diagram

4.1 Performance Evaluation

The performance evaluation of the SST-integrated multilevel converter, a GEO-FA-optimized PIDD² controller, compares it to various topologies and algorithms. The findings indicate that the proposed model outperforms all baseline architectures in every performance metric, indicating high power quality utility and stable performance. The comprehensive ablation study demonstrates the effectiveness, efficiency, and reliability of the proposed framework for grid-connected power conversion applications. Table 1 shows the Performance Comparison of Different Multilevel Converter Topologies

Table 1. Performance Comparison of Different Multilevel Converter Topologies

Topology	THD (%) ↓	Power Factor ↑	Efficiency (%) ↑	Switching Loss ↓ (W)	Voltage Ripple ↓ (V)	Switching Frequency (kHz)
NPC	5.5	0.94	95.2	210	2.5	5.4
FC-MLC	4.8	0.96	96.1	180	2.1	5.32
CHB	3.3	0.97	97.3	160	1.8	5.3
ANPC	2.7	0.985	97.9	140	1.5	5.1
Proposed	1.1	0.995	98.8	110	1	5

Table 1 demonstrates that the converter developed in this project yields the best performance overall among the other topologies compared in this work. Therefore, it is easily observed that the NPC, FC-MLC, CHB, and ANPC all have gradually decreased THD from 5.5% to 2.7% efficiency from 95.2% to 97.9%, while the proposed system had an even lower THD of 1.1% and an even higher efficiency level of 98.8%. Secondly, it also possessed the highest power factor of 0.995, while also having the lowest switching losses of 110 W and voltage ripple of 1 V. In the first trial, the proposed system produced these results at a switching frequency of ~5 kHz, which outperformed all other configurations that are able to produce comparable results.

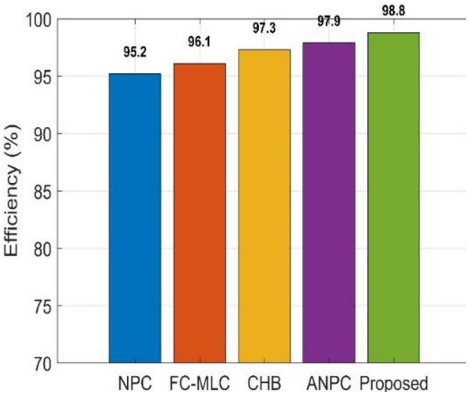

Fig. 5. Efficiency comparision of Convereter Topologies

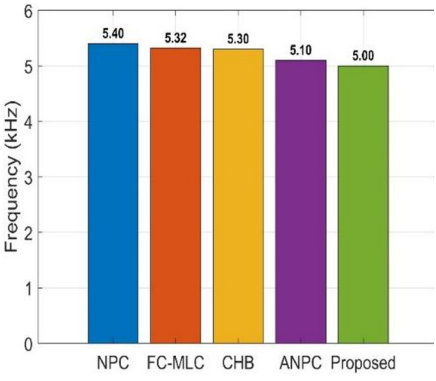

Fig. 6. Switching Frequency Comparison of Converter Topologies

Fig.5 depicts the efficiency comparison of various multilevel converter topologies. The proposed system achieved the highest efficiency of 98.8% against NPC, FC-MLC, CHB, and ANPC topologies of 95.2%, 96.1%, 97.3%, and 97.9% respectively. The

switching frequencies corresponding to the analysis are presented in Fig 6. The proposed system has the lowest switching frequency (5 kHz) among all other multilevel converter topologies.

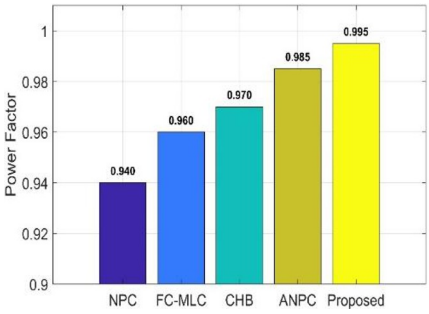

Fig. 7. Power Factor Comparison of Converter Topologies

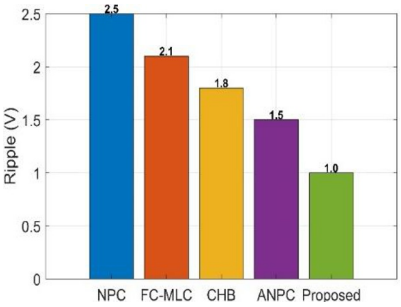

Fig. 8. Voltage Ripple Comparison of Converter Topologies

In Fig. 7, we see the comparison of the power factor between converter topologies, the proposed system giving the best value of 0.995, which is an improvement over NPC (0.94), FC-MLC (0.96), CHB (0.97), and ANPC (0.985). In Fig. 8, we see the comparison in voltage ripple performance; the proposed converter had a voltage ripple of only 1.0 V, compared to 2.5 V in NPC, 2.1 V in FC-MLC, 1.8 V in CHB, and 1.5 V in ANPC, showing its better voltage quality.

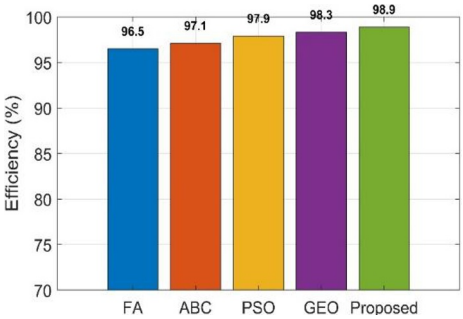

Fig. 9. Efficiency comparison of optimization algorithms

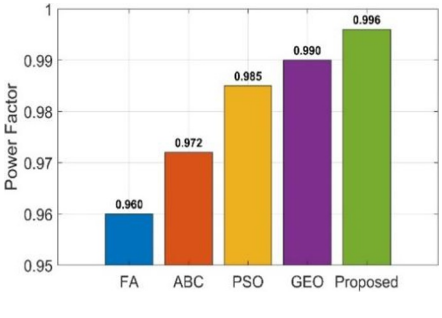

Fig. 10. Power factor comparison of optimization algorithm

Fig. 9 illustrates the efficiency comparison of optimization algorithms, where the proposed method achieves the highest efficiency of 98.9%, outperforming FA (96.5%), ABC (97.1%), PSO (97.9%), and GEO (98.3%). Fig. 10 shows the corresponding power factor performance, the proposed approach again leading at 0.996, compared to FA (0.960), ABC (0.972), PSO (0.985), and GEO (0.990), confirming its superiority in both efficiency and power quality.

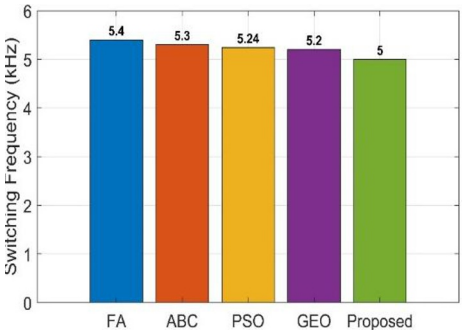

Fig. 11. Switching Frequency comparison of optimization algorithms

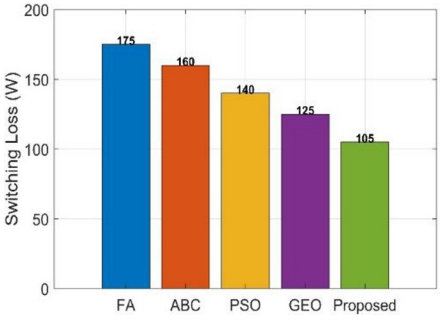

Fig. 12. Switching Loss comparison of optimization algorithms

Fig. 11 presents the performance of the suggested algorithm when used at the lowest switching frequency of 5kHz, just below the values from FA (5.4 kHz), ABC (5.3 kHz), PSO (5.24 kHz), and GEO (5.2kHz). The lower switching frequency is beneficial because it reduces the stress on the power electronics switches. As shown in Fig. 12, there are switching losses, and again the suggested method has the minimum value of 105 W compared to FA, ABC, PSO, and GEO, which have switching losses of 175 W, 160 W, 140 W, and 125 W, respectively.

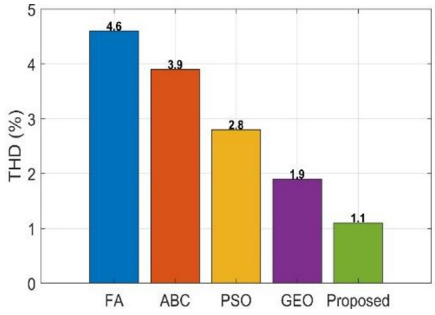

Fig. 13. Total Harmonic Distortion comparison of optimization algorithms

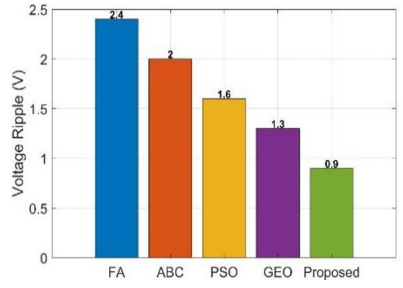

Fig. 14. Voltage Ripple comparison of optimization algorithms

Fig. 13 displays the Total Harmonic Distortion performance, where the proposed method has the minimum distortion level of 1.1%, compared to the FA (4.6%), ABC (3.9%), PSO (2.8%), and GEO (1.9%). This illustrates a clear capability for harmonic suppression. Fig. 14 also illustrates the voltage ripple, where the proposed method leads the others at only 0.9 V. The others are FA (2.4 V), ABC (2.0 V), PSO (1.6 V), and GEO (1.2). Table 2 shows the switching network topology.

Table 2. Switching Network topology of 6 switches, 11-level inverter

S.No	Switch 1	Switch 2	Switch 3	Switch 4	Switch 5	Switch 6	Vo
1	On	Off	Off	On	Off	Off	+5Vdc
2	Off	Off	Off	On	On	Off	+4Vdc
3	Off	Off	Off	On	Off	On	+3Vdc
4	Off	Off	Off	On	Off	Off	+2Vdc
5	Off	Off	Off	On	Off	Off	+1Vdc
6	Off	Off	Off	Off	Off	Off	0
7	Off	Off	On	Off	Off	Off	-Vdc
8	Off	Off	On	Off	Off	On	-2Vdc
9	Off	Off	On	Off	On	Off	-3Vdc
10	Off	Off	On	Off	Off	Off	-4Vdc
11	Off	On	On	Off	Off	Off	-5Vdc

The switching network table in Class 4 outlines the use of six switches to create an 11-level output voltage waveform shown in Fig. 15. By turning on or off specific switches, eleven unique states of voltage output (Vo) were achieved, from +5Vdc to -5Vdc. This multilevel modulation generates a staircase-like sinusoidal output voltage waveform, reducing total harmonic distortion and improving power quality compared to traditional two-level inverters.

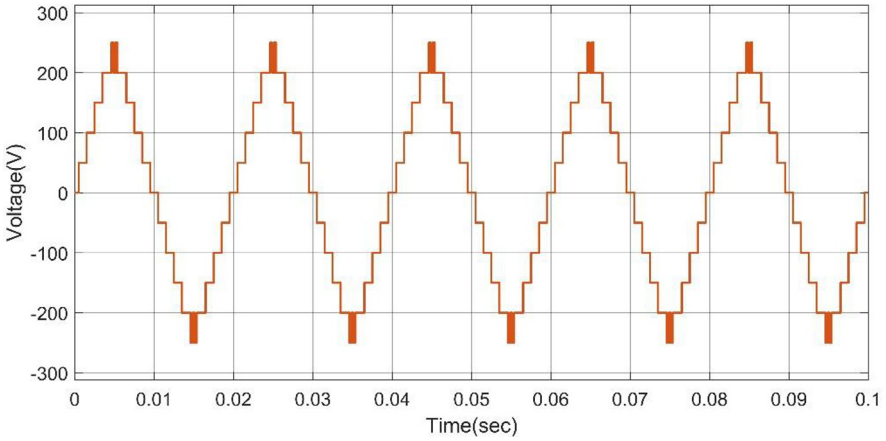

Fig. 15. Steady-State Output Voltage Waveform of the Proposed 11-Level

4.3 Ablation study

The study identifies the contribution of the Solid-State Transformer (SST), converter topology, and PIDD² controller to the integration system. The absence of an optimized PIDD² controller leads to significant performance losses, highlighting the collaboration between advanced hardware and intelligent control, with the PIDD² controller as the foundation. Table 3 shows the ablation study for key component.

Table 3. Ablation Study on the Impact of Key System Components

	THD (%)	**Power factor**	**Efficiency (%)**	**Switching loss**	**voltage ripple**	**Switching frequency**
Solid-State	2.3	0.99	98.5	120	1.2	5
out Solid-State	2	0.96	96	180	3	5
multi-level	2.1	0.988	98.2	130	1.3	5
out multi-level	3	0.945	95	210	3.5	5
PIDD2	1.1	0.996	98.9	105	0.9	5
out PIDD2	2.5	0.97	96.8	150	2.2	5

Table 3 shows an ablation study quantitatively measuring the contribution of each system innovation. The results show that the Solid-State Transformer improves both efficiency and power quality, and the multi-level converter provides a basic increment of performance above traditional designs. The most significant enabling technology is the optimization of the PIDD² controller because omitting it produced a drastic reduction of absolute performance in all counts. The reason the integrated system was able to take advantage of some of the ensuing synergies was due to the introduction of advanced hardware and intelligent control, which allowed the system's unprecedented performance of 1.1% THD and 98.9% efficiency.

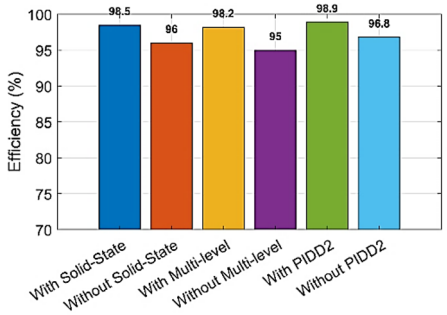

Fig. 16. Ablation Study on System Performance on Efficiency

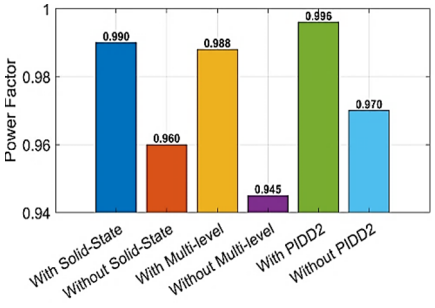

Fig. 17. Ablation Study on System Performance on Power factor

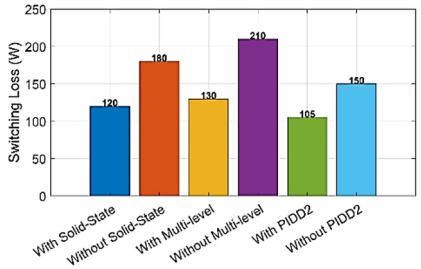

Fig. 18. Ablation Study on System Performance on Switching Loss

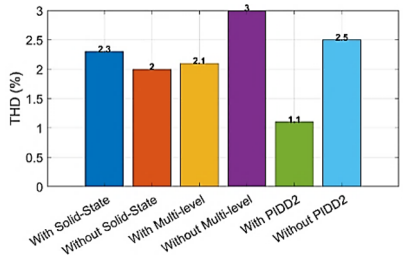

Fig. 19. Ablation Study on System Performance on THD

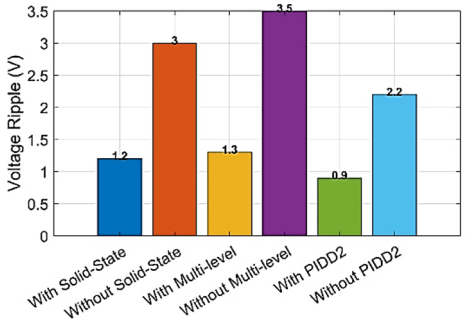

Fig. 20. Ablation Study on System Performance Voltage Ripple

Fig.16 to 20 summarizes the ablation study visually, showing the separate impacts of each of the key innovations. The combination of the Solid-State Transformer, the multi-level converter, and the PIDD2 controller each increases the efficiency and power factor of the system. Missing even one would drastically increase switching losses and voltage ripple. Without the PIDD2 controller, the system would experience the greatest drop-off in performance. This underscores its importance in the control strategy. This demonstrates that all three key components working together are if the system to achieve its best performance.

5 Discussion

The research showcased the exceptional performance of a grid-connected power system using an 11-topology of a level cascaded H-bridge converter and a hybrid GEO-FA-optimized PIDD² controller. The system achieved a THD of 1.1%, efficiency of 98.9%, and a power factor of 0.996, outperforming traditional multilevel alternatives and single optimization algorithms. The GEO-FA-optimized PIDD² controller was the pivotal variable, providing unprecedented system stability, reliability, and power generation quality for grid-interfaced systems for renewable energy.

6 Conclusion

The study presents a new 11-level cascaded H-bridge converter and an optimized PIDD² controller using a hybrid Golden Eagle Optimizer–Firefly Algorithm (GEO–FA). The hybrid optimization algorithm significantly improved the dynamic performance of the PIDD² controller, achieving ultra-low THD at 1.1%, power factor performance of nearly unity of 0.996, and overall system efficiencies of 98.9%. The proposed multilevel topology is a robust solution for future smart grid requirements and integration of renewable technologies. Future research aims to explore hybrid optimization for experimental hardware and real-time digital control platforms for smart grids and high-power industrial energy systems.

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