A Review of CMOS based Differential Ring Voltage Controlled Oscillators

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Abstract. The integrated differential ring voltage controlled oscillator (DRVCO), which has long been utilized in a variety of devices, is based on CMOS technology. CMOS device-based systems are the backbone of the modern electronics industry. It enables electronic systems and devices to be compact and portable. With the amelioration of CMOS technology, the portability and reliability of electronic systems and devices have increased. The VCO is the main building block of wireless communication systems generally used as clock generators, data recovery circuits, digital signal processors, analog to digital converter and other electronic applications. Emerging technologies, including radio frequency (RF) identification, internet-of-things (IoT) systems, and short-range wireless communication devices, have all used VCO circuits. Because of its ongoing use in several CMOS technologies, the differential ring VCO is a good option for integrated circuit designers. The implementation methods and performance comparison of differential VCO for diverse applications are reported in this manuscript.

Keywords: CMOS, differential ring VCO, frequency, phase noise, power, tuning range (TR)

1. Introduction

In the current era, there is a rapid growth in information and communication processing at the high-speed data rate. People desire to be attached all the time by utilizing communication gadgets. Therefore the increasing popularity of modern portable communication gadgets has boosted the need for low-power, high-efficiency, and more affordable wireless systems with improved battery life. CMOS technology has become the favored choice for integrated circuit design owing to its reliability and scalability. The progressive downscaling of the CMOS technology improves the feature size of a MOS transistor and increases the number of transistors on the chip. According to Moore's law, the number of transistors doubles on a chip after every eighteen months

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[1]. Therefore, the high-density chips diminished the cost per function with enhanced the system performance. However, it also increased the total chip power dissipation. Due to scaling, many design issues arise, such as short channel effects, which introduce leakage currents, electromigration, etc. [2]. In addition, other thin oxide devices show inferior thermal stability compared to thick oxide devices [3]. CMOS-based circuits have become the backbone of the modern communication industry. With the evolution of CMOS technology, the portability and power efficiency of the communication devices have increased due to their small size and better power efficiency [4]. The most effective method to reduce CMOS-based circuits' power is to reduce the supply voltage [5]. Whereas CMOS-based logic style has increased the density of silicon integration for system on chip (SOCs), system in package (SIP), and package on package (PoP) drastically [6]. Consequently, the design of modern communication systems needs to be compact to fulfill the demand for portability.

Frequency synthesizers, amplifiers, signal combiners, filters, signal converter (ADC, DAC) and phase-locked-loops (PLLs) are components of contemporary communication systems. PLL is the primary building block of wireless communication systems typically utilized as data recovery, clock generators circuits, digital signal processors, and other electronic applications [7]. In PLL systems, VCO circuits affect spectrum purity, lock time, accuracy, phase noise, frequency stability, and dissipate more power. Random changes in the VCO oscillation output frequency also show up as phase noise, which has an immediate effect on the timing accuracy needed for phase synchronization.

VCOs are also widely used in medical equipment such as magnetic resonance imaging (MRI) and ultrasonography, as well as in cybersecurity applications [8]. Owing to the widespread use of VCO, sophisticated research is being conducted in the design of nanoscale circuits to enhance VCO performance. Ideally, the output frequency (f_o) of a VCO exhibits a linear dependence on the applied control voltage (V_c) and is expressed as

$$f_{out} = f_o + K_{vco} V_c \tag{1}$$

$$K_{vco} = \frac{f_{\max} - f_{\min}}{V_{\max} - V_{\min}} \tag{2}$$

Where K_{vco} is the VCO gain. From equation 2, it is clear that to obtain a large VCO gain, a slight variation in V_c resulting in an broad change in the output oscillation frequency.

For high-quality VCO, the common requirements are high spectral purity, excellent frequency stability, and linear voltage to frequency transfer characteristics. Low fabrication cost and Low power dissipation and are also crucial for VCOs utilized in digital wireless applications. In various applications like high-speed digital interface, a wide tuning range may be required. The two topologies of VCOs that can be commonly utilized to implement in CMOS PLL designs are inductance (L) and capacitance (C) VCO and ring VCO. Table 1 illustrations the performance contrast among LC and ring VCO. Despite the disadvantages of high power dissipation, a large layout area, and a limited tuning range, an LC VCO structure can provide superior phase-noise [9]. In disparity, ring-based VCOs generally exhibit inferior phase noise characteristics but has a compact layout area, an extensive frequency range, low power consumption, and easy integration. The key factors to take into account for a VCO design are low power consumption, a large frequency with minimal phase noise (PN), and a compact layout area. In this paper, differential VCOs circuits, topology and performance comparison for different application are discussed

Table 1. LC and Ring topology based VCO Performance comparison

Parameter	**LC-VCO**	**Ring VCO**
Gain	Low	High
Tuning-Range	Narrow	Extensive
Power Consumption	High	Low
Layout Area	Large	Small
Phase Noise	Good	Poor

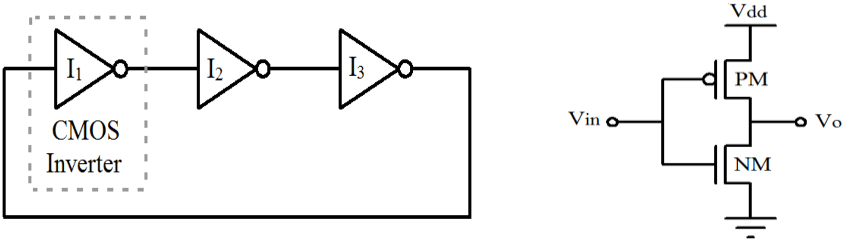
The organisation of this manuscript is as follows: Ring VCO structure's design are reported in section 2. Analysis, along with the suggested delay stages function, are covered in detail in section 3 while section 4 provides a comparision.

2. Ring Voltage Controlled Oscillators

A ring voltage-controlled oscillator structure comprises many delay stages (DS) connected in cascade mode, and the last stage output is coupled to the input of the initial stage. The oscillation occurs when loop satisfies unity gain and a cumulative shift in phase of 2π. A phase shift of π /N must be provided by each delay stage, where N is the number of stages, and the remaining π phase shift is provided by DC inversion [1]. Ring VCOs can be designed using either single or differential ended configurations.

2.1. Single-Ended Ring VCO

Figure 1 represents the arrangement of a single-ended three-stage ring VCO. It is a sequence of CMOS inverter stages comprising a P-type MOS and an N-type MOS, and the connected inverter stages must be odd. In this design, there is no means to control the operation. The control method can be added in several approaches, such as changing the strength of the inverter, varying the loads, or changing the power supply voltage.



(a) **(b)**

Fig. 1. (a) Single ended 3-stages ended ring VCO, (b) CMOS inverter

2.2 Differential Ring VCO

The designs of single-ended ring VCOs are not broadly utilized in the cutting edge for high frequency communication systems. Differential ring VCO structures tend to be chosen over single-ended due to their inherent advantages. Differential ring VCO offers high frequency spectrum, excellent immunity to reduce common mode, bulk and power supply injected noise [10]. It can be designed using a series of delay stages, where the total number of stages (N) is chosen to be even or odd. A ring VCO's frequency can be adjusted externally using a controllable voltage (V_c) or by selecting appropriate tuning techniques, such as increasing the loading, driving strength, or supply voltage, tuning with varactors, or adding or removing delay stages [11]. Figure 2 illustrates the four commonly employed differential ring VCO stages, depending on critical performance parameters, including power consumption, operating frequency and phase noise.

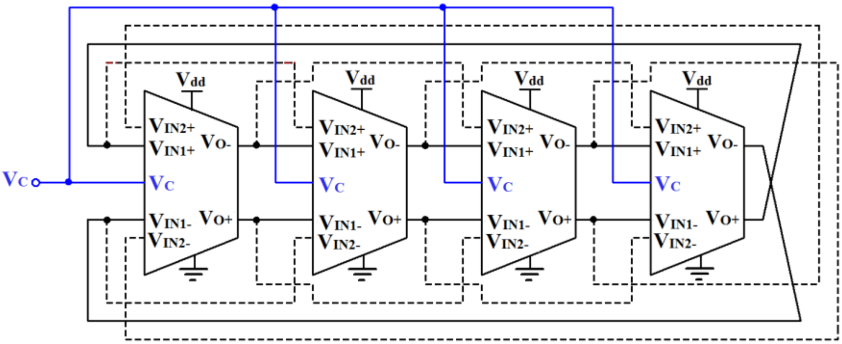


Fig. 2. Configuration of differential ring VCO [9]

Although it requires an additional phase shift in each delay stage, a ring VCO with two delay stages reduces power dissipation and improves phase-noise performance. High frequencies can be produced with a three-stage ring VCO, but in phase and quadrature phase outputs cannot be produced. To achieve this, differential ring VCOs have been designed with four stages.

3. Design Topologies for Differential Delay Stages for Ring VCOs

Improvements in crucial VCO properties, such as frequency, power dissipation, phase noise and figure of merit, have received significant attention over the past twenty years. To increase these crucial factors, a number of differential VCO modeling techniques have already been created [10–23].

To increase phase-noise performance, Park and Kim [10] presented a four-stage ring VCO using completely switching differential dual-delay cells. Each delay cell is made up of PMOS load devices M_3 and M_4 that create a positive feedback latch (PFL) and NMOS differential main input M_1 and M_2 NMOS transistors, as displayed in Fig. 3. The dual delay operation is implemented via an additional couple of PMOS auxiliary input M_5 and M_6 transistors linked to the PMOS loads devices, while gate voltages of M_3 and M_4 transistors are controlled by transistors M_7 and M_8.

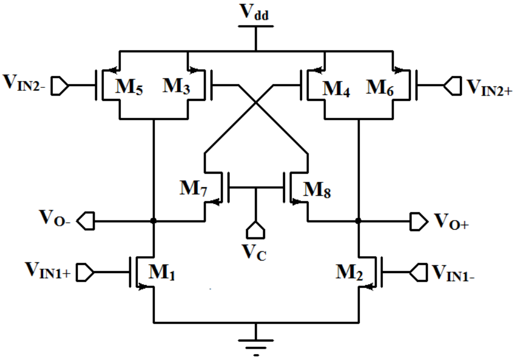


Fig. 3. Fully switching differential dual delay stage

The dual delay operation improves the VCO's output rise time and decreases the phase-noise (PN). Differential VCOs with multiple delay stages have a narrow frequency coverage of 0.75-1.2 GHz and enormous power dissipation of 30 mW.

Further, F. Yuan in [11] suggested the self-bias active inductor-based delay stage to raise the output frequency range. Differential delay-stage structure with self-bias active inductors (AI) is shown in figure 4. To realize the active inductor MOS transistors M_7-M_{10} are used, where a couple of M_7 and M_8 NMOS transistors are used as inductors and M_9 and M_{10} PMOS transistors are used as resistors. VCO based on self-bias active inductors provides the high-frequency-range without the expense of excessive layout area, but it has the disadvantages of huge power-dissipation (PD).

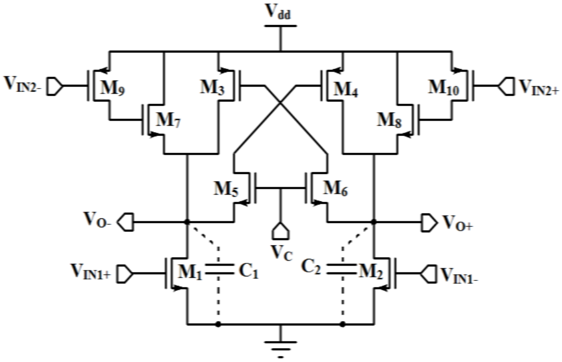


Fig. 4. Delay-stage with self-bias active inductor

Rezayee and Martin in [12] discussed a two-stage coupled ring VCO. The delay stage circuit with coupling and ring inputs is demonstrated in figure 5. The coupled VCO provides a wide frequency coverage of 2.5-9 GHz and a 113% tuning range. However, this advantage is offset by the inferior phase-noise performance of -82 dBc/Hz and enormous power dissipation of 170 mW.

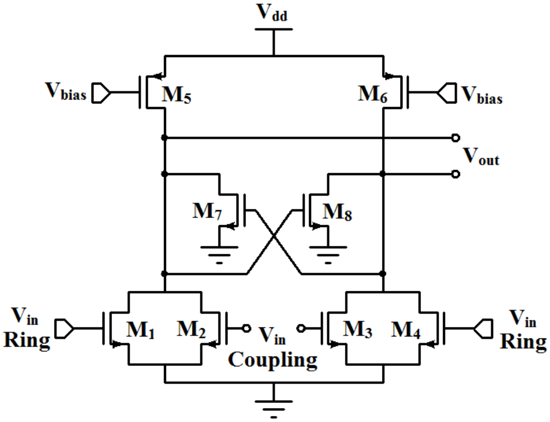


Fig. 5. Delay stage with coupling and ring inputs

The differential source-capacitively coupled current amplifier (SC_3A) has been utilized in [13] to design the five-stage ring VCO with negative feedback. A coupling capacitor (Cs) is attached at the source of the differential amplifier is depicted in figure 6. This configuration enhances the quality factor of the VCO, and it improves the phase noise of -85dBc/Hz by offering enormous power dissipation of 80 mW, and lesser a tuning range (TR) of 34.61%.

Y. A. Eken reported a latching saturated gain delay stage for three-stage ring VCO in [14]. The delay stage with a cross-coupled PMOS transistor has been depicted in figure

7. The designed circuit's feedback properties of latching PMOS transistors M3 and M4 increases output signal transition. As a result, it increases the output oscillation frequency range from 5.16 – 5.93 GHz and enhances the phase-noise (PN) of -99.50 dBc/Hz but suffers from poor tuning range of 12.98 % and enormous power dissipation of 80 mW.

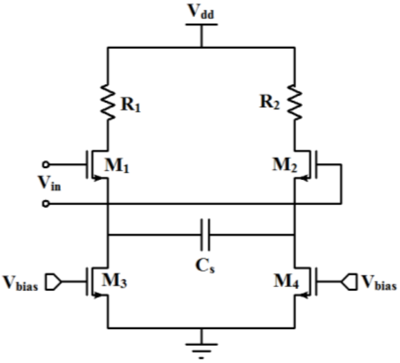


Fig. 6. Circuit of differential SC3A

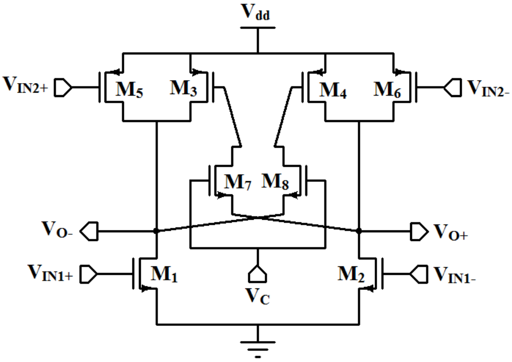


Fig. 7. Saturated gain differential delay stage

A three-stage differential ring VCO is presented by H. Q. Liu et al. [15] using the feed-forward technique that adds the secondary delay path in the loop to raise the output oscillation frequency. In feed-forward topology (FFT) based differential delay stage shown in figure 8, a pair of M_7 and M_8 NMOS transistors enhances the phase noise performance. It also provides positive feedback to decrease the output's nodes transition time. In addition, M_9 and M_{10} transistors is joined in shunt to the controllable load transistors (M_3, M_4) to evade the loss of oscillation. As a result, suggested VCO achieves high output frequency in the range from 8.1-10.50 GHz and improved phase-noise of -92 dBc/Hz, but it has disadvantages of high power dissipation of 68.4 mW a small tuning range of 25.80%.

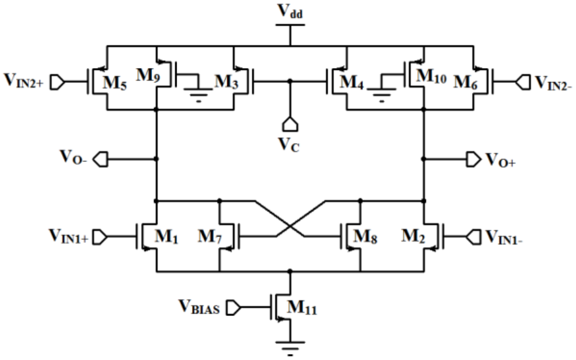


Fig. 8. Feed-forward topology based differential delay stage

In [16], a multiloop three stage ring VCO with coarse and fine tuning based on a differential delay stage is proposed. By altering the voltage at the gate of M_3 and M_4 transistors, coarse tuning (CT) is accomplished by diversifying load. By altering the tail-current passing by the transistors M_9 and M_{10} that make up the positive feedback latch, fine-tuning is achieved. Better phase noise performance of -103.4 dBc/Hz was attained by this differential ring VCO with fine tuning (FT) and CT with the penalty of a small tuning range of 7.3 % and enormous power dissipation of 60 mW. The differential dual delay stage with the coarse and fine-tuning scheme is depicted in figure 9.

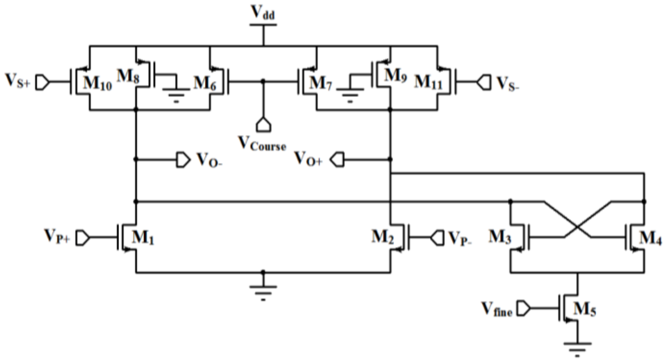


Fig. 9. Differential dual delay stage with coarse and fine tuning scheme

C. Danfeng et al. in [17], modified the differential delay stage for the four stages of differential ring VCO design. It used both current and voltage control together to offer dual-controlled inputs. The delay cell in [17] is quite identical to that in [14], except for the addition of transistors M_9 and M_{10} in parallel with the CMOS latch. With their gates grounded, these transistors inject extra current into the output nodes, altering the total control current and enabling an oscillation range of 4.2 GHz to 5.9 GHz with a phase noise of -99 dBc/Hz. This VCO's restricted tuning range of 12.98% and comparatively high power consumption of 58 mW are its primary disadvantages. Fig. 10 shows the appropriate circuit for the delay stage.

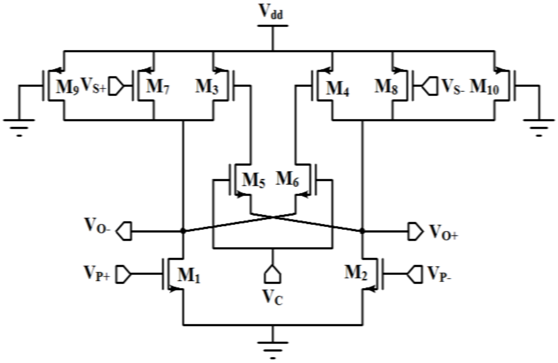


Fig. 10. Delay stage with push-pull inverters

For low-voltage operation, Y. S. Tiao and M. L. Sheu propose a differential delay stage with complementary current-controlled transistors (C_3T) in [18–19]. Figure 11 shows the circuit for the delay stage. A couple of M_9 and M_{10} C_3T are attached to the delay stage to allow surplus current to overwhelmed the low voltage operation limitation and expand the frequency range.

In [18], 0.18 μm CMOS technology is used to replicate a four-stage VCO with a complementary controlled-delay stage at 1.8 V of V_{dd}. Despite a enormous power dissipation of 100 mW, the VCO achieved full controllability, a wide range of tuning 43.39%, and improved noise performance of -107 dBc/Hz.

Furthermore, in [19] three-stage VCO with complementary-controlled (CC) delay stage has been designed with 0.18 μm CMOS technology at 1 V of V_{dd}. This configuration is achieved 88.29% tuning range and 13 mW power dissipation but agonizes from destitute phase noise performance of -93.3 dBc/Hz.

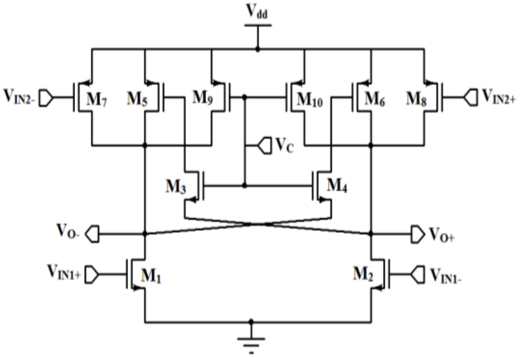


Fig. 11. A complementary current-controlled delay stage

S. Liang and W. R. White suggested a three-stage differential ring VCO with the staggered tuning voltage (STV) (V_1-V_5) generation technique for cognitive radio applications [20]. The delay stage with this topology is shown in figure 12. It achieved a wide frequency band of 4.85-7.60 GHz and low power dissipation of 5.04 mW, but it has the drawback of poor phase noise of -82.5 dBc/Hz.

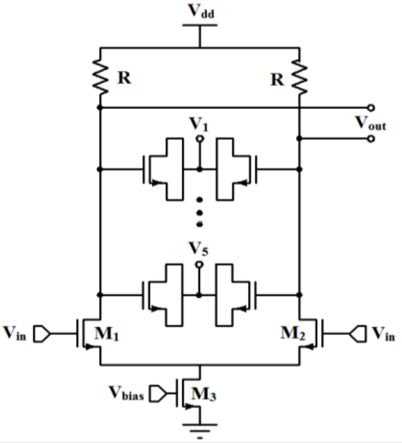


Fig. 12. Delay Stage with staggered tuning voltage

4. Comparison of Various Differential Ring VCOs with Different Performance Parameters

All the designs have been explored based on the merits and demerits. Based on different parameters such as CMOS feature size used, supply voltage (V_{dd}), output frequency (f_o), tuning-range (TR), power-dissipation (*PD*), phase-noise (PN), and figure of merit an exhaustive comparative analysis has been done as shown in tables 2 given below. A variety of inductor-less differential ring VCOs have been investigated according to various parameters. Each designed VCO has certain advantages and disadvantages. Table 2 summarizes the results of differential VCOs extracted from previous research articles of oscillators, including CMOS technology, supply voltage, no. of stages, output frequency, figure of merit (FoM), TR, PD and PN.

In the literature review, it has been found that free-running differential ring VCO is sensitive to temperature, power supply voltage (V_{dd}) and process; hence strict design control is helpful to decrease undesired frequency fluctuations. The selection of diverse differential VCO topologies depends on the application. Hence before selecting the distinct differential VCO topologies, it is necessary to estimate their performance. In the present scenario, the numerous VCO designers are working to succeed in crucial design like low voltage, high linearity, and high output oscillation frequency, extensive TR, high FoM, low PD and low PN.

Table 2. Performance comparison of existing VCO designs

Ref.	**Topology**	**CMOS Process (µm)**	**V_{dd} (V)**	**N**	**f_o (GHz)**	**TR (%)**	**PD (mW)**	**PN (dBc/Hz) at 1MHz**	**FoM (dBc/Hz)**
[10]	Full Switching Diff. Dual Delay-Stage	0.6	3	4	0.75-1.2	50	30	-117$^{\#}$	-171
[12]	Open Loop Inverting Amplifier in a Feedback	0.18	1.8	2	2.5-9.0	113	170	-82	-133.6
[13]	SC$_3$A	0.18	2	5	4.3-6.1	34.61	80	-85	-140
[14]	Delay stage with cross coupled FETs	0.18	1.8	3	5.16-5.93	12.98	80	-99.5	-155.7
[15]	Feed Forward (FF) with NMOS CC Pair	0.18	1.8	3	8.10-10.5	25.8	68.40	-92.0	-153
[16]	CT with Active Load and FT with Positive Feedback	0.13	1.5	3	7.30-7.86	7.30	60	-103.40	-163.0
[17]	CT with Latch Feedback and FT with Diff. Input Current Control	0.18	1.8	4	4.2-5.9	12.98	58	-99.1	-156.2
[18]	C$_3$T	0.18	1.8	4	3.03-5.36	43.39	100	-107.7	-161.3

[19]	C_3T	0.18	1	3	0.479-4.09	88.29	13	-93.3	-154.4
[20]	STV Generation	0.13	1.2	3	4.85-7.60	44.17	5.04	-82.5	-149

Note: *N: No. of delay stages in VCO;* $^{\#}$*: @ 600 KHz*

References

1. Gray K. Yeap, Practical low power digital VLSI design. *Kluwer Academic Publisher*, 1998. doi: 10.1007/978-1-4615-6065-4
2. K. Roy, S. Mukhopadhyay and H. M. Meimand, “Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits,” in *proceedings of IEEE*, vol. 91, no. 2, pp. 305-327, 2003. doi:10.1109/JPROC.2002.808156
3. B. Ullmann and T. Grasser, “Transformation: nanotechnology-challenges in transistor design and future technologies,” *e & i Elektrotechnik und Informationstechnik*, vol. 134, no. 7, pp. 349-354, 2017. doi: https://doi.org/10.1007/s00502-017-0534-y
4. J. Y. Chen, “CMOS-the emerging VLSI technology,” in *IEEE Circuits and Devices Magazine*, vol. 2, no. 2, pp. 16-31, 1986. doi: 10.1109/MCD.1986.6311801
5. R. Gonzalez, B. M. Gordon and M. A. Horowitz, "Supply and threshold voltage scaling for low power CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 32, no. 8, pp. 1210-1216, Aug. 1997, doi: 10.1109/4.604077
6. P. Rickert and W. Krenik, “Cell phone integration: Sip, soc, and pop,” in *IEEE Design & Test of Computers*, vol. 23, no. 3, pp. 188-195, 2006. doi: 10.1109/MDT.2006.64
7. Kumar, N., Kumar, M.: ‘Low power wide tuning range differential ring VCO designs with I-MOS and A-MOS varactor’, International Journal of Electronics and Communications, 2021, 131, pp. 153583. https://doi.org/10.1016/j.aeue.2020.153583
8. Tu, W. H., Yeh, J. Y., Tsai, H. C., Wang, C. K.: A 1.8V 2.5-5.2 GHz CMOS dual-input two-stage ring VCO, In: *IEEE Asia*-Pacific Conference on Advanced System Integrated Circuits, pp. 134-137, Japan, 2004, doi: 10.1109/APASIC.2004.1349429
9. Kumar, N., Kumar, M.: ‘Design of CMOS-based low-power high-frequency differential ring VCO’, International Journal of Electronics Letters, 2019, 7, (2), pp. 143-153. doi: 10.1080/21681724.2018.1477181
10. C. H. Park and B. Kim, “A low-noise, 900-MHz VCO in 0.6-µm CMOS,” in *IEEE Journal Solid-State Circuits,* vol. 34, no. 5, pp. 586-591, 1999. doi: 10.1109/4.760367
11. F. Yuan, “A modified park kim voltage controlled ring oscillator for multi-Gbps serial links,” *Analog Integrated Circuits and Signal Processing*, vol. 47, no. 3, pp. 345-353, 2006. https://doi.org/10.1007/s10470-006-5634-2
12. A. Rezayee and K. Martin, “A coupled two-stage ring oscillator,” in the Proceedings of *IEEE Symposium on Circuits and Systems, (Cat. No.01CH37257)*, Dayton, OH, USA, 2011, pp. 878-881. doi: 10.1109/ MWSCAS .2001.986327
13. R. Tao, M. Berroth, “The design of 5 GHz voltage controlled ring oscillator using source capacitively coupled current amplifier,” in the proceedings of *IEEE Symposium on Radio Frequency Integrated Circuits,* Philadelphia, USA, 2003, pp. 623-626. doi: 10.1109/MWSYM.2003.1211046
14. Y. A. Eken and J. P. Uyemura, “A 5.9-GHz voltage controlled ring oscillator in 0.18-µm CMOS,” in *IEEE Journal Solid-State Circuits,* vol. 39, no. 1, pp. 230-233, *2004.* doi:10.1109/JSSC.2003.820869

15. H. Q. Liu, W. L. Goh and L. Siek, “1.8-V 10-GHZ ring VCO design using 0.18 µm CMOS technology,” in the proceedings of *IEEE internal SOC Conference (SOCC)*, Herndon, VA, pp. 77-78, 2005. doi: 10.1109/SOCC.2005.1554459
16. H. Q. Liu. W. L. Goh, L. Siek, W. M Lim and Y. P. Zhang, “A low-noise multi-GHz CMOS multiloop ring oscillator With Coarse and Fine Frequency Tuning,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 4, pp. 571-577, 2009. doi: 10.1109/TVLSI.2008.2011206
17. C. Danfeng, R. Junyan, D. Jingjing, L. Wei and L. Ning, “A multiple-pass ring oscillator based dual-loop phase-locked loop,” *Journal of Semiconductor*, vol. 30, no. 10, pp. 105014(1-5), 2009. doi: https://doi.org/10.1088/1674-4926/30/10/105014
18. Y. S. Tiao and M. L. Sheu, “Full range voltage-controlled ring oscillator in 0.18µm CMOS for low-voltage operation,” *Electronics Letters,* vol. 46, no. 1, pp. 30-32, 2010. doi: 10.1049/el.2010.2542
19. M. L. Sheu, Y. S. Tiao and L. J. Taso, “A 1-V 4-GHz wide tuning range voltage-controlled ring oscillator in 0.18µm CMOS,” *Microelectronics Journal*, vol. 42, no. 6, pp. 897-902, 2011. https://doi.org/10.1016/j.mejo.2011.03.015
20. S. Liang and W. Redman-White, “A linear tuning ring VCO for spectrum monitor receiver in cognitive radio applications,” in the proceeding of 20th *European Conference on Circuit Theory and Design (ECCTD)*, 65-68. **doi:** 10.1109/ECCTD.2011.6043610