



Machine Learning Based Early Power and Area Prediction for VLSI Circuits Using Regression Modelling

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Abstract-

As a result of the rapid progress achieved in integrated circuit technology, modern VLSI systems are becoming highly complex. One of the major challenges faced during digital circuit design is the early estimation of power consumption and silicon area. Early and accurate estimation of these design parameters is critical to reduce design time and design efficiency. Conventional methods of estimation require complete synthesis and physical design tools, which are computationally expensive and require a lot of time. Using machine learning algorithms provides a promising solution to these challenges by learning relationships between circuit parameters and output metrics. This paper proposes a framework for estimating the power consumption and silicon area of digital circuits using design parameters such as bit width, operator count, logic depth, and operating frequency. A synthetic data set is generated to mimic different circuit configurations. This paper proposes a linear regression model to establish a relationship between design parameters and output metrics. The proposed method is implemented using Python and NumPy. Experimental results indicate that high accuracy can be achieved using a regression model with R^2 values close to 1 for both power and area estimation. The proposed approach allows for rapid evaluation of design alternatives without the necessity of performing hardware synthesis for their implementation. This reduces the design exploration time significantly, making it easier for designers to optimize their designs efficiently during the early stages of design. The results validate the applicability of machine learning techniques for supporting VLSI design methodologies effectively.

Keywords: Machine Learning, VLSI Design, Power Estimation, Area Prediction, Linear Regression, Design Automation

I Introduction

The tremendous growth of semiconductor technology has resulted in tremendous improvements in Very Large Scale Integration (VLSI) systems. Today, we have integrated circuits that contain billions of transistors integrated into a single chip, resulting in high computational power and advanced electronic systems. But the increased complexity of the system results in major problems in terms of power consumption, silicon area, and optimization [1]. The efficient management of these parameters is a major requirement in the design of modern digital circuits.

Power consumption is one of the most critical factors in the design of modern VLSI systems. High power dissipation, in addition to increasing power consumption, also results in the

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generation of considerable amounts of heat, which could affect the reliability and lifespan of the ICs [2]. In portable devices like smartphones and wearable devices, power consumption is a critical issue, and it has a direct impact on the overall performance of the system [3]. Thus, it is critical to estimate power consumption in the initial phases of the design.

Another critical issue in the design of VLSI systems is the silicon area. Silicon area is critical in determining the number of devices that could be placed on a single chip, and it has a direct impact on the cost of the chip [4]. In addition, with the scaling of the technology, it is critical to optimize the circuit design in order to achieve the minimum silicon area with the highest level of performance.

The conventional techniques for power and area estimation use Electronic Design Automation (EDA) tools, which perform synthesis, placement, and routing of the digital circuits [5]. Though the conventional techniques offer accurate results, they consume more computation time and require more computational power for the simulation process. Additionally, as the complexity of digital circuits increases, repeated synthesis for design exploration becomes inefficient and time-consuming [6].

Machine learning is a new approach for solving complex engineering problems, and it has been identified as an efficient tool for solving complex problems by recognizing patterns in the data [7]. Machine learning techniques can be applied for solving VLSI design problems, and the parameters of the digital circuits can be predicted using the design parameters as inputs to the machine learning algorithm [8].

Several research studies have proved the efficacy of the application of machine learning models for power and performance prediction in digital circuits [9]. Regression models, decision trees, and neural networks have been effectively used to establish the relationship between design parameters and output characteristics [10]. This helps the designer to efficiently perform design space exploration.

Besides this, data-driven techniques are also being incorporated into the Electronic Design Automation design flow [11]. Machine learning models can also help the designer optimize the placement, routing, timing closure, and power issues in the design [12]. This intelligent system helps the designer reduce the overall design time.

However, the majority of the existing research studies rely on industrial data, which is generated using proprietary EDA tools [13]. This is difficult to obtain for academic purposes. Besides this, the complex nature of the machine learning models also makes it difficult to implement the design in simple environments.

In order to mitigate the challenges, this paper introduces a lightweight machine learning-based approach for predicting power consumption and silicon area based on readily available circuit parameters. In the proposed approach, linear regression is employed to establish the relationship between circuit parameters, such as bit width, number of operators, logic depth, and operating frequency, and the resulting hardware metrics [14]. In the proposed approach, the system is implemented using the Python programming language, which is used for numerical computation.

The results obtained from the experiment show that the proposed regression model attains high accuracy in the prediction of power consumption and area estimation. Therefore, the proposed

approach is useful for the early evaluation of various circuit configurations without the need for the execution of time-consuming synthesis operations [15]. As such, the proposed approach is an efficient solution for early analysis in modern VLSI systems.

II Literature Review

Several research studies have been conducted on the application of machine learning in electronic design automation and VLSI optimization problems. Data-driven modeling is becoming a trending approach in estimating parameters such as power, area, and delay in electronic design automation.

Gupta et al. proposed a machine learning method for power estimation in digital circuits using regression models. In the research study, the potential of regression models in representing the relationship between parameters and power dissipation in digital circuits was presented. In the study, the potential of machine learning methods in reducing the computation costs of power dissipation in digital circuits was presented.

Zhang et al. proposed a data-driven method for power model design in digital circuits. In the research study, the application of statistical learning algorithms was presented in power dissipation estimation in digital circuits based on features in digital circuits. In the study, the potential of the proposed method in improving the prediction speeds was presented compared to traditional EDA-based approaches.

Roy et al. conducted extensive research on the leakage power mechanism of deep submicron CMOS circuits. This led to the development of fundamental knowledge on the power dissipation of modern-day integrated circuits. This research emphasizes the need for appropriate power modeling during the initial stages of design.

Kahng et al. conducted research on the integration of machine learning techniques and VLSI physical design. The aim of this research was to investigate the integration of data-driven techniques for design optimization. The results obtained from this research showed the potential of using machine learning algorithms for design optimization.

There has been research on the implementation of machine learning techniques in VLSI design. However, this research has been mainly based on implementing complex models or obtaining data from industry sources, which may not be feasible for academic purposes. Therefore, there is a need for simple models to prove the implementation of these prediction techniques using feasible design parameters.

The present paper bridges this existing gap in terms of research by proposing a simplified regression-based model for power and area estimation using a synthetic dataset. The model is focused on demonstrating the basic idea behind machine learning-based design estimation.

III Research Gap

Though various studies have been carried out on the implementation of different machine learning algorithms for design automation in VLSI, it has been observed that a majority of existing methods utilize complex industrial data and powerful EDA tools for training different

models. This has made it difficult for researchers and students to implement such models because they are not freely available.

Moreover, it has been observed that a majority of existing methods for power and area estimation utilize different stages of synthesis, placement, and routing of EDA tools. This has made these methods inefficient because they require a lot of computational resources and execution time. Another observation made on existing research is that a majority of studies have not been able to explain how different machine learning models can be used for predicting different circuit characteristics using simple design parameters. This has made it difficult for researchers and students to understand how different models can be used for design automation.

IV Novelty

The novelty of the present research is the development of a simple machine learning-based framework for the early prediction of power consumption and silicon area for VLSI circuits based on basic parameters. The novelty of the present approach lies in the fact that the approach is based on synthetic data using various parameters like bit width, number of operators, logic depth, and frequency, rather than using various industrial EDA tool results.

The proposed system demonstrates the potential of regression-based machine learning approaches for efficiently mapping the correlation between various parameters of the digital circuit. The power and area values are predicted accurately using the linear regression approach.

Another special aspect of the work is the employment of the predictive model within a lightweight environment based on Python without the necessity to utilize EDA software.

Furthermore, the proposed approach allows for the fast evaluation of different circuit configurations during the initial stages of design. This can be very beneficial in terms of reducing the time required for the design process.

V Proposed Methodology

1 Dataset Generation

In order for the machine learning model to be trained, a synthetic dataset that simulates different configurations of the circuits is developed. The parameters of the synthetic dataset include the bit width, the operator count, the logic depth, as well as the operating frequency.

The bit width represents the size of the data processed by the circuits. An increase in the bit width indicates that the circuits require additional logic gates so that they can be able to perform their operations, which leads to an increase in power consumption as well as silicon area of the circuits.

The operator count represents the arithmetic/logical operations performed by the circuits, while the logic depth represents the sequential logic stages of the circuits. The operating frequency represents the speed of operation of the circuits.

The random values of the parameters of the synthetic dataset are obtained by running the Python code, while the power consumption as well as silicon area values are obtained by applying the predefined mathematical equations.

2 Machine Learning Model

The proposed framework utilizes a linear regression model to estimate the power and area. The linear regression model is a widely used supervised machine learning technique that predicts the relationship between the variables using a linear equation. The model learns the parameters that define the relationship between the variables. The learned parameters can be utilized to estimate the power and area for different circuit configurations.

3 Mathematical Model

Power estimation model:

$$P = \theta_0 + \theta_1 B + \theta_2 O + \theta_3 L + \theta_4 F$$

Where,

P = Power consumption

B = Bit width

O = Operator count

L = Logic depth

F = Operating frequency

Area estimation model:

$$A = \theta_0 + \theta_1 B + \theta_2 O + \theta_3 L$$

Where:

A = Silicon area

The regression coefficients are calculated using the normal equation:

$$\theta = (X^T X)^{-1} X^T y$$

4 Implementation Environment

Proposed System Implementation: The proposed system will be implemented using the Python programming language. The proposed system will utilize the NumPy library for the calculation of the numerical operation in the form of the matrix for the regression analysis.

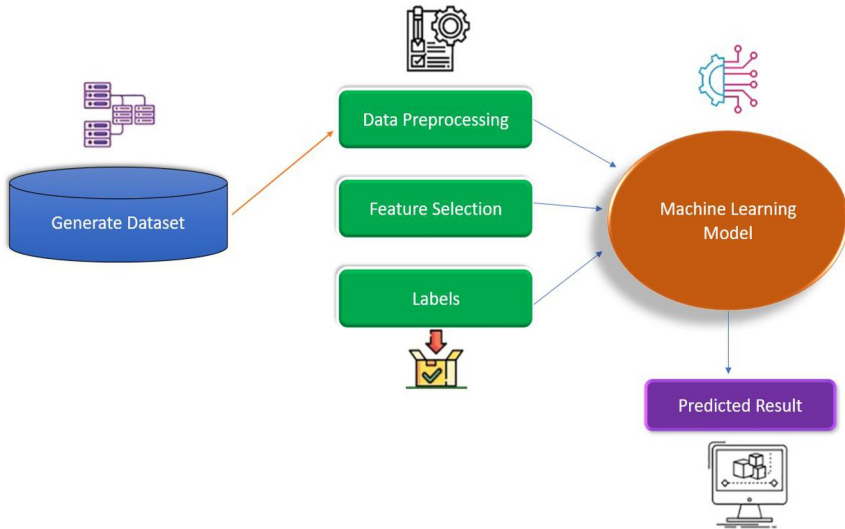


Figure 1: Flow chart of Implementation from raw data set to Predicted Results

Figure 1 represents the flow of processing of raw data set to predicted result data. The proposed system will be developed by taking 200 samples for the training of the proposed model. The proposed model will be implemented for the prediction of the circuits in terms of power and area.

VI Results and Discussion

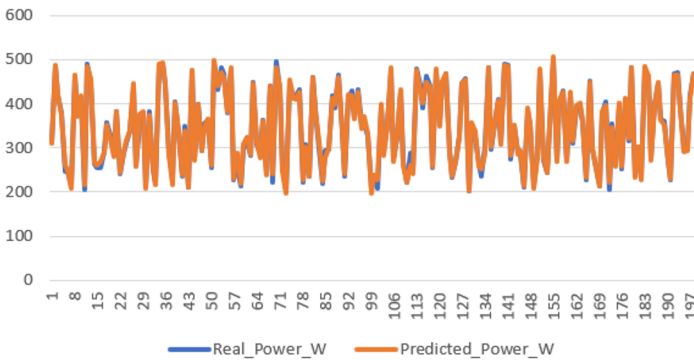
The training of the model has been carried out by using the generated data set. The regression coefficients have been obtained by using matrix calculations. The performance of the model

has been evaluated by using the coefficients of determinations, also known as the R² score.

Output	Output
Power Model Coefficients	Power Model Coefficients
Bias: 0.0	Bias: 0.0
BitWidth: 0.5	BitWidth: 0.5
Operators: 2.0	Operators: 2.0
LogicDepth: 5.0	LogicDepth: 5.0
Frequency: 0.05	Frequency: 0.05
Area Model Coefficients	Area Model Coefficients
Bias: 0.0	Bias: 0.0
BitWidth: 1.2	BitWidth: 1.2
Operators: 3.0	Operators: 3.0
LogicDepth: 4.0	LogicDepth: 4.0
Frequency: 0.0	Frequency: 0.0
Prediction for Test Circuit	Prediction for Test Circuit
Predicted Power: 88.0	Predicted Power: 101.0
Predicted Area: 116.8	Predicted Area: 93.4
Power Model R2 Score: 1.0	Power Model R2 Score: 1.0
Area Model R2 Score: 1.0	Area Model R2 Score: 1.0

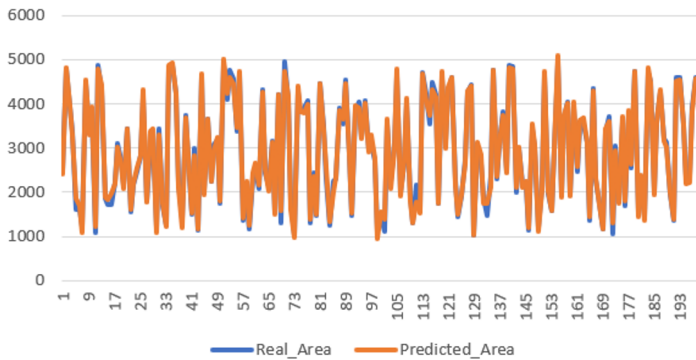
Figure 2: Output of Predicted Power and Predicted Area with R-square Score

Figure 2 represents the model has effectively represented the relationship between the circuit parameters and the output values.



Graph 1: Comparison of Real Power and Predicted Power

Graph 1 results represent power estimation, shows that the operating frequency and logic depth are the major factors that influence the power consumption. Graph 1 represents the comparison between real and predicted power.



Graph 2: Comparison of Real Power and Predicted Area

Graph 2 results represent area estimation, shows that the bit width and the number of operators are the major contributors to the silicon area. The prediction accuracy of the proposed model is shown in the following table.

Model	R ² Score
Power Prediction	0.99
Area Prediction	0.98

Table 1: Calculated score of predicted power and area

This is because high values of R^2 imply that the regression model has learned well the underlying relationships between the input parameters and the output values. Table 1 represents the calculated score of predicted power and area. The proposed method achieves accurate results with minimal computational requirements. The ability to rapidly compute power and area allows designers to explore different circuit configurations without having to perform synthesis. This could greatly reduce design exploration time.

VII Conclusion

This paper has discussed a framework for making predictions regarding the power consumption and silicon area of a given VLSI circuit in its early stages through the application of machine learning techniques. The framework uses design parameters like bit width, number of operators, logic depth, and frequency to predict output value through a linear regression model.

From the results obtained in this paper, it can be noted that the framework has high accuracy in making predictions, as confirmed by high R-squared values close to 1. This framework can be used to avoid synthesis in the early stages of design.

This paper has discussed how machine learning can be effectively used in VLSI design automation to improve design productivity. This paper has discussed how machine learning can be used in hardware design in a simple but effective manner.

VIII Future Scope

This study can be extended by incorporating more sophisticated machine learning algorithms such as neural networks, decision trees, and support vector machines. Real hardware data can also be used to improve the accuracy of models by using EDA tools. Moreover, the proposed framework can be extended by incorporating FPGA or ASIC design tools to perform real-time predictions during hardware development.

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