Computer Aided Computational Intelligence Design Environment for Automated Analog Circuit

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Abstract. The design of CMOS based analog circuits has become progressively more challenging as device scaling advances. The transistor sizing strongly influences the performance metrics such as power dissipation, silicon area, unity gain bandwidth, slew rate, and open loop gain. This makes an analog circuit design a multi objective optimization problem. Conventional analytical design methods, which rely on simplified transistor level models are frequently struggle to identify globally optimal solutions. Which makes analog circuit design a highly nonlinear and high dimensional engineering design problem. To address these limitations, metaheuristic optimization techniques are very successful due explore complex search space effectively and handle multiple objectives simultaneously. In this study, a two stage operational amplifier designed in the BSIM4 model with 130 nm technology node optimized for the required specifications. The circuit level simulations are carried out in Ngspice-26 circuit simulator. The optimization employing optimization algorithms: Grey Wolf Optimization (GWO) and Teaching Learning Based Optimization (TLBO). These algorithms were implemented using Python language and the simulations were executed on an AMD Ryzen™ based system with 16 GB RAM running a 64-bit Ubuntu operating environment. The two-stage operational amplifier optimized to achieves an open loop gain of 82.02 dB, 80.65 dB, a unity gain-bandwidth of 391 MHz, 388 MHz, CMRR of 76.36 dB, 83.69 dB and a low power consumption of 19.8 µW, 18.3 µW respectively for the GWO and TLBO algorithms. These results show both algorithms are achieved the majority of the required specifications and implemented in the automated analog circuit design framework to optimize the analog circuit design.

Keywords: Optimization, TLBO Algorithm, GWO Algorithm

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1 Introduction

The physical world is analog in nature and digital systems increasingly require the integration of analog components on the same chip in the modern Mixed Signal System-on-Chip (SoC) designs. The integration of analog and digital subsystems has become a standard practice in modern System-on-Chip (SoC) designs, with nearly 75% of SoCs incorporating analog part on the same chip [1]. CMOS based analog circuit design presents significant challenges to meet stringent performance specifications. An important aspect of analog circuit design is circuit sizing which is also referred to as schematic level design, which involves determining appropriate values for design parameters that directly influence circuit performance. During schematic design, a large number of parameters must be carefully adjusted to meet the desired specifications for a given circuit topology [2]. Analytical equations are used to model device behavior in conventional analog circuit design, and the circuit simulated manually. This approach is time consuming, labor intensive, and iterative [3]. An ideal solution in terms of important performance parameters such as gain, bandwidth, slew rate, and power consumption is not guaranteed by this method. Developing innovative approaches to solve this issue has been the focus of substantial scientific efforts in recent years [4]. Analog circuit design automation can significantly reduce integrated circuit (IC) development costs and the total design cycle time. To create a robust computer-aided design environment capable of effectively handling intricate engineering design challenges, extensive research is underway [5]. The literature has documented several methods for automated schematic level design of analog circuits. These methods mainly divided into: (1) optimization-based methods and (2) knowledge-based methods. Synthesis rules are developed using the knowledge and experience of analog circuit designers in the knowledge-based approach. The design problem is subsequently solved by incorporating these guidelines into an algorithm [6]. Although applicable in certain situations, this approach is frequently laborious and time consuming, and it is restricted to a small number of circuit topologies, limiting its scope. On the other hand, an optimization-based technique uses search algorithms to iteratively modify circuit design parameters in order to achieve a performance target [7]. Because it can handle complex and multidimensional design spaces and is mainly independent of circuit topology, this approaches are more accurate and reliable for analog circuit design.

1.1 Analog Circuit Optimization

Optimization is the process of finding the best possible solution within a given search space that meets required design specifications within the defined set of parameters. It is a key area of computational science that determines optimal solutions through continuous trial and error iterative search procedures [8]. When applied to CMOS based

analog circuit design, optimization techniques aim to satisfy required performance specifications by adjusting circuit design parameters using metaheuristic optimization algorithms. In CMOS based analog circuits, the primary design variables include, transistor width (W), length (L), resistance (R), capacitance (C), and bias current (I_{bias}). The optimization process is iterative, during which these parameters are updated and evaluated until an optimal or near-optimal solution that meets the desired design objectives is achieved [9].

2 Automated Analog Circuit Design Environment

The width (W) and length (L) of MOS transistors are the main transistor level parameters that must be precisely tuned in analog circuit design, which is a multi-dimensional optimization problem. Designs usually aim to achieve high gain, sufficient bandwidth, low power consumption, enhanced slew rate, enhanced CMRR, and minimal silicon area to meet multiple complex design objectives [10]. As MOSFET scaling increases the complexity of device physics with lower technology nodes, manual design approaches become more and more unfeasible. The creation of intelligent and auto-mated design environments based on metaheuristic optimization algorithms is encouraged by the increasing dimensionality of the problem [11]. In order to optimize transistor sizing in analog circuits, this paper proposes an automated design framework that uses metaheuristic methods. The automated simulation framework, illustrated in Figure 1, which offers a comprehensive automated design environment with an optimization algorithm.

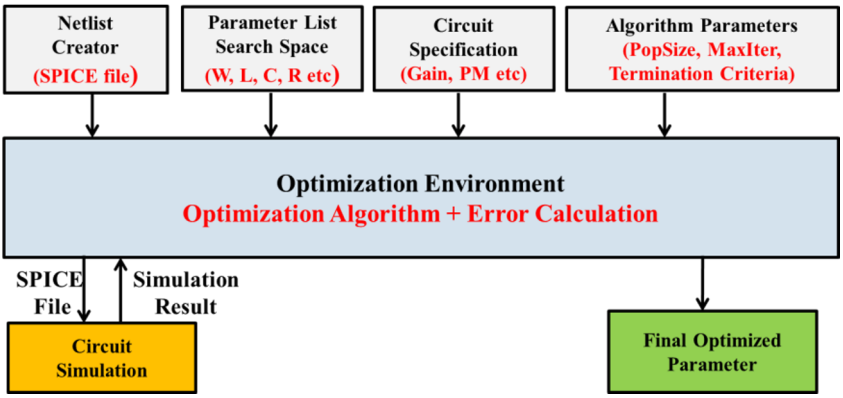

Fig. 1. Optimization based simulation environment for Analog Circuit Design.

2.1 Fitness Function Formulation

To enable precise performance evaluation via circuit simulation, a SPICE netlist of the analog circuit is created. This netlist and the device models for the chosen technology node are supplied to the Ngspice-26 circuit simulator during the optimization phase. Automated, iterative exploration of the design parameter space is made possible by a

specialized software interface that guarantees smooth communication between the circuit simulator and the optimization algorithm. The first step in the optimization process is to randomly generate potential design parameter sets within predetermined lower and higher ranges. After circuit simulation is used to analyze each potential solution, performance metrics are generated for fitness evaluation. A fitness function based on the root-mean-square (RMS) error was utilized to measure the difference between the target design parameters and the simulated circuit performance [12]. Each performance metric is normalized according to its target value to prevent any single specification from dominating. The fitness function is defined as in Equation (1) to compare desired specifications and simulated specifications.

$$Fitness = \sqrt{\sum_{i=1}^{N} \left(\frac{Specification_{desired} - Specification_{simulated}}{Specification_{desired}} \right)_i^2} \quad (1)$$

N is the total number of design specifications taken into account throughout the optimization process in this case. By giving each performance metric equal weight, the root mean square (RMS) error formulation avoids bias toward any one parameter and implicitly balances trade-offs between conflicting goals. In order to penalize deviations from the necessary specifications with higher fitness values, which directs the optimization process toward optimum solutions. By gradually guiding the solution toward designs that satisfy all performance requirements, the optimizer's main objective is to iteratively minimize the fitness function. The optimization process terminates either the fitness value falls below a predefined tolerance threshold or the maximum number of iterations is reached. Through this iterative procedure, the design variables are continuously updated, leading to an optimal solution that meet all required specifications [13].

3 Optimization of Two Stage Operational Amplifier

The operational amplifiers are the fundamental building blocks in analog and mixed-signal ICs. However, continued CMOS scaling into lower technology nodes poses significant design challenges due to various short channel effects, lower supply voltages, and complex device models. To meet the growing demand for high gain, low power, and wide bandwidth the two stage op-amp architectures remain widely adopted as single-stage designs often fail to achieve sufficient gain in scaled technologies. Although multi stage designs introduce stability concerns, various compensation and gain enhancement techniques, such as Miller compensation, gain boosting, and advanced compensation have been explored to address these issues at the cost of increased complexity and increase in power consumption. The design of a two stage operational amplifier constitutes a highly multi-dimensional optimization problem, as the sizing of each device must be carefully adjusted to satisfy performance requirements such as gain, bandwidth, power consumption, and silicon area [14]. To address this complexity, optimization algorithms are employed to automate the CMOS analog circuit design process by optimizing key design parameters including transistor width and length [15]. The

design framework integrates these optimization algorithms with a SPICE based simulation environment to achieve required design specifications as mentioned in the Table 1for the two stage operational amplifier shown in the figure 2.

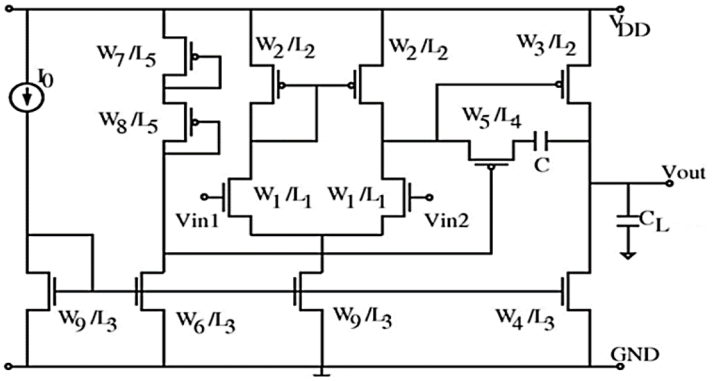

Fig. 2. Two Stage Operational Amplifier

Table 1. Design Specification of Two Stage Operational Amplifier.

Sr. No.	Required Specifications
1	AC voltage gain AV > 80 dB
2	Phase margin > 60°
3	Unit gain bandwidth (UGB) > 100 MHz
4	Power Supply Rejection Ratio (PSSR) > 75 dB
5	Common Mode Rejection Ration (CMRR) > 80 dB
6	Rise Slew Rate (RSR) > 40 V/μs
7	Fall Slew Rate (FSR) > 40 V/μs
8	Power Consumption < 20 μW

4 Results and Discussion

The two stage operational amplifier designed in the BSIM4 model file implemented in 130 nm technology node and optimized for the required design specifications as mentioned in the Table 1. All simulations were conducted on an AMD Ryzen™ processor with 16 GB RAM, 64-bit Ubuntu system environment. The GWO [16] and TLBO [17] optimization algorithms were implemented in Python language and circuit level performance evaluations were performed using the Ngspice-26 simulator. To ensure a fair and consistent comparison, a standardized experimental setup was adopted for both the algorithms. Each optimizer was initialized with a population size of 30, and

the design dimension set to 16 corresponding to the total number of transistor level variables. The maximum number of iterations was fixed at 1000, with a fitness function termination threshold of 1×10^{-6} with detail mentioned in the Table 2. Each algorithm was evaluated over 10 independent runs to account for stochastic variability. The optimized design variables are presented in Table 3 which are the output of the automated design environment.

Table 2. Algorithm parameters for the GWO and TLBO algorithm.

Sr. No.	Parameters of GWO Algorithm	Parameters of TLBO Algorithm
1	Population Size (N) = 30	Population Size (N) = 30
2	Fitness = 1e-6	Fitness = 1e-6
3	Maximum Iteration = 1000	Maximum Iteration = 1000
4	Dimension = 16	Dimension = 16
5	Number of Runs = 10	Number of Runs = 10

Table 3. Optimized parameters of two stage op-amp for the GWO and TLBO algorithm.

Design Variable	Variable Range	Obtained Parameters of GWO	Obtained Parameters of TLBO
W1 / L1	W: 0.5 to 30 (µm) L: 0.2 to 1 (µm) Transistor dimensions are in µm.	0.89 / 0.41	2.61 / 0.42
W2 / L2		3.44 / 0.38	2.12 / 0.38
W3 / L2		8.66 / 0.38	10 / 0.38
W4 / L3		4.56 / 0.97	3.17 / 0.39
W5 / L4		1.22 / 0.20	1.8 / 0.61
W6 / L3		3.04 / 0.97	1.17 / 0.39
W7 / L5		8.11 / 0.28	0.32 / 0.24
W8 / L5		2.91 / 0.28	23.9 / 0.24
W9 / L3		2.31 / 0.97	1.04 / 0.39
Io (µA)	1 to 10 µA	7.57	6.68
C (pF)	0.10 to 10 pF	0.170	0.0559

The performance specifications optimized using the GWO and TLBO algorithms are summarized in Table 4. Both algorithms meet most of the targeted specifications, including voltage gain, phase margin, unity-gain bandwidth, slew rate, and power consumption. However, the design based on TLBO does not fully satisfy the CMRR (Common-Mode Rejection Ratio) requirement of greater than 80 dB, whereas the GWO-based design meets all specified constraints.

Table 4. Optimized Specifications of two stage op-amp for the GWO and TLBO algorithm.

Sr. No.	Required Specifications	GWO Results	TLBO Results
1	AC voltage gain AV > 80 dB	82.02	80.65
2	Phase margin > 60°	66.36°	65.08°
3	Unit gain bandwidth (UGB) > 100 MHz	391	388
4	Power Supply Rejection Ratio (PSSR) > 75 dB	80.23	83.34
5	Common Mode Rejection Ration (CMRR) > 80 dB	83.69	76.36
6	Rise Slew Rate (RSR) > 40 V/us	67.9	60.74
7	Fall Slew Rate (FSR) > 40 V/us	62.26	65.21
8	Power Consumption < 20 µW	19.8	18.3

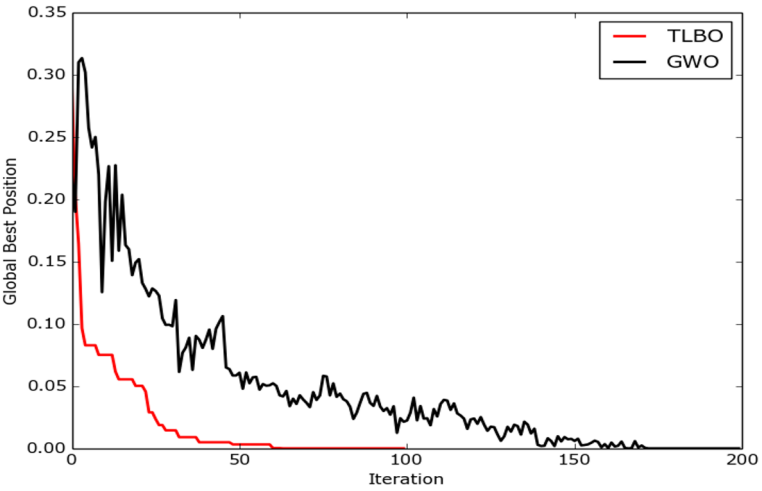

Fig. 3. Convergence Graph for TLBO and GWO Algorithm

Table 5. Comparative Performance Metrics of GWO and TLBO (Mean Values for 10 Runs).

Performance Metric	GWO Algorithm	TLBO Algorithm
Mean RMS Error	0.0	0.0
Average Design Time (s)	205	154
Confidence intervals (Out of 10 run)	10	10

As shown in Table 5, both algorithms achieve a mean RMS error of zero over 10 independent runs, indicating successful convergence to feasible solutions. TLBO requires lower average design time compared to GWO, reflecting faster convergence behavior. The convergence characteristics illustrated in Fig. 3 further confirm that TLBO converges more rapidly during the initial iterations but stabilizes at a higher fitness value due to constraint violations. In contrast, GWO exhibits a more gradual convergence and attains a lower final fitness value, demonstrating superior exploration capability and consistent constraint satisfaction. Overall, these results indicate that while TLBO offers improved computational efficiency, GWO provides a more effective balance between exploration and exploitation for the optimization of the considered analog circuit.

5 Conclusion

This work presented an automated design framework for the optimization of a two-stage CMOS based operational amplifier designed in the BSIM4 model file implemented in 130 nm technology node and optimized for the required design specifications. All simulations were conducted on an AMD Ryzen™ processor with 16 GB RAM, 64-bit Ubuntu system environment. The GWO and TLBO optimization algorithms were implemented in Python language and circuit level performance evaluations were performed using the Ngspice-26 simulator. The optimized two stage operational amplifier achieved an open loop gain of 82.02 dB, 80.65 dB, a unity gain-bandwidth of 391 MHz, 388 MHz, CMRR of 76.36 dB, 83.69 dB and a low power consumption of 19.8 μW, 18.3 μW respectively for the GWO and TLBO algorithms respectively. The optimized designs attained a high open-loop gain, a wide unity-gain bandwidth, an acceptable phase margin, low power consumption, and a high slew rate. The design based on the GWO method met all performance specifications, including the Common Mode Rejection Ratio (CMRR) requirement, while the design based on the TLBO method satisfied most criteria but partially failed to meet the CMRR constraint. Convergence analysis has shown that the Teaching-Learning-Based Optimization (TLBO) algorithm achieves faster initial convergence but ultimately stabilizes at a higher fitness value due to premature convergence. In contrast, the Grey Wolf Optimizer (GWO) demonstrates a more gradual convergence process, resulting in a lower final fitness value while consistently satisfying constraints. These findings suggest that GWO strikes a better balance between exploration and exploitation for the multi-dimensional analog circuit optimization problem. The proposed automated framework is robust and effective for analog circuit sizing and optimization. This work focuses on nominal transistor-level optimization, future research will aim to extend the framework to account for process variations, temperature effects, and device mismatches integrated with this automated environment. This framework also be tested to more complex analog and mixed-signal building blocks, such as voltage-controlled oscillators, operational transconductance amplifiers, filters, oscillators, and ADC front-end circuits. These extensions will further enhance the scalability and applicability of the proposed automated analog circuit design framework in complex System-on-Chip (SoC) environments.

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