Analysis of Drain Current and Transconductance characteristics of Nano-Wire FET for Low Power Circuit Application

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Abstract. Because of their better electrostatic control and lower short-channel effects, NW-FETs have become attractive options for low-power and high-performance nanoelectronic devices. The drain current and transconductance properties of nanowire FETs are fully investigated in this work, with a focus on low-power performance. To assess the device's efficiency in subthreshold and strong inversion areas, the drain current behaviour is examined under various gate bias and channel length circumstances. To evaluate the device's switching capacity and gate control efficiency, transconductance properties are investigated. To comprehend their influence on power consumption, important performance measures, including threshold voltage, subthreshold slope, and transconductance efficiency, are investigated. The findings show that nanowire FETs are appropriate for energy-efficient VLSI systems because they have better current control and increased transconductance at lower supply voltages. This paper demonstrates the substantial benefits that nanowire-based transistor designs provide for the construction of next-generation low-power integrated circuits.

Keywords: NW FET, GAA, SS, FET.

1 Introduction

Device performance, reliability, and integration density have all improved, owing in large part to CMOS technology's ongoing downscaling. Yet, short-channel phenomena, including drain-induced barrier lowering (DIBL), inefficient subthreshold swing (SS), and high leakage current, substantially restrict the performance of planar MOSFETs when they are scaled to deep sub-nanometer dimensions. These factors make it challenging to scale planar devices significantly because they reduce device dependability and enhance static power consumption [1]. Non-planar transistor topologies were developed to solve these problems, and FinFETs are now the industry norm for sophisticated semiconductor nodes. Because the gate may wrap across the channel on several sides, FinFETs provide superior electrostatic control compared to planar MOSFETs.

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FinFETs have scaling issues at sub-10 nm nodes besides these benefits. The device becomes more susceptible to process-induced changes as the fin width decreases, making it more challenging to retain strong gate control and consistent electrical properties. A promising way to get through these restrictions is using Gate-All-Around (GAA) Nanowire Field-Effect Transistors (NW-FET). A nanoscale wire, which is entirely en-circled by the electrode known as the gate, is used to create the channel in a nanowire FET [2]. Short-channel effects (SCE) are successfully minimized due to the design's improved gate-to-channel coupling. GAA nanowire FETs offer nearly ideal sub-threshold swing, decreased DIBL, lesser leakage current, and superior threshold volt-age control than FinFETs. Additionally, the nanowire diameter may be accurately determined, allowing for higher device optimization in superior performance and low-power uses. Accessibility and structural flexibility are two more significant ad-vantages of nanowire FETs. The electrical characteristics of the device may be modified by changing factors such as nanowire diameter, channel length, gate oxide thickness, and gate material. While lowering the size of the nanowire enhances gate control, it also introduces more quantum-confined phenomena that impact threshold voltage and carrier transit. The consequence allows developers more option to maximize device efficiency in accordance with specific application requirements. As a result, nanowire FETs offer greater design flexibility than conventional FinFET de-signs [3]. Integrating nanowire FETs with contemporary materials increases their importance as future technology node. High-κ gate dielectrics will reduce gate leakage while maintaining efficient electrostatic control. Metal gate electrodes reduce variation by increasing threshold voltage stability and enabling effective work-function control. Additional channel materials, such as germanium and III-V semiconductors, were investigated as well to boost carrier mobility and drive current. Because nanowire architectures are consistent with such cutting-edge materials, they are suitable for continuous CMOS scaling. As device size approaches the nanoscale, quantum mechanical effects become increasingly important in determining transistor efficiency. Nanowire FETs have significant quantum confinement due to the lower cross-sectional widths of the channel. This confinement affects the amount of modes and carrier energy distribution, as well as threshold voltage, mobility, and current conduction [4]. Because of this, conventional device models are unable to predict the functioning of nanowire FETs. Quantum effects must thus be considered into consideration in device analysis for precise assessment and design of nanowire-based transistors. The electrical properties and scalability potential of a Gate-All-Around nanowire FET are the main topics of this work's methodical TCAD-based investigation. The device's functioning has been investigated using the input and output features, and important parameters such threshold voltage, on-current, off-current, subthreshold swing, and drain-induced barrier lowering are evaluated. The goal of this study is to show how nanowire FETs are superior to current non-planar devices and to emphasize their applicability for next-generation nanoscale CMOS technologies [5].

Schematic and Cross-Sectional View of Proposed Device. A nanoscale semiconductor wire serves as the channel among the source and drain contacts of a NW-FET. A gate electrode is positioned below or around the nanowire, isolated by a thin gate dielectric to regulate the channel conductivity, whereas the source and drain are produced at the two terminals of the nanowire in the schematic image as shown in figure 1. The nanowire, that provides superior electrostatic control over the channel, shows in the cross-sectional perspective as a cylindrical or rectangular arrangement formed by the gate oxide and gate metal, frequently in a GAA arrangement. By providing the gate to efficiently regulate the whole channel area, this arrangement significantly minimizes leakage current and SCE [6]. There-fore, in comparison with traditional planar MOSFETs, nanowire FETs provide better drain current control, better transconductance efficiency, and lower power consumption, which makes them appropriate for low-power and nanoscale VLSI purposes.

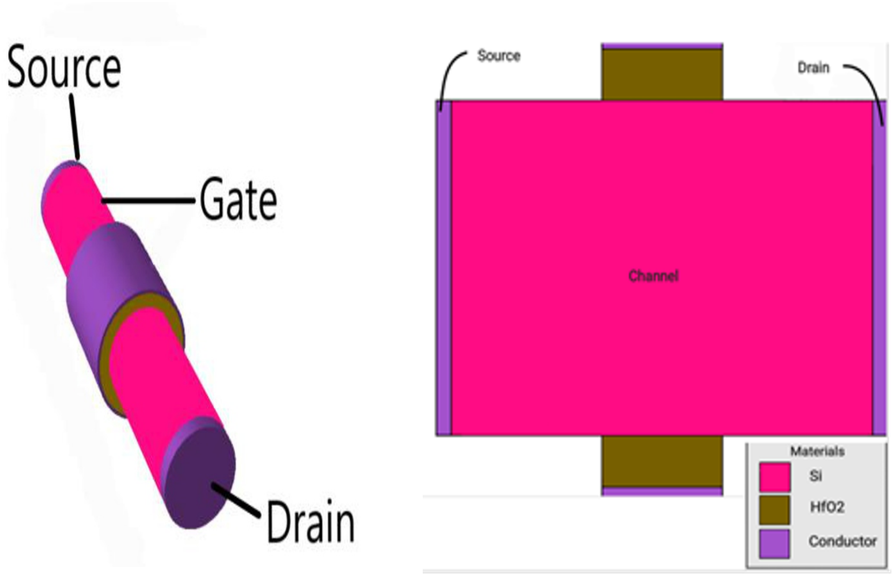

Figure 1:- Cross Sectional View and Schematic view of NW-FET

Table 1. Simulations Parameters of Proposed GAA NW FET.

Heading level	Unit	Parameters Values
Gate Length (L_G)	nm	50
Drain Length (L_D)	nm	5
Source Length (L_S)	nm	5
Work Function (ϕ)	eV	4.8
Dpoing Concentration	Cm^3	1 x 10^{20}

The acceptor concentration charts of a NW-FET with V_{DS} =0.2 V, 0.4 V, and 0.6 V show that a given drain bias affects the carrier concentration and channel doping pattern. The acceptor concentration along the channel is comparatively constant at a lower V_{DS} of 0.2 V, demonstrating less drain-induced consequences and effective electrostatic control by the gate. Since there is increased electric field penetration and partial carrier depletion, there is a slight decrease of efficient acceptor concentration close to the drain area when V_{DS} rises to 0.4 V. The acceptor concentration graph exhibits greater apparent fluctuation adjacent to the drain terminal at an elevated V_{DS} of 0.6 V, indicating larger DIBL and stronger field effects as shown in figure 2. These patterns illustrate that the GAA topology of the NW-FET contributes to steady doping control, which is necessary for dependable low-power operation, while simultaneously highlighting the sensitiveness of the nanowire channel to drain bias [7].

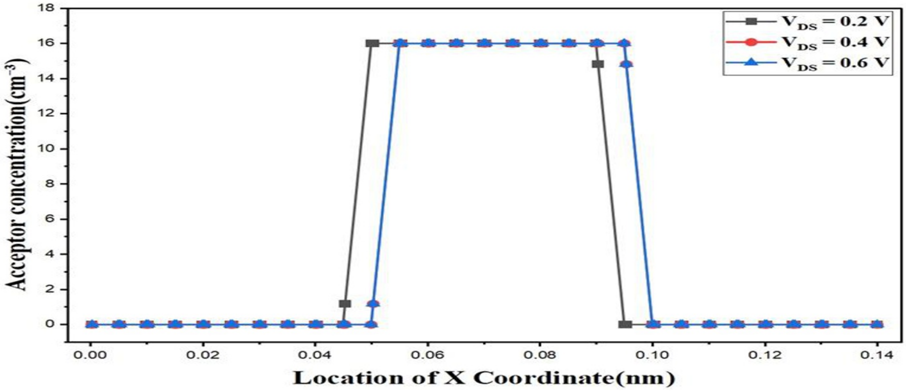

Fig. 2. Acceptor Concentration curve at different V_{DS}

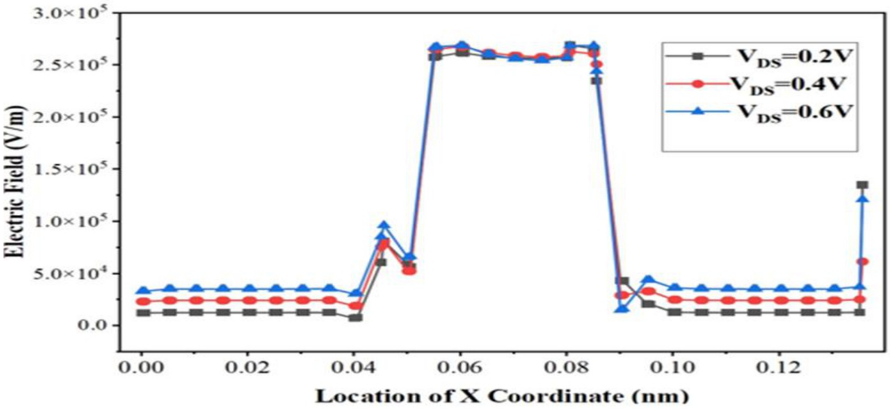

Fig. 3. Electric Field curve at different V_{DS}

NW-FET considerably changes depending on the applied V_{DS}. The electric field is comparatively consistent and mild throughout the channel at a relatively small drain bias of V_{DS} =0.2 V, demonstrating near-linear functioning with inadequate field trap-ping adjacent to the drain as shown in figure 3. The electric field magnitude improves and grows more irregular when V_{DS} rises to 0.4 V, and the higher potential drop causes a distinct peak to appear close to the nanowire's drain end. The electric field achieves its optimum intensity with a significant concentration near to the drain area at a greater drain bias of V_{DS} =0.6 V, showing the initial stage of velocity saturation and enhanced carrier dispersion. Generally this increase, the NW-FET's GAA structure efficiently limits and regulates the electric field, minimizing leakage current and SCE, both of which are beneficial for low-power performance. A NW-FET's conduction current density patterns at various V_{DS} demonstrate that current conduction is certainly depending on the supplied drain bias. The current density rises almost exactly with gate voltage at low V_{DS}=0.2 V, implying operating in the linear area with a de-creased electric field across the channel and constrained carrier velocity. The conduction current density improves more quickly when V_{DS} approaches to 0.4 V because of increased charge injection from the source, greater channel modulation, and quicker carrier transport [8]. The device progresses approaches saturation as the carrier velocity nears its limit beneath high electric fields, and the maximum current density is seen at V_{DS} =0.6V as shown in figure 4.

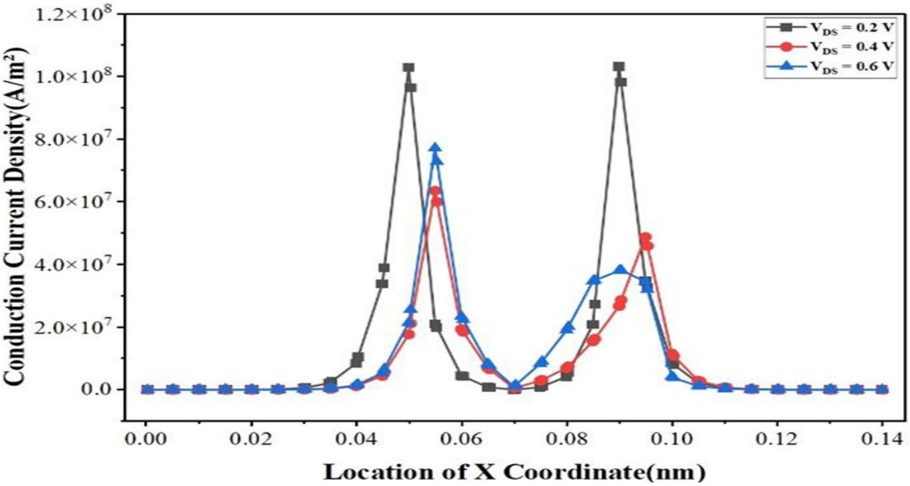

Fig. 4. Conduction Current Density at different V_{DS} = 0.2V, 0.4V, 0.6V

Plotting a NW FET's transconductance (G_M) graph as a result of gate voltage for various V_{DS} usually reveals that gm rises as V_{DS} increases because of increased carrier transport and channel electric field. Since the device works closer to the linear area with limited carrier velocity at lower V_{DS}, G_M steadily increases with gate voltage and reaches a lower peak value shown in figure 5. Enhanced gate control and enhanced drain-induced carrier injection are reflected in the gm curves' upwards shift when V_{DS} rises to 0.4V and 0.6V, which show larger peak transconductance and occasionally a wider G_M peak.

While extreme V_{DS} may potentially produce SCE such mobility degradation or drain-induced barrier lowering at larger gate voltages, the greatest V_{DS} =0.6 V often gives the largest G_M, suggesting better current modulation capabilities. A nanowire FET's drain current (I_D) features, evaluated at various V_{DS}=0.2V, 0.4V, and 0.6V, usually exhibit a distinct dependency on V_{DS} throughout the gate voltage sweep. Because the larger longitudinal electric field enhances carrier transport across the nanowire, the I_D grows at all gate voltages when V_{DS} improves. Drain-induced barrier lowering (DIBL), that lowers the actual threshold voltage, causes increased V_{DS} in the sub-threshold zone to marginally enhance I_D as shown in figure 6. The divergence among the graphs became more apparent in the strong inversion (ON) area, with V_{DS}=0.6 V producing the maximum current, subsequent to 0.4 V and 0.2 V, demonstrating better carrier injection and lower channel resistance. In general, effective electrostatic control of the nanowire channel and appropriate FET functioning are indicated by the linear rise in I_D with V_{DS} [9-10].

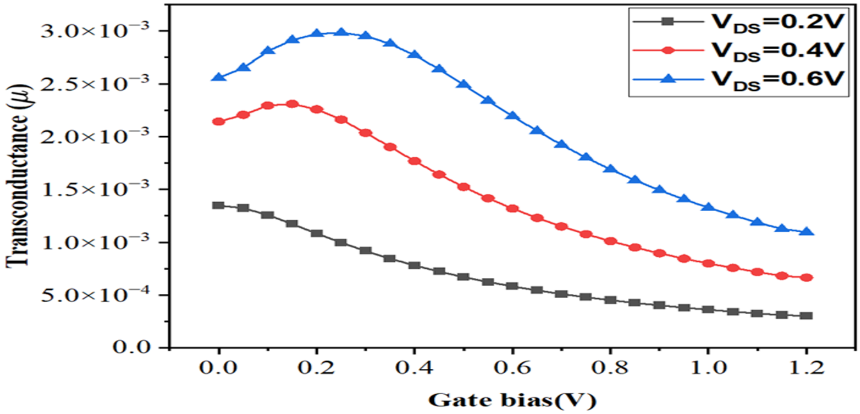

Fig. 5. Transconductance curve at different V_{DS} = 0.2V, 0.4V, 0.6V

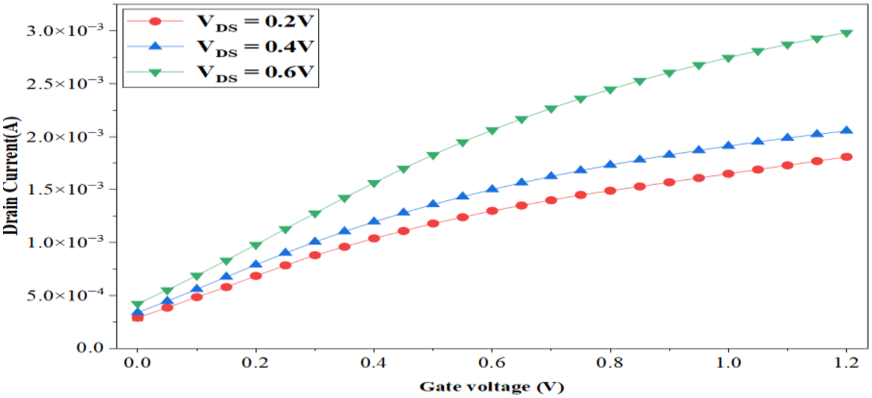

Fig. 6. Drain Current vs. Gate Voltage Curve at different V_{DS}

Table 2:- Parameters Extraction of Proposed Device

Parameters	Unit	Simulated value
I_{ON}	A	2.75×10^4
I_{OFF}	A	4.23×10^{-12}
I_{ON}/I_{OFF}	-	0.65
Subthersholed Slope	mV/dec	43.62
Transconductance	µ	9.8

Conclusion: - The current and transconductance properties of a NW-FET were carefully investigated, with an emphasis on low-power circuit uses. The results show that the nanowire FET has superior electrostatic control because of its GAA shape, resulting in significantly better drain current modulation and transconductance efficiency than traditional planar MOSFETs. The drain current features show less leakage current and better SS performance, which are crucial for reducing static power consumption in low-power circuits. Additionally, the transconductance study showed increased peak transconductance and enhanced transconductance efficiency at smaller operational voltages, giving the nanowire FET an excellent choice for energy-efficient analog and digital systems. The nanowire FET has great potential as a device design for future low-power integrated circuits because of its improved transconductance, scaling, and greater current regulation.

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