

Improve the quality of Faster Than At-Speed Testing using the statistics information

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Abstract: Test generation method for the small delay defects not only requires low algorithm complexity, but also need more possibility to detect small delay. The method proposed in this paper uses statistical information to provide guidance for the back stage in test generation, which can improve test quality effectively. This method firstly uses simulation to obtain the statistical probability of nodes in the circuit, and then uses statistical information and controllability of nodes in circuit to determine the unknown conditions in advance in back stage, thereby reducing the number of backtrack and improving fault coverage. The result of testing on ISCAS'89 benchmark circuits shows that the test generation based on probability statistics method can make the transition delay fault coverage increase about 1.3% and time save about 9%.

Keyword;small delay defects; faster than at-speed testing;probability statistics; path sensitize

I. INTRODUCTION

With Continuous shrinking of the process geometries and rising of the operation frequency of the integrated circuit(IC), the test for circuit become more and more difficult. The IC requires the right response to the input within the prescribed time in addition to the properly logic function. A small manufacturing defect of high-frequency circuit may increase additional delay, which can cause the circuit to stop functioning properly[1].The reason of the chip failure caused by the delay fault is approaching the small delay defect gradually so that the small delay defect is becoming the important reason to affect the quality of IC[2].

The main task of test generation for small delay defects is to sensitize fault through paths as long as possible, and there are three types of methods. The first method is to study the new test generation method associated with timing. It uses a transition fault model to ensure coverage and refers to the long path sensitization of the path delay fault model on the basis of test generation strategy to implement the test generation for a small delay defect. The core of this method is how to find the longest measurable path through each point. The literature[3] uses a static timing analysis techniques to guide test generation and chooses a longer excitation path and the propagation path to detect small delay defect; The literature[4] uses the topology of circuit to guide test generation, finding a part of the node from the circuit to test generation by the known timing method and using traditional methods for remaining nodes, thus saving time of test generation; The literature [5] divides the transition fault of circuit into two categories. The one uses

test generation algorithm associated with timing, and the other use the traditional and timing-unrelated test generation algorithm to accelerate the speed of test generation. The second category is a selection method of test vector based on the assessment of test quality. It does not directly generate high-quality test vectors, but select some high-quality test vectors from redundant vector set by fault simulation, which can reduce the complexity of the test generation. The literature[6-7] proposed the probability notation of a gate delay defect and the so-called " output offset " test quality assessment criteria, which only need to do a depth-firstly traversal on the circuit for each test vector of N-detect test set to get quality parameters .It picks out the best vector for testing the small delay defect and simplifying the calculation. The literature [8] proposed the method of sensitizing fault along the longest path to get benchmark vector set, which can improve fault coverage. However, the test volume will sharply increase. The literature [9] proposed the method of selecting vector by using the benchmark vector set detecting stuck-at fault. The third method uses faster than at-speed testing, that is it will test those small delay defects only sensitized along the short path by using clock higher than the nominal operating frequency of circuit. One of the biggest benefits of faster than at-speed testing is using test generation method associated with timing, which reduces the complexity of test generation algorithm According to the path length, it can group the test vectors to alleviate these problems[10].The literature[11] selects path by using path delay fault model and groups the vector by using the single-path path sensitization, which makes the paths whose delays are close become a set. The literature [12] proposed the method of selecting measurable path and groups them base on path delay fault model and single-path path sensitization.

The above three types of methods have some problems. The time of test generation of first method is several times as much as the traditional test generation, so its efficiency is an unavoidable problem. The test generation quality of second method depends on the baseline vector set, but the generation of high-quality benchmark vector set is a very difficult problem. The third method is difficult to grasp the size of the packet because the thick packet has no effect and small packet will result in severe over-test phenomena, moreover the requirement of the tester for faster than at-speed testing is high.

This paper obtains the value information of each node in the circuit by probability statistical method and guides the process of test generation by using the information and

controllability of node. We can use these information to guide the determination of unknown something in the back stage of test generation, which will reduce the backtrack time of test generation and accelerate it. Meanwhile, using the information of node in circuit can reduce possibility of failure test generation in condition of predetermined backtrack times, thereby improving fault coverage.

II. SUMMARY OF METHOD

Each node of circuit has a logic value corresponding with the certain input vector when we load random vector to the circuit. A node may appear same value when the circuit was applied different input vectors. Because of a vector being not unidentified bit, the logic value of the node may arise two situations, namely 0 and 1. When we need value of a node to equal 1 in the back stage of test generation, but the possibility of the node's value being 1 is very small after the probability statistics, which can indicate that obtaining the test vector is difficult. This paper does probability statistical by using input vector that is randomly generated, that is the probability of each input value equals to 1 is about 0.5. We found that the value of each node is not random, even the probability of some nodes that its value equals to 1 is biased at both ends, that is it is difficult to make this node value equal to 1 or 0, which may provide very good guidance for deterring unknown information. In figure 1, the node number that probability of the node value equals to 1 is higher than 0.75 or less than 0.25 exceeds the half of number of sum nodes, which shows that the interaction among nodes is greater than others in IC S15850.

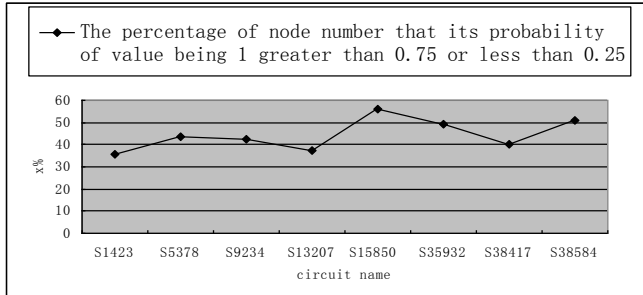


Figure 1. The scale drawing of the probability of nodes' value is 1.

In order to get the information of nodes, we need count the value of node in circuit. The node value in circuit is affected by the input value, so some vectors need be loaded to input. In the effect of each vector, each node in circuit will arise a value correspond with the vector, and we only record this value. The number of the same value of node would be got when loading more vectors, and the probability of one value of node would be got. The vector that is loaded to input need to have the certainly representation because our necessity is information among node, so the vector need be generated randomly. In the case of small scale of circuit, we can choose an exhaustive method to get the input vector. The method adopted in this paper is that generating the vector set is based on the scale of circuit.

Test process: Firstly, it get the correlation information of logic nodes, line and path in circuit by doing the static

timing analysis. Secondly, it employs the transition delay fault set that is constituted by line as the seed set (for simplicity, this paper does not take the different into account to the rise transition and fall transition) and choose a seed to look for the path that it passes target fault point and its path delay meets requirement of test timing. Finally, it combines the sensitized standard to do test generation. If the selected path could be sensitized, mark the logic gate of the path to be already detected and mark these nodes in the TDF set. If there is some seeds not marked in TDF set, we will continuously do test generation until all TDF be traversed. The flow chart is shown in figure 2.

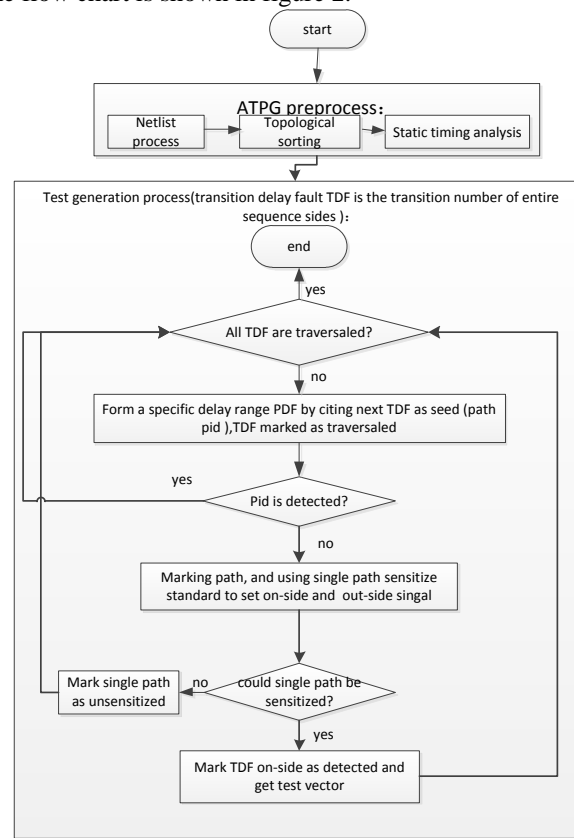


Figure 2. Test flow chart

III. TEST GENERATION PROGRAM

A. Application of statistical probability

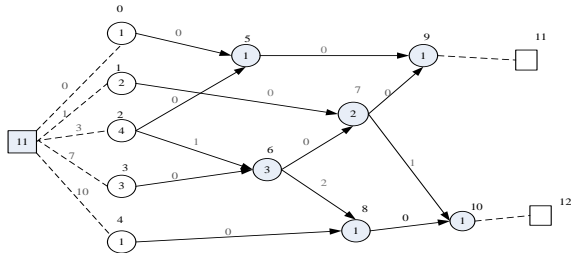
It is necessary to sensitize the path when we select a path that it meets the requirement of the delay. It shows that the path is measurable if the path could be sensitized, otherwise it is not measurable. The process of path sensitized consists of three aspects that are implication, back and backtrack. Using good back strategy not only can reduce the number of backtrack and save the time of test generation, but also can increase the number of detected fault in the case of limiting times of backtrack. The back strategy proposed in this paper based on probability statistics and controllability of node has sharply improvement in time of test generation and number of detected fault relative to the existed back strategy.

The back strategy in this paper firstly gets the probability

statistical of associated nodes, then guides the process of back by using the probability statistical and controllability of node. For example, we can not determine the input value through the implication when the output value of a and (or) gate does not equal to 0(1), which is necessary to use the back strategy to determine the input value. The back strategy proposed in this paper firstly determines the input value according to the controllability of node, if it failures, that is the controllability of input value is bad, so we can determine the input value that is very possible by using the probability statistical of input. Assuming that it is a and gate that has n input and is not determined the value, and its probability equaling to 1 of input value is π_i , that we need select a input that has the smallest probability equaling to 1 from the n input and make the input value equal to 0. It makes the input value equal to 1 if $\pi_i > 1 - \pi_i$ and makes the input value equal to 0 if $\pi_i < 1 - \pi_i$ in remaining input. The input value not only meets the requirement of output value but also be obtained easily when output value of a logical gate already has determined. It is necessary to select an input that meets the requirement of output value and that its probability is big, which determines the input value. It can be compared separately for the rest of the inputs to make each input equal to very possible value.

B. Static timing analysis

The algorithm base on the path static timing analysis has the high complexity because the number of path and the number of node shows the relationship of exponentially increasement, so this paper adopts the method applied by many researchers -- static timing analysis base on node. Firstly, it makes the circuit equivalent to a directed acyclic graph, and then it calculates the relevant property value of each node to calculate easily by using the topological order. For simplicity, it is necessary to code respectively for each path of all circuit. We record the number of path from the node to the original output or pseudo output, and mark each path by using the marker. Moreover, we not only can calculate the number of path in circuit but also can look over path and calculate the path delay through it. The directed acyclic graphic of C17 is shown in figure 3.



Element structure in circuit c17

We use the circle to represent the logical gate node in circuit, and the number on it means the code of node, and the number of in it or the number of in block indicates the number of path from the node to the original output or pseudo output, and the number online means the marker of path. For purposed of calculation, it treats the input and

output as the node in circuit when preprocessing circuit so that the input tag becomes the start tag. The code of path is sum of the input start tag of the path plus path tag of line on path.

IV. THE RESULT AND ANALYSIS OF EXPERIMENT

The paper performs experiment for enhanced scan ISCAS'89 benchmark circuits that its test program is completed by using C language, running on a 2.31GHz, 2GB RAM PC. The delay of different types of gate and standard deviation in the process of static analysis are showed in table 1.

In this paper, we compare with the literature[12] using a single path sensitization criterion to produce faster than

Table 1 the expected value and standard deviation of different gates in benchmark circuit

The style of gate	Expectations of gate delay (μ)	standard deviation of gate delay (σ)
BUFF	4	0.3
INV	2	0.2
NOR,NAND(g_i)	g_i+1	0.3
OR,AND(g_i)	g_i+2	0.3

at-speed test generation, and the results are shown in Table 2. The 1th column in Table 2 represents the benchmark circuit names, and the 2th, 3th column respectively represents the sum of PDF and TDF (including the jump-up and jump-down) in benchmark circuits. The 4th, 5th column respectively represents the TDF coverage and CPU running time in literature [12], and the 6th, 7th column respectively represents the TDF coverage and CPU running time in this paper. According to the literature [12] and with the fault coverage of the 4th column, we calculate the fault coverage and CPU running time without using the statistical probability, and the results are shown in the 8th,9th column respectively. With comparing the results among the 4th, 6th, 8th column, it is shown that the information of the statistical probability can contribute to improve the fault coverage. Comparison of the 5th, 7th, 9th column indicates that test generation using the statistical probability can save about 9 percent of the CPU running time. The experimental results present our method has improvements in both the average running time and the TDF fault coverage. Of course, it requires some preprocessing time to obtain the statistical information, but usually less.

To estimate the effect of the statistical probability on test generation, we use the standard deviation of statistical probability to represent its distribution in this paper. The standard deviation indicates the dispersion of samples, and the better value means the better dispersion. In the calculation of standard deviation, we consider all nodes whose probability value is 1 in each circuit as a whole, and each node whose probability value is 1 as an individual, thus obtain the standard deviation of nodes whose value is 1 in each circuit. In the process of test generation, we need to make a decision on some unknown information. Obviously, the greater the probability of certain value is, the stronger the guidance of unknown information in the process is. As shown in

TABLE 2 COMPARISON OF THE PRESENT METHOD WITH OTHER METHODS

Circuit name	PDF number	TDF number	literature 12		The method proposed in this paper		The TDF coverage being not use probability statistics	The CPU(s) of fixed fault coverage
			TDF coverage	CPU(s)	TDF coverage	CPU(s)		
S1423	89452	3004	94.44%	4	94.85%	3.73	93.98%	5.22
S5378	28092	11046	93.13%	5.28	94.36%	5.84	92.62%	7.1
S9234	489708	18968	68.41%	20.4	69.58%	21.88	67.99%	24.57
S13207	2690738	27938	83.89%	38.59	85.33%	45.43	83.41%	50.14
S15850	329476092	33062	79.21%	212	81.06%	196	78.75%	209
S35932	394282	75320	61.22	576	62.37%	510.3	60.7%	589
S38417	2783158	80162	89.70%	371.6	90.88%	326.3	89.16%	395
S38582	2161446	80324	88.04%	352	89.66%	339	87.43%	348.3
average			82.26%	197.48	83.51%	181.06	81.76%	203.54

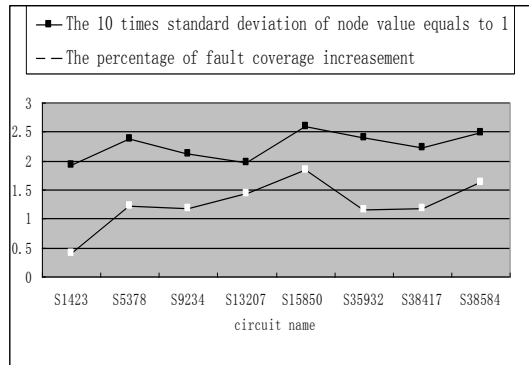


Fig5. The relation picture between variance of node's value and growth percentage of fault coverage

Figure 5, the top line represents the difference of fault coverage whether use of statistical probability, i.e., the difference between the 4th column and the 6th column in table 2. And the following line represents the 10 times standard deviation of statistical probability, where we use the 10 times standard deviation to compare intuitively. It is shown that there is a positive correlation between the statistical probability and the test generation, which means the statistical probability can guide the process of test generation and improve the fault coverage in less time.

V. CONCLUSION

Using small-delay detection based on probabilistic method has the following advantages: (1) the use of probability and statistics can guide the part of the test generation process and improve the small delay TDF coverage. (2) Using of probability and statistics can determine the unknown information in

advance, thus saving test generation time.

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