

Zero-IF and Modularization RF Design of Wireless Identification Reader for UHF Passive Tags

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Abstract—In this paper, a zero-IF and modularization RF design scheme of wireless identification reader for UHF passive tags is presented. The reader works at 860-960MHz, and corresponds to the standard of EPC C1 G2 and ISO/IEC 18000-6C. The realization of some key modules is elaborated. The tests have shown that the proposed RF design scheme of reader works well. The transmit power of the reader is up to 32dBm, and the stable reading range reaches 9 meters.

Keywords—wireless identification; reader; UHF passive tag; zero-IF; modularization

I. INTRODUCTION

High performance and low cost has changed UHF passive technology into the application mainstream of Internet of Things based on wireless identification, or RFID (RFID IoT). However, in the practical application, it is well known that one of the bottleneck problems in RFID IoT is the design of reader, because one reader must manage at least thousands of tags. Therefore, high-quality wireless identification reader (WIR) for UHF passive tags stands for one of the core techniques in the industrialization of UHF RFID.

Some of design schemes of UHF RFID readers have been proposed [1-10]. But these schemes either stayed in simulation level, or were based on the existing single RF chips. In other words, they didn't focus on the practical challenges, or were not so flexible in realization.

In this paper, we propose a zero-IF and modularization RF design scheme of WIR for UHF passive tags based on discrete elements and small scale ICs. The reader works at 860-960MHz, and corresponds to the standard of EPC C1 G2 and ISO/IEC 18000-6C. The scheme is simple and flexible, and will be changed into real product.

II. PROPOSED RF DESIGN SCHEME

Our proposed RF design scheme is shown in Fig. 1. In Fig. 1,

Crystal Oscillator is used to generate the reference frequency of PLL (Phase-Lock Loop). Here, the working frequency is 33MHz.

PLL is used to multiply the 33MHz to the demand frequency of EPC C1 G2, that is, 915MHz.

Modulator is used to modulate the working frequency to generate the modulated RF signal.

Power Amplifier (PA) is used to magnify power to the demand scope of the EPC C1 G2, for example, the maximum value is 32dBm.

Circulator is used for common use of the transmitter and the receiver, i.e., to transmit modulated signal and to receive the return signal.

The function of antenna is to transmit and receive the EM wave.

The function of demodulator is to demodulate the return signal.

The function of differential amplifier is to magnify the demodulated signal. It can enhance the receiving sensitivity.

The function of comparator is to reshape the waveform of the demodulated and magnified signal for the processing convenience of the controller.

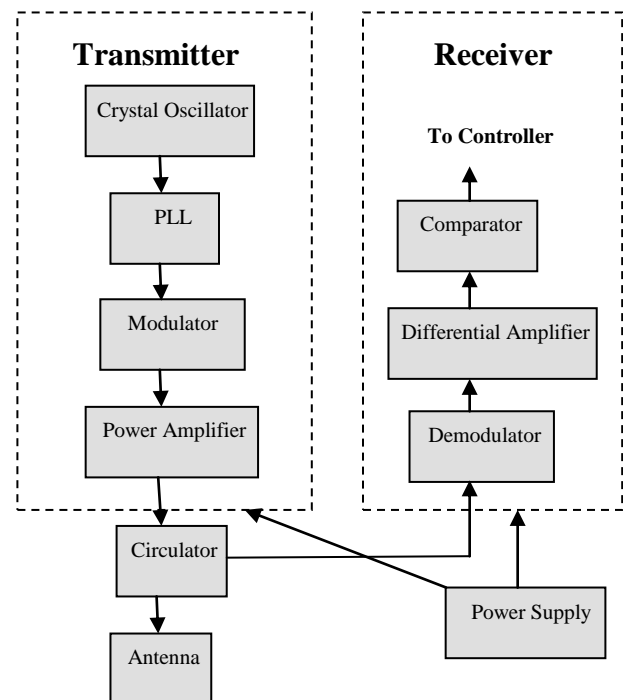


Fig. 1 Proposed RF design scheme of WIR

III. REALIZATION OF SOME KEY MODULES

A. Crystal Oscillator

An active crystal oscillator chip named F33.000 from JVC is adopted here. It works at 33MHz. The concrete realization of Crystal Oscillator is shown in Fig. 2.

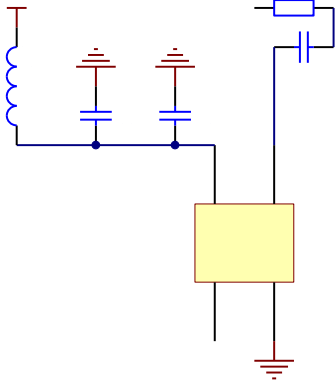


Fig. 2 Realization of Crystal Oscillator

B. PLL

The core chip is PLL400-915 whose working frequency is from 902 MHz to 928 MHz, and its center frequency is 915MHz. Its typical output phase noise is -111dBc/Hz, and the typical second harmonic suppression is -15dBc. The concrete realization of PLL is shown in Fig. 3.

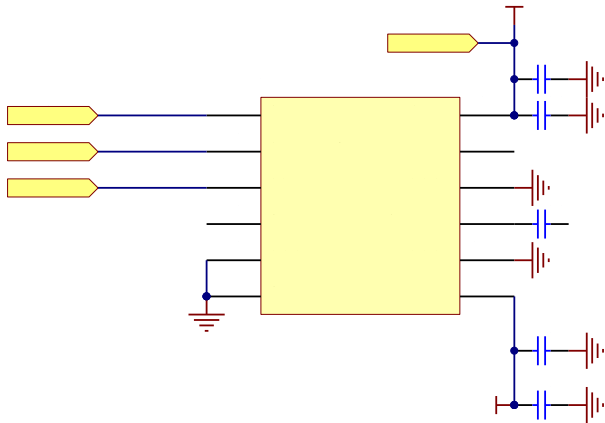


Fig. 3 Realization of PLL

C. Modulator

The chip of HMC194 is utilized here. It is a GaAs MMIC SPDT switch, and can control signals from DC to 3 GHz. It has been optimized to provide 50dB high isolation between two RF paths with minimal insertion loss of 0.7dB. The concrete realization of Modulator is shown in Fig. 4.

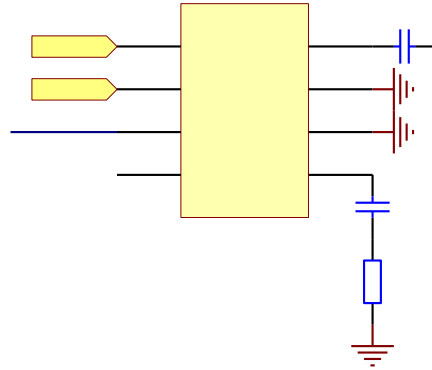


Fig. 4 Realization of Modulator

D. Power Amplifier

PF01411A is the core chip. The chip is a MOS FET power amplifier module, and a high gain 3 stage amplifier with 0 dBm input. It owns wide gain control range of 90 dB. The output power is 4.3W, and can be adjusted by pin V_{APC} . This is very important to change the reading range of WIR. The concrete realization of PA is shown in Fig. 5.

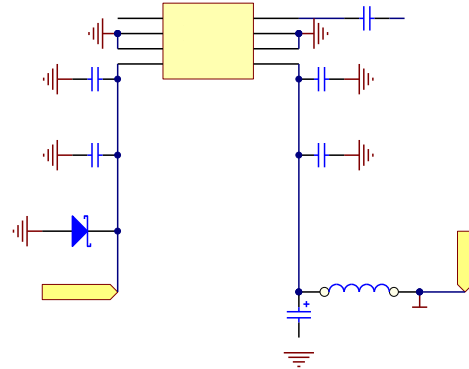


Fig. 5 Realization of PA

IV. TEST AND ANALYSIS

The scheme described in II and III has been implemented by 4-layer FR-4 PCB. The size of the PCB is 160mm \times 100mm. The picture of real RF product of WIR is shown in Fig. 6.

In Fig. 6, the upper part is the Transmitter, the lower part is the Receiver. In the upper part, from left to right, you can find the Crystal Oscillator, PLL, Modulator, PA, Circulator and the interface to the reader Antenna. In the lower part, from right to left, you can find the Demodulator, Differential Amplifier, and Comparator.

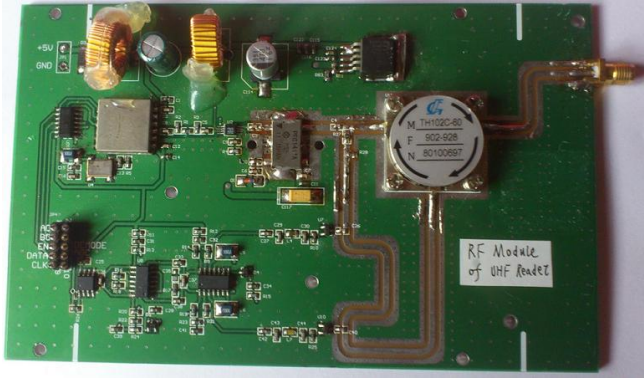


Fig. 6 Picture of real RF product of WIR

The waveforms of real RF product of WIR in Fig. 6 using oscilloscope are shown in Fig. 7. These two waveforms illustrate the VCC of PA (shown in yellow color) and the output of Circulator (shown in green color). They indicate that the working voltage of the PA is 4V, and that the output of Circulator (to the interface of the reader antenna) is the expected modulated signal. At the same time, the two waveforms have good synchronization performance.

The transmit power of the reader is up to 32dBm, and the stable reading range reaches 9 meters.

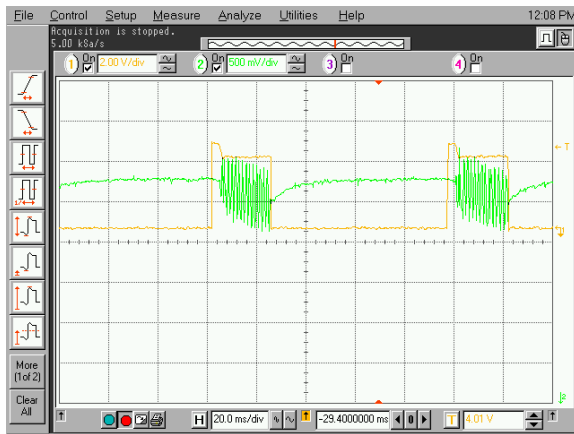


Fig. 6 Waveforms of 1) VCC of PA (shown in yellow color)
2) Output of Circulator (shown in green color)

V. CONCLUSION

In this paper, we have presented a zero-IF and modularization RF design scheme of WIR for UHF passive tags. The reader can work at 860-960MHz, and corresponds to the standard of EPC C1 G2 and ISO/IEC 18000-6C. We have elaborated the realization of some key modules. The

test have shown that the proposed RF module of reader work well. The transmit power of the reader is up to 32dBm, and the stable reading range reaches 9 meters.

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