Scrambling Code and Channelisation Code Parallel Generation for WCDMA on Vector Core

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***Abstract*—In a Wideband Code Division Multiple Access (WCDMA) environment, each user is assigned a unique complex-valued spreading codes to encode its information-bearing signal. The spreading sequence composed of scrambling codes and channelisation codes spread transmitted symbols and despread received chips. This essay presents the parallel generation method of scrambling code and channelisation code for WCDMA on vector core.**

Keywords- scrambling code;channellisation code;spreading code;parallel generation; WCDMA; vector core;

I. INTRODUCTION

The CDMA technology is widely used in 3G wireless communications. Scrambling code is used in WCDMA and CDMA2000.Channelisation code is used in WCDMA, CDMA2000 and TDS-CDMA. Scrambling code is generated from Gold sequence while channelisation code is generated from OVSF(Orthogonal Variable Spreading Factor) code[1]. The typical implementation methods of 3G system adopt the method of ASIC(Application Specific Integrated Circuit), which is optimal in the chip area and power consumption, while deficient in long design period, high cost, low flexibility, difficult upgradation and high design risk. Thus the advantage of ASIC chip is merged only in case of large quantity and regardless of chip cost. With the fast development of wireless communication, the 3G system like WCDMA, CDMA2000 and TDS-CDMA requires a multi-mode coexist with 4G system like TD-LTE and LTE-FDD in base stations or with WLAN and Bluetooth in terminal stations. And it will be a large waste in the chip area and power consumption if every system uses a ASIC chip. Besides, taking it into consideration that the typical evolution of 4G system requires continuous evolution of base station and terminal station chips, it will increase chip cost by using ASIC chips. To avoid those demerits, the SDR(Software Defined Radio) scheme defined by using RISC (Reduced Instruction Set Computer) should enjoy priority in developing base station chips that require low power consumption, rather than terminal station chips that require high power consumption. Yet, with the evolution and blending of those communication systems, alone with the mature application of VCORE(Vector Core), which is multi-core, efficient in power consumption and fast calculation, the SDR scheme of RISC technology will be a new trend of intelligent terminal chips with its advantage of low design period, low design cost, high flexibility, easy upgradation, low design risk, smaller chip area and low power consumption due to multi communication systems integration.

Mature research and application have come into use with the help of large and simple data processing by 4G system as TD-LTE/LTE-FDD , which are easily realized by VCORE. This essay discusses the technology of realizing 3G CDMA on VCORE. The transport channel encoding & decoding and physical channel transmiting & receiving in physical layer have the large amount of computation. The Convolutional code and Turbo code are used to transport channel encoding and decoding, which can be kept as hardware acceleration in vector core. While the physical channel transmiting and receiving vary in different communication systems, it is more reasonable for implementing in the vector core.. The spreading codes composed of scrambling codes and channelisation codes spread transmitted symbols and despread received chips. In this paper, it discusses the parallel generation method of scrambling code and channelisation code for WCDMA on vector core.

II. PSEUDO-RANDOM SEQUENCES

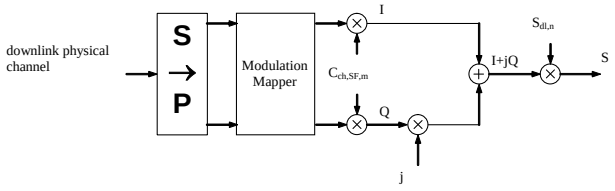
Pseudo-random sequences are sequences of 1s and 0s generated by an algorithm so that the resulting numbers look statistically independent and uniformly distributed. A random signal differs from a pseudo-random signal in that a random signal cannot be predicted. A pseudo-random signal is not random at all; it is a deterministic and periodic signal known to both the transmitter and the receiver. Even though the signal is deterministic, it appears to have the statistical properties of sampled white noise. To an unauthorized listener, it appears to be a truly random signal. Pseudo-random sequences are typically generated using a system of linear feedback shift registers (LFSRs). The LFSR generators produce a sequence that depends on the number of stages, the feedback tap connections, and the initial conditions.[2]

In a CDMA scheme, all users transmit on the same frequency and are differentiated by their unique spreading codes composed of scrambling codes and channelisation codes. The spreading codes appear to have the statistical properties of sampled white noise, so the spreading signal appear to have the statistical properties of sampled white

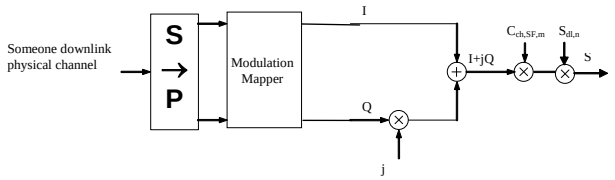
noise, which makes spreading signal easier to be transmitted in the wireless channel. The receiver correlates the received signal with a synchronously generated replica of the spreading code to recover the original information-bearing signal. [3] The third-generation partnership project (3GPP) specifications define how these downlink complex scrambling codes and channellisation codes are generated.

III. Spreading for WCDMA

In WCDMA downlink transmissions, all downlink physical channels are subjected to spreading with a complex-valued spreading code composed of scrambling code $S_{dL,n}$ and channelisation code $C_{ch.SF,.m}$. Fig 1(a) illustrates the spreading operation for all physical channels. Fig 1(b) illustrates the spreading operation for someone physical channel.The spreading operation includes a modulation mapper stage successively followed by a channelisation stage, an IQ combining stage and a scrambling stage.



(a) Spreading for WCDMA all downlink physical channels



(b) Spreading for WCDMA someone downlink physical channel

Fig. 1. Spreading for WCDMA downlink physical channels

The spreading codes maintain the orthogonal property and distinction between different channels in the same CELL in WCDMA , so as the WALSH CODE. First, we must recognize the different cells, and then distinguish different channels, and we should also minimize mutual interference between cells, therefore, the scrambling codes are introduced. Gold sequences are used as scrambling codes because Gold sequences have lower cross-correlation properties than M-sequence. OVSF Codes are used as channelisation code because their orthogonal property can distinguish different physical channels. The length of OVSF Codes varies with the data rate.

IV. Scrambling Code Generation for WCDMA

Scrambling code Typical Generation on Asic

The sequence of complex valued chips shall be scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$. A total of 2^{18}-1 = 262,143 scrambling codes, numbered 0…262,142 can be generated. However not all the scrambling codes are used. Only scrambling codes k = 0, 1, …, 8191 are used. Each of these codes are associated with a left alternative scrambling code and a right alternative scrambling code, that may be used for compressed frames. The left alternative scrambling code corresponding to scrambling code k is scrambling code number k + 8192, while the right alternative scrambling code corresponding to scrambling code k is scrambling code number k + 16384.[1]

The scrambling code sequences are constructed by combining two real sequences into a complex sequence. Each of the two real sequences are constructed as the position wise modulo 2 sum of 38400 chip segments of two binary m-sequences generated by means of two generator polynomials of degree 18. The resulting sequences thus constitute segments of a set of Gold sequences. Gold sequences have low cross-correlation properties to ensure as many users as possible to use the channel with minimum mutual interference .The scrambling codes are repeated for every 38400 chip. Let x and y be the two sequences respectively. The x sequence is constructed using the primitive (over GF(2)) polynomial $1+X^7+X^{18}$. The y sequence is constructed using the polynomial $1+X^5+X^7+X^{10}+X^{18}$.

The sequence depending on the chosen scrambling code number n is denoted z_n, in the sequel. Furthermore, let x(i), y(i) and z_n(i) denote the i:th symbol of the sequence x, y, and z_n, respectively.

The m-sequences x and y are constructed as:

Initial conditions:

- x is constructed with x(0)=1, x(1)= x(2)=...= x (16)= x (17)=0.
- y(0)=y(1)= … =y(16)= y(17)=1. (1)

Recursive definition of subsequent symbols:

- x(i+18) =x(i+7) + x(i) modulo 2, i=0,…,2^{18}-20. (2)
- y(i+18) = y(i+10)+y(i+7)+y(i+5)+y(i) modulo 2, i=0,…, 2^{18}-20. (3)

The n:th Gold code sequence z_n, n=0,1,2,…,2^{18}-2, is then defined as:

- z_n(i) = x((i+n) modulo (2^{18} - 1)) + y(i) modulo 2, i=0,…, 2^{18}-2. (4)

These binary sequences are converted to real valued sequences Z_n by the following transformation:

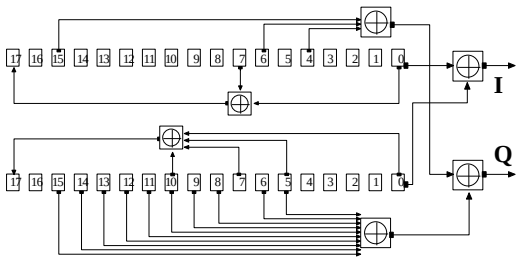
$$Z_n(i) = \begin{cases} +1 & \text{if } z_n(i) = 0 \\ -1 & \text{if } z_n(i) = 1 \end{cases} \quad \text{for} \quad i = 0,1,\ldots,2^{18}-2. \tag{5}$$

Finally, the n:th complex scrambling code sequence $S_{dl,n}$ is defined as:

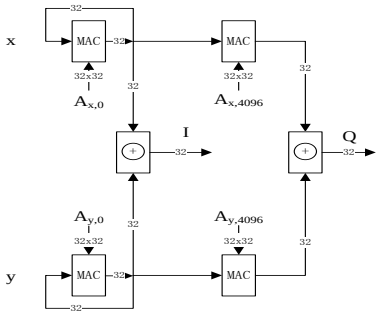
- $S_{dl,n}$(i) = Z_n(i) + j Z_n((i+131072) modulo (2^{18}-1)), i=0,1,…,38399. (6)

Note that the pattern from phase 0 up to the phase of 38399 is repeated. The m-sequences y initial value is independent of the n:th complex scrambling code.

Fig 2(a) illustrates the scrambling code typical LFSR generator on ASIC.



(a)Downlink scrambling code typical LFSR generator



(b) Downlink scrambling code parallel generator

Fig. 2. Downlink scrambling code generator

Scrambling code Parallel Generation on Vector Core

The scrambling code typical generation on asic is a chip-by-chip way, which is not suitable for fast generation and cannot use the fast calculation of vector core. The following introduces a scrambling code parallel gerneration which can be used on vector core. Let

$x_m=[x(m*32+31), \ldots,x(m*32+1),x(m*32)\ ]^T$ (7)

and

$y_m=[y(m*32+31), \ldots,y(m*32+1),y(m*32)\ ]^T$. (8)

The m-sequences x and y are constructed as:

Initial conditions:

- x_0=[0010 0000 0000 0100 0000 0000 0000 0001]^T=[2004 0001]^T. (9)
- y_0=[1001 1100 0000 0011 1111 1111 1111 1111]^T=[9c03 ffff]^T. (10)

Recursive definition of subsequent symbols;

- $x_m=A_{x,m}*x_0$ mod 2 (11)
- $y_m=A_{y,m}*y_0$ mod 2 (12)

$A_{x,m}$ is defined as:

- $A_{x,m}=A_{x,0}^m$ mod 2. (13)

$A_{y,m}$ is defined as:

- $A_{y,m}=A_{y,0}^m$ mod 2. (14)

Initial conditions:

$$A_{x,0}=\begin{bmatrix}4880\ 0000\\2440\ 0000\\1220\ 0000\\0910\ 0000\\0488\ 0000\\0244\ 0000\\0122\ 0000\\0091\ 0000\\0048\ 8000\\0024\ 4000\\8002\ 0000\\4001\ 0000\\4000\ 8000\\1000\ 4000\\8810\ 0000\\4408\ 0000\\2204\ 0000\\1102\ 0000\\0881\ 0000\\0440\ 8000\\0220\ 4000\\8100\ 0000\\4080\ 0000\\2040\ 0000\\1020\ 0000\\0810\ 0000\\0408\ 0000\\0204\ 0000\\0102\ 0000\\0081\ 0000\\0040\ 8000\\0020\ 4000\end{bmatrix},\quad A_{y,0}=\begin{bmatrix}DDDD\ 8000\\6EEE\ C000\\B7E3\ 4000\\DB65\ 8000\\6DB2\ C000\\B64D\ 4000\\DBB2\ 8000\\6DD9\ 4000\\B678\ 8000\\5B3C\ 4000\\AD0A\ 0000\\5685\ 0000\\2B42\ 8000\\15A1\ 4000\\8A44\ 8000\\4522\ 4000\\A205\ 0000\\5102\ 8000\\2881\ 4000\\94D4\ 8000\\4A6A\ 4000\\A5A1\ 0000\\52D0\ 8000\\2968\ 4000\\9420\ 0000\\4A10\ 0000\\2508\ 0000\\1284\ 0000\\0942\ 0000\\04A1\ 0000\\0250\ 8000\\0128\ 4000\end{bmatrix} \quad (15)$$

The n:th Gold code sequence z_n is then defined as:

- $z_n=x_{n,m}+y_m$ mod 2 (16)
- $z_{n+131072}=A_{x,131072}*x_{n,m}+A_{y,131072}*y_m$ mod 2 (17)

$A_{x,131072}$ and $A_{y,131072}$ can be respectively achieved from $A_{x,0}$ and $A_{y,0}$.

The $x_{n,m}$ is defined as:

$x_{n,m}=A_{x,m}*x_{n,0}$ mod 2, (18)

and $x_{n,0}$ can be merged from $x_{n/32}$ and $x_{n/32+1}$.

These binary sequences are converted to real valued sequences Z_n by the following transformation:

$$Z_n(i)=\begin{cases}+1 & if\ z_n(i)=0\\ -1 & if\ z_n(i)=1\end{cases}\quad for\quad i=0,1,\ldots,2^{18}-2. \quad (19)$$

Finally, the n:th complex scrambling code sequence $S_{dl,n}$ is defined as:

-$S_{dl,n}=Z_n+jZ_{n+131072}$ (20)

Fig 2(b) illustrates the scrambling code parallel generator on vector core.

V. CHANNELISATION CODE GENERATION FOR WCDMA

Channelisation Code Typical Generation on ASIC

For all physical channels (except SCH) in the WCDMA environment the I and Q branches shall be spread to the chip rate by the same real-valued channelisation code $C_{ch,SF,m}$, i.e. the output for each input symbol on the I and the Q branches shall be a sequence of SF chips corresponding to the channelisation code chip sequence multiplied by the real-valued symbol. The channelisation code sequence shall be aligned in time with the symbol boundary.[1]

The channelisation codes in WCDMA are Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between a user's different physical channels. The OVSF codes can be defined using the formula (21).The channelisation codes are uniquely described as $C_{ch,SF,k}$, where SF is the spreading factor of the code and k is the code number, $0 \le k \le SF-1$.

The leftmost value in each channelisation code word corresponds to the chip transmitted first in time.

$$C_{ch,1,0}=1$$

$$\begin{bmatrix} C_{ch,2,0} \\ C_{ch,2,1} \end{bmatrix} = \begin{bmatrix} C_{ch,1,0} & C_{ch,1,0} \\ C_{ch,1,0} & -C_{ch,1,0} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

$$\begin{bmatrix} C_{ch,2^{(n+1)},0} \\ C_{ch,2^{(n+1)},1} \\ C_{ch,2^{(n+1)},2} \\ C_{ch,2^{(n+1)},3} \\ \vdots \\ C_{ch,2^{(n+1)},2^{(n+1)}-2} \\ C_{ch,2^{(n+1)},2^{(n+1)}-1} \end{bmatrix} = \begin{bmatrix} C_{ch,2^n,0} & C_{ch,2^n,0} \\ C_{ch,2^n,0} & -C_{ch,2^n,0} \\ C_{ch,2^n,1} & C_{ch,2^n,1} \\ C_{ch,2^n,1} & -C_{ch,2^n,1} \\ \vdots & \vdots \\ C_{ch,2^n,2^n-1} & C_{ch,2^n,2^n-1} \\ C_{ch,2^n,2^n-1} & -C_{ch,2^n,2^n-1} \end{bmatrix} \quad (21)$$

The typical generation method for the channelisation code on asic is defined as Fig 3.

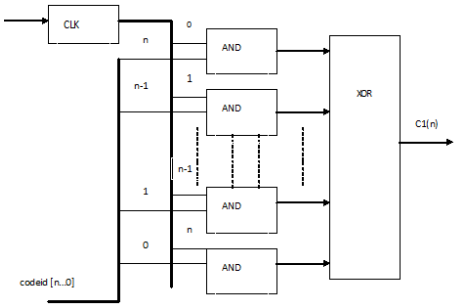


Fig. 3. Downlink channelisation code typical gerneration on ASIC

The channelisation code generator is composed of an n bit binary counter, n 'AND' gates and a 'XOR' gate. Firstly, the 'AND' gates are initialized by the channelisation code id in sequence which the least value in channelisation code id corresponds to the last 'AND' gates. Then, n bit binary counter counts from 0 to 2n-1 in sequence which the least value in counter corresponds to the first 'AND' gates. Finally, the outputs of every 'AND' gates perform 'XOR' operation bit-by-bit. The output of 'XOR' gate is the sequence corresponds to channelisation code id.

Channelisation Code Parallel Generation on Vector Code

If channelisation code parallel generation is implemented on vector core, the channelisation code are defined as:

$C_{ch,SF}=B*codeid \bmod 2$, (22)

$codeid=[C_{ch,SF,codeid}(0),C_{ch,SF,codeid}(1),\ldots,C_{ch,SF,codeid}(SF1)]^T$.(23)

When SF=32, B is defined as:

$B = [00\ 01\ 02\ 03\ \ldots\ 1e\ 1f]^T$. (24)

VI. SPREADING CODE GENERATION FOR WCDMA

In WCDMA Spreading is applied to the physical channels. It consists of two operations. The first is the channelization operation, which transforms every data symbol into a number of chips, thus increasing the bandwidth of the signal. The number of chips per data symbol is called the Spreading Factor(SF).The second operation is the scrambling operation .where a scrambling code is applied to the spread signal.

With the channelisation data symbols on so-called I-and Q-branches are independently multiplied with an OVSF code. With the scrambling operation, the resultant signals on the I- and Q-branches are further multiplied by complex-valued scrambling code, where I and Q denote real and imaginary parts, respectively. The spreading operation is defined as

$$R = \sum_{n=0}^{SF-1} S * (S_{dl}(n) + C_{ch}(n)) \quad (25)$$

Where SF is Spreading Factor, S is the transmitting complex-valued symbol, and R is the transmitting complex-valued chip after spreading operation. S_{dl} is the scrambling codes sequence, and C_{ch} is the channelisation code sequence.

The dispreading operation performs the reverse operation compared to the spreading operation. The despreading operation is defined as:

$$\hat{S} = \sum_{n=0}^{SF-1} R * \mathrm{conj}(S_{dl}(n) + C_{ch}(n)) \quad (26)$$

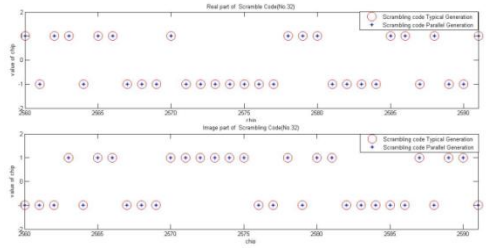
Where R is the received complex-valued chip, and S is the received complex-valued symbol after despreading operation.

If scrambling code and channelisation code parallel generation are used, the spreading and dispreading operation are defined as:

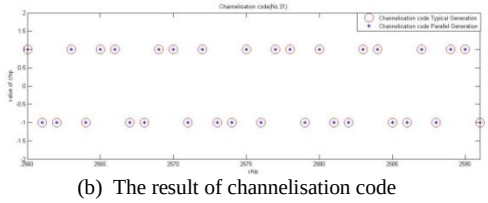
$$R = S * (S_{dl} + C_{ch}) \quad (27)$$

$$\hat{S} = R * \mathrm{conj}(S_{dl} + C_{ch}) \quad (28)$$

VII. RESULTS



(a)The result of real and image part of scrambling code



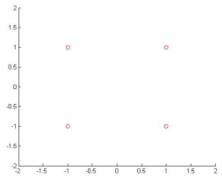
(b) The result of channelisation code

Fig. 4. The result of typical generation and parallel gerneration

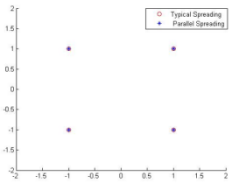
The plots in Fig 4(a) show the corresponding scrambling code typical generation and scrambling code parallel generation results for the complex scrambling code chip value. As these figures indicate, the scrambling code typical generation and scrambling code parallel generation results agree.

The plots in Fig 4(b) show the corresponding channelisation code typical generation and channelisation code parallel generation results for the complex channelisation code chip value. As these figures indicate, the channelisation code typical generation and channelisation code parallel generation results agree.

In Fig 4(a) and Fig 4(b), the x-axis represents the number of the chip, and the y-axis represents the magnitude of each of the chips. The complex scrambled signal obtained from the parallel generator matches the typical generator.



(a)QPSK Constellation Before Complex Spreading



(b) QPSK Constellation Map after Complex Spreading

Fig. 5. QPSK Constellation Before Complex Spreading

Fig 5(a) shows the signal constellation for the I-Q/code multiplexed signal before complex spreading, and Fig 5(b) shows the signal constellation after the complex spreading operations. The I-Q/code multiplexed signal with complex spreading results in a rotated QPSK constellation. Fig 5(b) shows the resulting constellation achieved by both the typical spreading and the parallel spreading.

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