Design of Highly Linearity Active Mixer for 4G RF Receiver

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Abstract—A down-conversion active mixer for LTE receiver is proposed, which focus on improving the traditional sub-threshold compensation method. The linearity is improved by adjusting the load inductance of transconductance stage and optimizing the phase of third-order transconductance coefficient; the noise is reduced with current injection technology. The designed active mixer is simulated with TSMC 0.18μm 1P6M CMOS technology. The results show that: the mixer can be operated at the 1.4-3.6 GHz band, and with the IIP3 of 5.6~ 10.7dBm, the SSB NF ranges from 9.4 to 13.6 dB, the gain ranges from -0.25 to 3.4 dB, the power consumption is 14.1mW with supply of 1.5V. The proposed mixer also has a merit of low NF and high linearity.

Keywords-4G; down-conversion; threshold compensation; current bleeding;linearity

I. INTRODUCTION

In recent years, with the growing demands for high quality of communication, the fourth generation of mobile communication (4G) has been proposed in 2009, which can provide high and fixed data rate with the adoption of MIMO and OFDM. The new communication system can operate at 1.4~3.6GHz and supports a variety of bandwidth allocations: 1.4MHz, 3MHz, 5MHz, 10MHz, 15MHz and 20MHz etc. Compared with 3G, the band width gets broader and data rate gets larger, so the requirements for hardware are increasing high also.

Linearity is an important parameter of the RF receiver, which determines the dynamic range of the input signal [2]. Linearity and the isolation between port and port decide the linearity and stability of the receiver. To improve the linearity, many different methods have been proposed in the literatures. The method biasing one of the transistors in strong inversion region and the other one in sub-threshold region in proper workplace to achieve the aim that the third-order transconductance closes to zero is adopted in [3, 4]. Then the *IMD*3 gets reduced and the linearity gets improved. However, this method requires a better level of the hardware circuit because of the external factors such as temperature which will cause zero drift. As we know zero drift can lead to floating of the *IMD*3. Even the design in the [4] just operates at 0.7-2.7GHz; [5] proposed a nonlinear compensation method that gets the *IIP*3 improved by 4.3 *dBm* with the using of *LC* folding load structure. However, the power consumption increases by 10%. [6] proposes a subthreshold MOSFET compensation method, with the principle of making two transistors connect two transistors connected in parallel in different workspaces, in order that both the third-order transconductances can be distributed on both sides of zero. Since the coefficients are vectors, they can be eliminated by adjusting the phase of vectors to reduce *IMD*3. But the design mainly works for the applications in the 2.4GHz. Also it can not be applied for broadband systems. When the frequency gets higher, the third-order transconductance can not be completely eliminated, leading to a worse performance of the *IIP*3.

This paper presents a high linearity mixer design which optimizes the subthreshold MOSFET compensation method by substituting tapped inductor for ordinary inductor. Then the phase of the Third-order transconductance will be eliminated with *IMD*2. The current bleeding technology also is adopted in this design to decrease the flick noise that produced from the common source node of the switch stage.

II. CIRCUIT ANALYSIS AND DESIGN

For the active mixer designed for LTE, most of them are based on the active Gilbert mixer structure [7, 8]. Fig.1 shows the mixer structure used in [6], which is the same with the circuit of the subthreshold MOSFET compensation method. The mainly work is optimizing the linearity of the transconductance stage. The following picture is the analysis of the circuit and the improvement program.

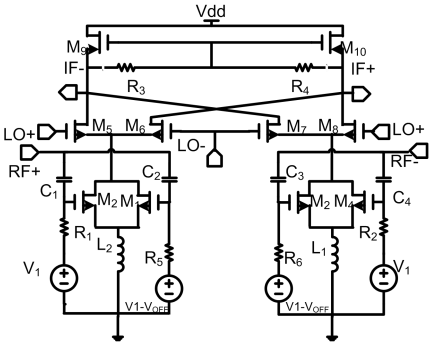

Figure 1. Mixer based on subthreshold MOSFET Compensation

A. Linearity Analysis

For a MOS transistor operating in the saturation region, the relationship between small signal leakage current and the gate voltage of the signal is given by:

$$i_d(v_{gs}) = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + ... \quad (1)$$

g_1 is the transconductance and g_2, g_3 are the higher order coefficients. Among them, g_3 has the greatest impact on the *IIP*3 .Without the case of the high frequency signal, the *IIP*3 can be simply expressed as:

$$A_{IP3} = \sqrt{\frac{4}{3} \cdot \left|\frac{g_1}{g_3}\right|} \quad (2)$$

g_3 mainly dependents on the gate-source (V_{gs}) and drain-source (V_{ds}) voltage. However, when the *MOS* transistor operates in the saturation region, the impact of drain-source voltage can be ignored, and then the each order of the transconductances coefficients can be expressed as:

$$g_1 = \frac{\partial I_D}{\partial V_{GS}} \quad g_2 = \frac{1}{2} \cdot \frac{\partial^2 I_D}{\partial V_{GS}^2} \quad g_3 = \frac{1}{6} \cdot \frac{\partial^3 I_D}{\partial V_{GS}^3} \quad (3)$$

When the transistor trans from weak inversion region or moderate inversion region to strong inversion region while under the action of V_{GS}, g_3 also changes from positive to negative.

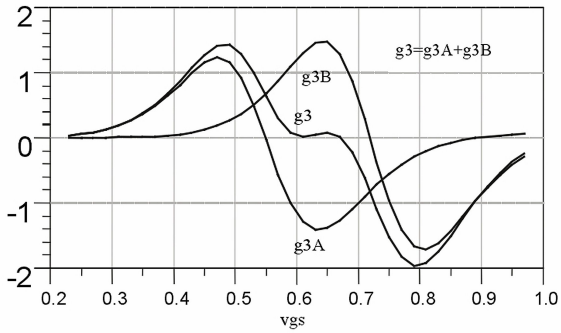

Figure 2. Third-order transconductance versus the bias voltage

As shown in the Fig .2, if the g_3 of one transistor is biased in the positive region, the other one is biased in the negative region. Then both of them can offset each other to get a combination of them, which is close to zero. Ideally, g_3 tends to be zero and A_{IP3} can achieve an infinite value. Fig. 3 shows the circuit arrangement:

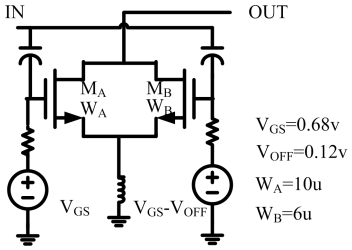

Figure 3. Subthreshold MOSFET compensated transconductance stage

M_A, M_B are biased in different regions, making sure that the transconductance of M_1, M_2 are located in strong inversion and weak inversion region respectively. So we can get, then g_{3A} and g_{3B} will mutually offset. The total output third-order transconductance can be expressed as:

$$g_3 = g_{3A} + g_{3B} \quad (4)$$

When V_{gs} is 0.63V, g3 tends to be zero. Then we can get a larger A_{IP3}. When considering the case of high frequency, Fig. 4 shows the small-signal model:

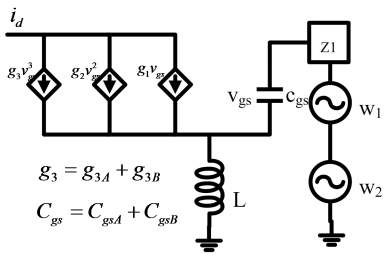

Figure 4. nonlinear small-signal model

In the small-signal nonlinear model, we neglect the impact of C_{gd}. All the *IMD*3 is produced in $g_3 v^3_{gs}$ when there is no *L*. The source inductor *L* forming a negative feedback circuit and the feedback gets more obvious impact on the high frequency signal. For example: the second harmonic generated by $g_2 v^2_{gs}$ will produce third-order intermediation signals, so the second harmonic can also generate nonlinear *IMD*3.

Since $\triangle\omega$ （$=\omega_2 - \omega_1$） is much smaller than ω_2 and ω_1, then we can get $j\triangle wL \approx 0$. When the circuit is matched to the signal source, we can obtain IIP3 as follows:

$$IIP_3 = \frac{4 g_1^2 \omega^2 L C_{gs}}{3|\varepsilon|} \quad (5)$$

$$\varepsilon = g_3 - \frac{2 g_2^2 / 3}{g_1 + \frac{1}{j2\omega L} + j2\omega C_{gs} + Z_1(2\omega)\frac{C_{gs}}{L}} \quad (6)$$

From (5) and (6), we can see that where *L* is the source inductor the ε cannot be zero even by setting the bias voltage only. In (6), the latter half is not only determined by the third-order transconductance. However, from the foregoing, the second harmonic generates again after mixing. In this regard, it is not effective to improve

*IIP*3 by relying on the DC circuit only.

By reducing the scale of the source inductor, we can reach the aim of improving the *IIP*3. However, the value of the Z_1 (2 ω) would get larger too. What's worse, the feedback of C_{gd} gets enhanced which leads to another frequency mixing which would contribute to *IMD*3. So simple to reduce value of the inductance is difficult to enhance *IIP*3. In [6], although the method has improved the linearity, as the inductance value is so small, the performance of the *NF* and the *VSWR* is not very satisfactory.

B. Noise Analysis

For *MOS*, *the* main sources of noise are the induced gate noise and the noise generated from the leakage current in the RF circuits:

$$\overline{i_{nd}^2} = 4kT\Delta f\gamma g_{d0} \tag{7}$$

$$\overline{i_{ng}^2} = \frac{4}{5}\frac{k^2T^2\Delta f\delta\gamma\omega^2C_{gs}^2}{I_{D.sat}\cdot q} \tag{8}$$

γ and δ are independent bias noise factor, and g_{d0} is the transconductance when V_{ds} equals to zero. When *MOS* is biased in strong inversion region:

$$g_{d0} = \frac{2I_{D.sat}}{V_{GS}-V_{TH}} \tag{9}$$

Where $I_{D.sat}$ is the drain current, V_{TH} is the threshold voltage. The two noise currents in equations (7) and (8) are partially correlated, and the correlation coefficient is:

$$c = \frac{\overline{i_{ng}\cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^*\cdot i_{nd}^*}}} \tag{10}$$

For long channel MOS transistor biased in saturated region, the γ and δ are 2/3, 4/3. For short channel transistors, γ and δ can be achieved 2-3 times than those. For simplicity, the short channel effect is ignored here. The γ and δ are derived as 1/2, 5/4. Since current of the transistor biasing in weak inversion is diffusion current, g_{d0} takes $I_{D.sat}$ / Φ_t, where Φ_t is the thermal voltage coefficient and equals to kT / q:

$$g_{d0} = \frac{I_{D.sat}}{\phi_t} \tag{11}$$

Take the (11) into (8), we can obtain:

$$\overline{i_{ng}^2} = 4kT\Delta f\delta\gamma\frac{\omega^2C_{gs}^2}{\frac{5I_{D.sat}\cdot q}{KT}} \tag{12}$$

$$= \frac{4}{5}\frac{k^2T^2\Delta f\delta\gamma\omega^2C_{gs}^2}{I_{D.sat}\cdot q} \tag{13}$$

What can be seen from the above equations, the induced gate noise in weak inversion region of the *MOS* transistor will decrease with the increasing of the diffusion current. Flicker noise in the strong inversion region of the transistor is [9]:

$$V_{1/f\_out} = \frac{4I_{LO}}{S\cdot T_{LO}}\frac{2K_N}{C_{OX}(WL)_{SW}}\frac{1}{f} + \frac{2C_P}{T_{LO}}\frac{2K_N}{C_{OX}(WL)_{SW}}\frac{1}{f} \tag{14}$$

The $S{\bullet}T_{LO}$ can be seen as 4*A*, where *A* is the amplitude of the oscillation. When the transistor is in strong inversion region, the flicker noise and leakage current fall in a negative correlation. In the circuit designed of this paper, as the use of current injection technology, the current source Shares the current by 60%, reducing the impact of the flicker noise:

III. MIXER CIRCUIT DESIGN

The mixer circuit structure that has been improved is shown in Fig. 5:

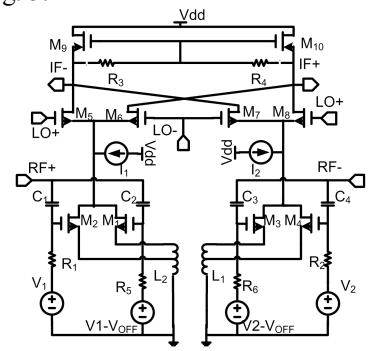

Figure 5. the proposed improved mixer circuit

In this circuit configuration, M_9~M_{10} are the loads; M_5~M_8 are switch stage transistors, which are the input terminal of oscillation signal; R_1~R_6 are protection resistors;V_1,V_1-V_{OFF} are the bias voltages; C_1~C_4 are blocking capacitors; M_1~ M_3 are biased in the saturation region; M_2~M_3 are biased in the subthreshold region; L_1~L_2 are tapped inductor. By adjusting the access inductance values of M_2~M_3, the phase deflection of third-order transconductance can be achieved.

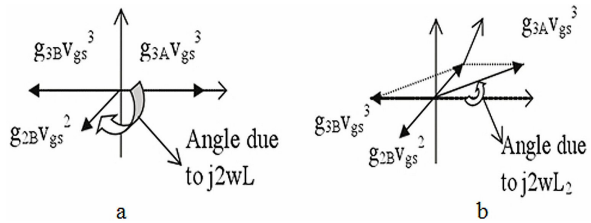

Figure 6. the phase deflection of third-order transconductance

Fig. 6(a) shows the second and third transconductance phase diagram. Fig. 6(b) shows those of the circuit proposed in this paper. Compared with chart (a), by adjusting the access value of the tapped inductor, we can change phase direction of the third-order transconductance. Then the phase of the third transconductance of M_1 and M_2 can be rotated to be eliminated. The linearity gets improved. I_1~I_2 are current sources.

IV. MEASUREMENT RESULTS

The designed MIXER was manufactured in a 0.18 μ m *CMOS* technology. In order to evaluate the mixer performance, external matching circuit was designed. As the tapped inductor was adopted, the value of the *IMD*3 was drastically reduced, leading to the greatly enhance of *IIP*3. As shown in the fig. 7, the *IIP*3 increases by 4*dBm*, reaching to 10.7*dBm* with the adoption of the tapped inductor. At the same time, the current injection structure shares the current by 2.8*mA*, so that the current of the switch stage can be greatly reduced, which could optimize the performance of the *NF*. Fig. 8 shows the *SSB NF*, from

which we can see that the *NF* gets decreased by 5.5*dB* and becomes more flat. Although the power consumption increased by 28%, but relative to the improvements of the performance, the sacrifice is still quite valuable. In the frequency range from 1.4 to 3.6GHz, the consumption is 14.1*mW*, while with a supply voltage of 1.5*V*. Fig. 9 shows that the *RF* and *LO* input reflection coefficient are located within the scope less than-10dB. Fig. 10 shows that the conversions gain curve with *LO* power, from which we can see that the peak position of the gain varies with the operating frequency. In order to balance the performance of the parameters, here we take the oscillator power at -7*dBm*. From the figure we can see that the conversion gain range from -0.25 to 2.4 *dB*. TABLE Ⅰ compares the performances between the proposed mixer and the mixer in the literature.

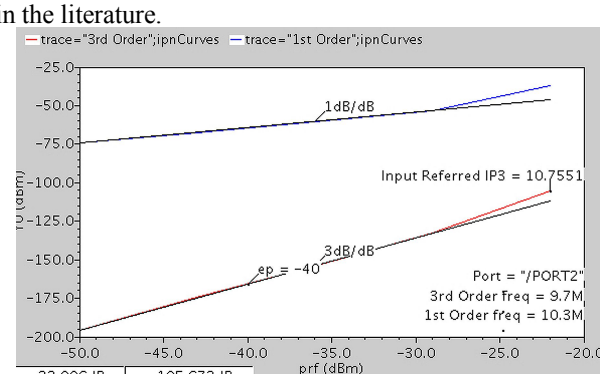

Figure 7. (a) IIP3 improved

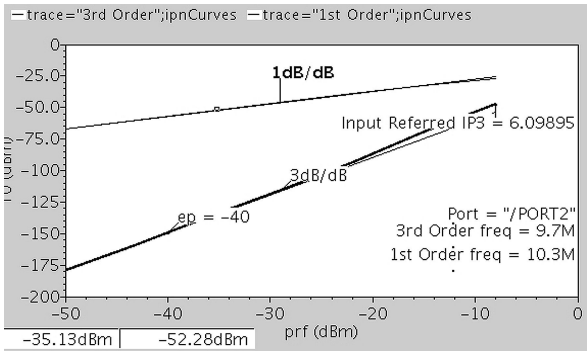

Figure 7. (b) IIP3 before improved

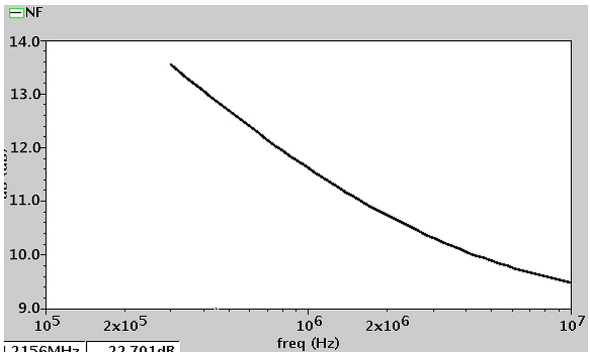

Figure 8. (a) SSB NF improved

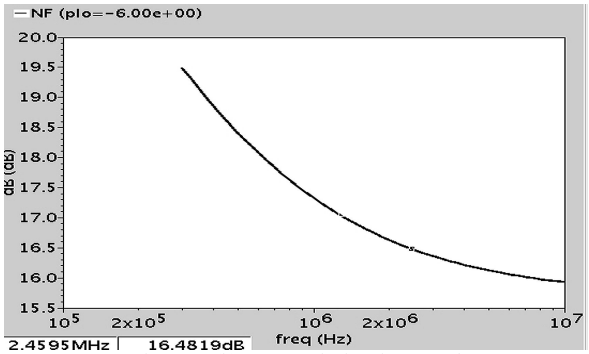

Figure 8. (b) SSB NF before improved

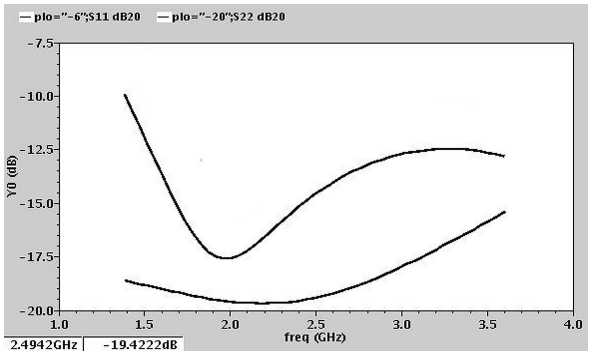

Figure 9. (a) RF S11，L_O S22

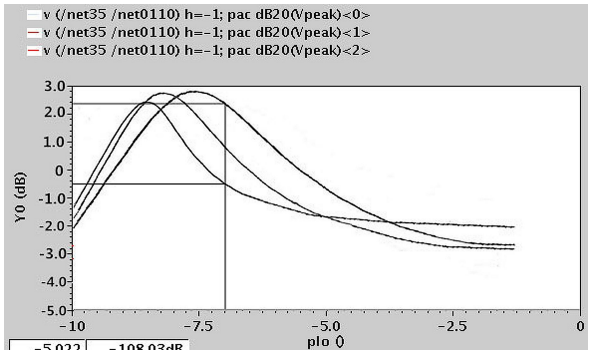

Figure 10. Conversion gain versus LO power at different frequencies

TABLE I. PERFORMANCE COMPARISON OF DIFFERENT MIXER PUBLISHED IN RECENT YEARS AND THIS WORK

	ref[10]	ref[11]	this
Tech (*um*)	0.13	0.18	0.18
Vol（V）	1.2	1.2	1.5
f_{RF}(GHz)	1.4~3.6	1.4~3.6	1.4~3.6
f_{LO}(GHz)	1.39~3.59	1.39~3.59	1.39~3.59
P_{LO}(*dBm*)	N/A	-8	-7
IIP3(*dBm*)	-13~-10	-0.5~2.6	5.6~10.7
P_{-1}*dB*(*dBm*)	N/A	-12.9~13.9	-11.53~2.3
Gain(*dB*)	6.5~7	4.3~6.9	-0.25~2.4
NF_{SSB}(*dBm*)	2.7~6.5	20.8~23.2	9.4~13.6

V. CONCLUSION

In this paper, subthreshold MOSFET compensation method was analyzed and improved: By replacing the ordinary inductor into tapped inductor to optimize the feedback of the transconductance stage, which purpose is to adjust the phase direction of the transconductance, so that the sum of the transconductance coefficients closes to

zero to improve the linearity. The use of the current injection technology effectively reduces the noise factor. The stimulation results show that: the linearity of the proposed mixer gets improved by 4*dBm*; the single-sideband noise figure decreases by 5.5*dB*, which is suit for the application of the *LTE*.

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