

# Virtual Input Method Real-time Detection System Based on Multi-core Digital Image Processing Technology

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**Abstract**—Parallelizable processing mechanism and multi-core architecture characteristics of image processing algorithm are studied. On the basis, image processing algorithm parallel design paradigm based on multi-core computing environment with five design procedures of analysis, modeling, mapping, debugging and performance evaluation as well as test publishing is proposed. Image Fourier transform parallel algorithm design is adopted as an example to verify the validity of the parallel paradigm. Meanwhile, a virtual input method based on digital image processing, operated in embedded system is also proposed. Camera equipment attached to embedded equipment is utilized for collecting image in user key pressing process on virtual keyboard. Keys are identified through corner-point identification and image segmentation in order to position target keys clicked by user through collected image, thereby realizing information input process. Experimental results show that the paradigm can expand application space of image processing in the aspect of image processing parallel design, thereby providing reference treatment method for interaction design of embedded equipment.

**Keywords**- virtual; digital image processing; software layer; Multi-core; Paradigm

## I. INTRODUCTION

In recent years, a variety of brand-new interactive methods are launched. The study of parallel image processing algorithms under multi-core computing environment has obtained more and more attention with the development of multi-core processor technology. Traditional design method and programming mode based on parallel machines and parallel cluster algorithm are not applicable under the multi-core computing environment, therefore it is very important to study common parallel design paradigm under the multi-core architecture[1-3]. Meanwhile, since various input methods based on keyboards always keep the most important positions, research of related work is mainly divided into two aspects at present: optimization study based on traditional keyboard and research of virtual input method alternative technology[4]. It is difficult to completely reproduce traditional keyboard in a limited space with deep popularization of embedded equipment, therefore various virtual input methods quickly become

concerned hotspots, namely realization of character or information input by the mode expect non- entity keyboard. When most virtual input methods adopts sensor for replacing traditional keyboards currently, it has the biggest drawback that additional cost and power consumption control are increased[5]. Parallel image Fast Fourier Transform algorithm under multi-core environment is designed and realized for verifying effectiveness of paradigm based on digital image processing algorithm parallel design paradigm according to the above problems in the paper. Other virtual input methods require additional cost, the current problem was overcome to some extent, and it can be promoted further in other fields.

## II. SUMMARY OF RELATED WORK AND METHODS

At present, research of keyboard-related technology is mainly divided into two aspects of traditional keyboard optimization design and virtual input method research. The former is mainly used for hardware transportation on existing entity keyboard, key position distributions are adjusted, and input efficiency is improved through regional mapping and other methods. Additional virtual keyboard has the following main problems: additional cost is greatly improved, special requirements are proposed on production process. Meanwhile, the method is lack of real key feeling and positioning sense[6-7]. Input speed and user experience are affected to certain extent. Additional virtual keyboards are mostly used as experimental products due to the lack of practical value. Camera capture tools are generally embedded with improvement of embedded equipment function. Therefore, virtual input method without additional sensing device is proposed in the paper aiming at market demand for virtual input product and insufficiency of current virtual keyboards. Firstly, one pseudo keyboard with painted keyboard schematic symbols is provided for user firstly, and user can input and click on the pseudo-keyboards with finger. Meanwhile, camera capture device on the embedded equipment can process projection of the finger on the pseudo-keyboards, thereby identifying the clicked keys, wherein the pseudo-keyboards only can provide positioning information and providing uses with visible area. It can be made of various materials.

### III. TECHNICAL INDICATORS AND DETECTION PRINCIPLES OF SYSTEM

Input recognition depends on whether drilled positioning holes are divided into porous type or non-porous type or not. Concrete type is determined according to different translucence of different applied films. Therefore, the system should have good compatibility. Wavelength of lighting source should not be less than 900nm in order to ensure input safety[8]. System software should be designed to meet production flow of testing and finishing workshop. Film shot by CCD camera through high-speed image acquisition card can be displayed on computer display under the condition that the infrared light source provides suitable and even lighting conditions. Meanwhile, images collected by system software should be analyzed and treated. Defects can be separated from film base background to reach detection purpose through image smoothing and image segmentation methods according to principle that gray scale of image obtained after light irradiation on film basis is different.

### IV. MULTI-CORE ARCHITECTURE DESIGN

Multi-core CPU refers that many CPU cores are integrated into a single chip. Each CPU is regarded as one independent processor. All CPUs share one unified address space with separate L1 Cache. Multi-level Cache structure is adopted. Bus or Crossbar is adopted as interconnection structure. Cache coherence protocol is

used for maintaining data consistency. Multi-thread or multi-process is adopted as parallel software design method. Parallelism of multi-core processor is divided into instruction-level parallelism, thread-level parallelism and simultaneous multi-thread. Wherein, thread-level parallelism is mainstream parallel technology of multi-core processor. Each multi-core processor can support thread parallel implement with equal quantity as core quantity under the condition of not adopting Hyper-Threading technology[9-10]. The action provides realization environment for parallel execution of procedure. In addition, communication among cores is completed through sharing memory, thereby completely solving communication delay among nodes in parallel cluster.

### V. OVERALL DESIGN AND PROCESSING FLOW

Virtual input method based on digital image processing technology is proposed in the paper. Images collected by camera device is processed and analyzed for establishing virtual keyboard model of abstraction space. Text symbol input method of mobile equipment is realized. It is assumed that the equipment has video capture function. The equipment is provided with one virtual keyboard for positioning. Finger can enter image acquisition area along fixed direction during input operation. The method is realized based on the precondition of the above assumption. It is provided with overall architecture figure shown in Fig .1.

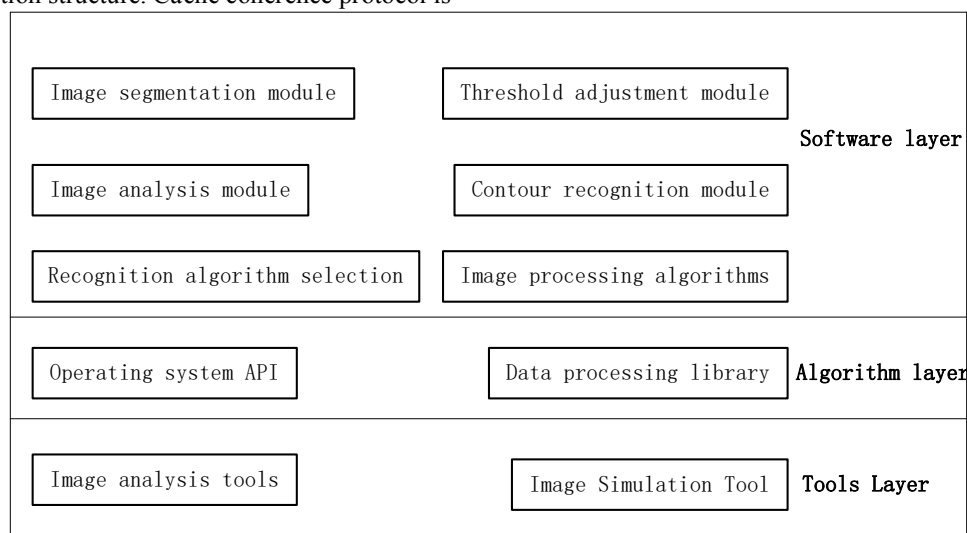


Figure 1. System Overall Architecture

Related embedded equipment, pseudo keyboard with video acquisition tool in line with positioning requirement (i.e. entity virtual keyboard) are demanded for realizing the method as hardware support. Video capture, threshold selection, corner-point recognition, image segmentation and other operations are completed in order under the support of related operation system and image processing library. The processed images can be analyzed for obtaining corresponding key information, and virtual input method can be realized. Implementation steps of the method are shown in Fig .2, namely keyboard recognition, image capture, image segmentation and key identification, wherein keyboard

recognition belongs to preparation action. Characteristic shape of keyboard can be utilized in the process for establishing basic coordinate space.

Pseudo-keyboard is set into a rectangular area in order to avoid loss of generality. Three black identification points are available, which are respectively located on three top corners of the rectangle, namely left upper corner, left lower corner and right upper corner, thereby identifying effective keyboard area. Line segment groups parallel to the sides are used for dividing the rectangle into M lines and M rows. They are used for representing keys as many as M \* M. Camera equipment can be firstly turned on firstly during system operation,

user can input after calibration and key recognition, and camera equipment can collect effective image. Secondly, the extracted image is binarized, corner points are recognized, geometric distortion is corrected, etc. Interested area ROI can be obtained by segmentation, namely effective area of real keys. Effective judgment images can be selected from images obtained from continuous sampling, which can be binarized. Finally, the effective images after binarization can be retrieved and analyzed for obtaining keyboard placement information and recognizing placements. The above operations are circulated for completing the input process, wherein, image segmentation, geometric distortion correction and key placement recognition are key problems that should be realized in the method.

## VI. IMAGE PROCESSING ALGORITHM PARALLEL DESIGN PARADIGM UNDER MULTI-CORE COMPUTING ENVIRONMENT

Massive algorithms of image processing are analyzed in the paper according to characteristics of multi-core architecture. Design paradigm of digital

image processing parallel algorithm under multi-core computing environment is proposed. The paradigm divides parallel design of digital image algorithm into five steps: serial algorithm hotspot analysis, parallel modeling, mapping to multi-core architecture, debugging and performance evaluation as well as testing release. When the procedure is implemented, only main thread exists, serial part of main thread implementation procedure can execute other parallel parts through deriving other threads. When the serial part of the procedure is re-implemented, the thread will be terminated. Mapping of parallel design algorithm to dual-core, quad-core, eight -core and multi-core computing environment can be conveniently realized through the process. Therefore, mapping of parallel algorithm to multi-core architectures can be realized in the paradigm. After mapping of parallel paradigm to multi-core architecture is realized, algorithms after parallel implementation can be debugged, errors should be eliminated, and performance should be analyzed aiming at debugging and performance evaluation and concrete process is shown in Fig .2.

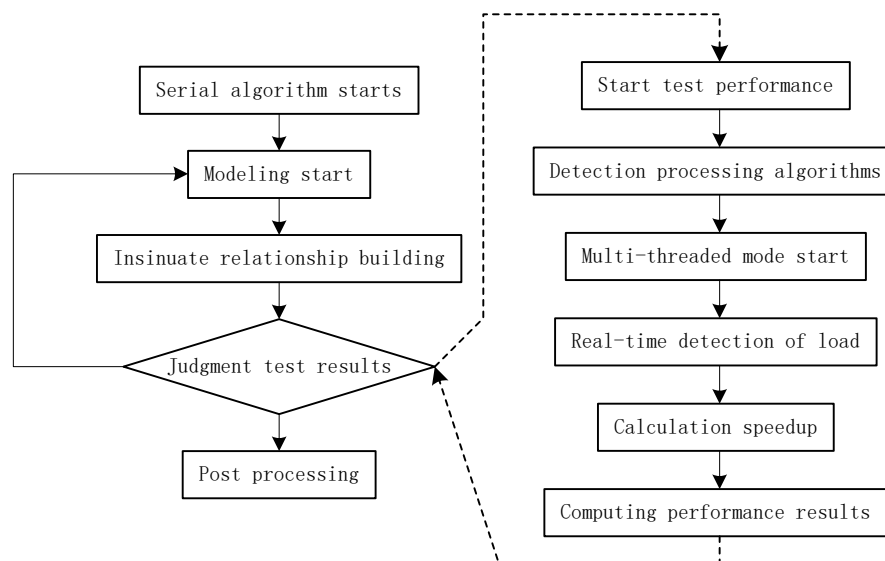


Figure 2. Paradigm Design Performance Evaluation Flow chart

After the above procedures are completed, it should be mapped to multi-core architectures. After parallel modeling of algorithms is completed, the parallel algorithms should be mapped on multi-core architecture. Multi-core architecture can realize parallel implementation of algorithm through multi-thread parallel execution. Communication and data exchange can be realized directly through shared memory among threads. Performance loss due to communication delay among nodes is solved compared with the parallel cluster. Parallel execution model is shown in Fig .3. Parallel algorithms should be debugged, and errors should be eliminated, including solution of thread synchronization and load balancing problem. Multi-core

architecture uses shared memory mechanism, which may lead to data competition aiming at access of shared memory. Procedure results depend on two core more thread implementation time order by undetermined mode. Data competition problem can be solved through thread synchronization mode. In addition, load balance problem due to parallel execution is also important factor affecting algorithm execution time. In addition, algorithm operation time can be reduced by balancing calculation load of all procedures. It is very important to evaluate parallel algorithm performance, and speedup ratio is an important indicator to evaluate performance of parallel algorithms.

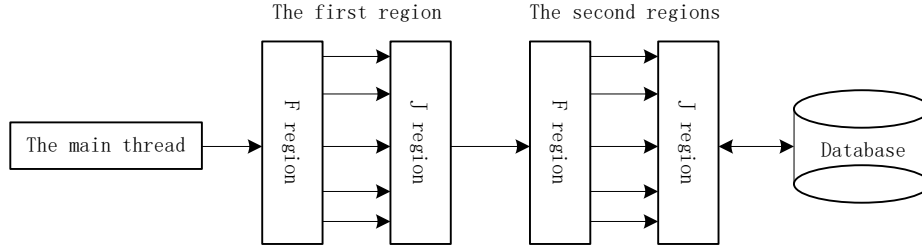


Figure 3. Parallel Mechanism Execution Model Design

## VII. TEST RESULTS

Performance of parallel two-dimensional FFT algorithm is tested under multi-core environment and traditional single-core environment. In the paper, thread quantity opened under different calculation environment is equal to the core quantity of processor in the paper.

TABLE I. TIME STATISTIC TABLE

Resolution	The time for different resolution/ms			
	Mononuclear	Dual-Core	Quad-Core	Eight nuclear
512*1024	304.4	67.2	35.2	17.3
1024*1024	2012.3	453.7	206.6	104.2
512*2048	5365.4	2198.7	832.4	238.1
1024*2048	9438.4	3845.2	843.2	321.3

Data in Table 1 show that the two-dimensional FFT time is significantly shortened under multi-core environment. Speedup ratio curves produced by pictures in different sizes on four platforms are shown in Fig .4. Fig .4 indicates that each speedup ratio curve has linear increasing trend along increase of core quantity in processor under experiment environment. The speedup

Processing time of image with different dimensions under different environments is timed in the experiment, and average execution time can be obtained according to ten experiment results. The experiment result is shown in table 1.

ratio reaches 14.2 especially under eight-core environment. The experiment result shows that two-dimensional fast Fourier transform algorithm reached linear speedup ratio after parallel design, wherein pictures with  $1024 \times 1024$  pixel can achieve the best acceleration effect under multi-core environment.

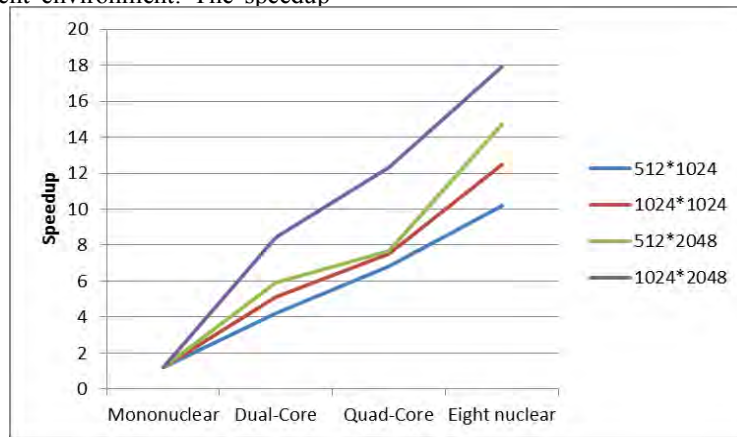


Figure 4. Speedup Ratio Curve of Various Pictures

## VIII. CONCLUSION

In the paper, application status of multi-core processor and important role of input method are firstly analyzed, thereby basic description of related research work and method is proposed. Then, system technical indicator and test realization principles are designed. Multi-core architecture and implementation process are designed on the basis. Excellent digital image processing paradigm is designed and realized accordingly. In the paper, digital image processing algorithm parallel design paradigm under multi-core computing environment is

proposed. Parallel computing ability of multi-core processor is fully utilized. Concept of image recognition input method is launched, and excellent input method detection system is designed. The method in the paper is a typical application of image processing technology and embedded system. Experimental results show that the paradigm is easy to understand and convenient for application with high versatility and good test results. Meanwhile, the paper has the shortcoming that it is difficult to recognize continuous press of one key, in addition other keys are swept during finger forward and backward movement process on keys, thereby easily

leading to wrong recognition. Therefore, correction of threshold decision method, calibration of geometric distortion algorithm, improvement of effective key image recognition and other aspects can be focused in next work, thereby improving recognition precision, expanding shooting angle, and associating with existing input method thesaurus for realizing linked input. Meanwhile, applicable scope and accuracy of paradigm can be further improved for solving decreased parallel algorithm performance and other problems due to increased picture scale.

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