Ultra High Definition Stereo Video Format Conversion System of Multi View

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Abstract. With the improvement of display manufacturing technology ,4K LCD of Ultra High Definition resolution emerges as the times require.In order to realize five view auto-stereoscopic display on 4K LCD and make people get the more shocking stereo vision from multi angle,a five view Ultra High Definition stereo video format conversion system was proposed in this article.This system uses Kintex-7 FPGA as the main processing chip,completes a series of image processing functions combined with the HDMI input and output card.And finally a strong 5 view stereo display on 4K LCD without loss of resolution is achieved.

1. Introduction

Nowadays, more and more stereoscopic products come into our daily life. They can be used in many aspects of society, such as education, science, entertainment, medical industry, aerospace field, military training, architecture modeling and etc.Especially,with the improvement of display manufacturing technology,4K LCD of Ultra High Definition resolution comes into our daily life[1].If we can realize five view auto-stereoscopic display on 4K LCD,people will get more shocking stereo vision[2].

However,the traditional software algorithm processing speed is too slow,not stable,and costs high..If we can break through these limitations,develop a ultra high definition stereo video format conversion system of multi view which has low cost,high speed,strong stability,it will have a great significance [3].This paper has developed a system,it uses Kintex-7 FPGA as the main processing chip[4],completes a series of image processing functions combined with the HDMI input and output card.Finally a strong 5 view stereo display on 4K LCD without loss of resolution is achieved[5].

2. Description of the Xth view

Generally,there are two ways for the acquisition of multi-view images,by rendering or by photographing. Both of the ways, 5 cameras(camera1,camera2,camera3,camera4,camera5) are located at 5 different positions with reasonable interval space, as shown in Figure 1.

Fig.1 Camera arrangement for multi-view images

Camera1~5 individually produce image,the Xth camera captures the Xth view image,then view image 1~5 may be gotten,as shown in Figure 2.

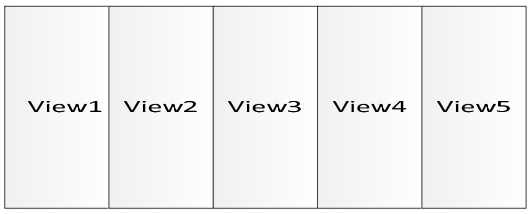

Fig.2 view arrangement of 5 view

3. Principle of the system

The system is ultra high stereo video format conversion sytem of five view,it consists of five physically separated components.They are PC, HDMI1.4 input card[6],Kintex-7 FPGA board,HDMI1.4 output card,4K LCD. the overview of the whole system is shown in Fig.3.

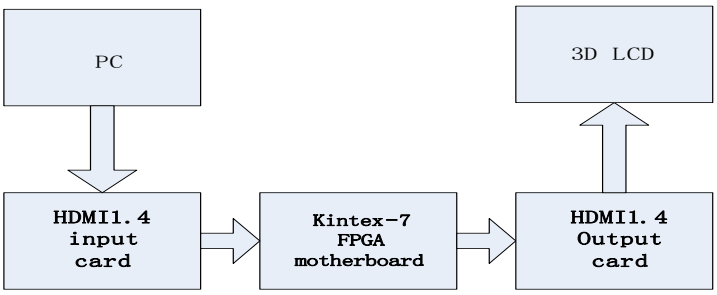

Fig.3 Ultra high definition stereo video format conversion system based on FPGA

Among them ,the video processing capacity of HDMI1.4 input card and HDMI1.4 output card is 3840*2160@30Hz.Firstly,PC output the full view format video source,the full view format video source is composed of five single view format video source,and the five single view format video source is arranged from left to right as shown in Figure 2.

The full view format video source from PC gets into HDMI1.4 input card,then the output video of HDMI1.4 input card gets into the Kintex-7 FPGA motherboard.The transform algorithm from the full view format video to five view auto-stereoscopic format video is completed inside Kintex-7 FPGA .After conversion algorithm,the five view auto-stereoscopic format video gets into the HDMI1.4 output card.Finally,the five view auto-stereoscopic format video is displayed on 4K LCD,then a strong 5 view stereo display without loss of resolution on 4K LCD is achieved.

3.1 The Ultra High Difinition Stereo Video Format Conversion

The output video format of HDMI1.4 input card is full view format,which has the resolution of 3840*2160.In order to realize the conversion from the full view format video to five view auto-stereoscopic format video,we have developed the Scaler algorithm[7],the 90 degree image rotation algorithm [8]and the five view image fusion algorithm.

The Scaler algorithm mainly completed the pixel amplification from the HDMI1.4 input siganl.That is,we finally get 2304 lines from 2160 lines through the Scaler algothrim.The mininum Scaler unit expanded 15 pixels to 16 pixels. The 90 degree image rotation algorithm mainly rotates the image after Scaler 90 degrees clockwise.Then the first view is in 0-767 line,the second view is in 768-1535line,the third view is in1536-2303 line,the fourth view is in 2304-3071 line,the fifth view is in 3072-3839 line.The five view image fusion algorithm mainly fusion the five view image according to the 5view fusion mode of 4K LCD.

4. FPGA control principle of the 5 view stereoscopic video format conversion

In the five view ultra high definition stereo video format conversion system,These requirements must be met : the high video stream processing speed,enough storage resources and the IP cores can meet the design requirements[9].Therefore,we choose the Kintex-7 FPGA based on 28nm technology as the main processing chip. A detailed block diagram inside the FPGA is shown in Fig.4.

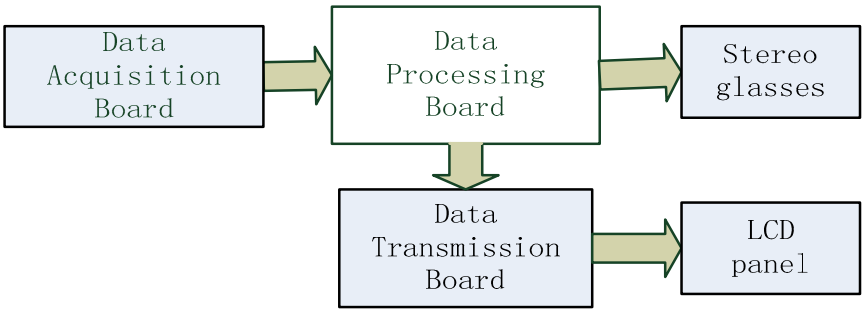

Fig.4 Block diagram inside FPGA

The video processing algorithm inside Kintex-7 FPGA mainly includes a clock generation module :CLK_GENERATOR, HDMI input control module :HDMI_2_DDR3,HDMI_4K2K timing generation module:Video Timing Generator,HDMI output control module: DDR3_2_HDMI,DDR3 memory control module: MIG, serial communication module : UART_TOP,HDMI input register configuration module : HDMIRX_REG_CFG, HDMI output register configuration module : HDMITX_REG_CFG.

4.1 Clock Generation Module and Video Timing Generation Module

Clock generation module CLK_GEN produced FPGAinternal clock signal and reset signal[10].It receives 200MHz on-board crystal oscillator clock, generates a 148.5MHz pixel clock to the HDMI output control module in DDR3_2_HDMI.Once the system is on power,the reset signal function as a global reset,so that the whole system is in the initial predictable state.The timing generation module is used for HDMI output control module DDR3_2_HDMI,which generates the HDMI 4K2K timing of the HDMI output interface,controls the fusion pixel output.

The HDMI output video timing is shown in Fig.5

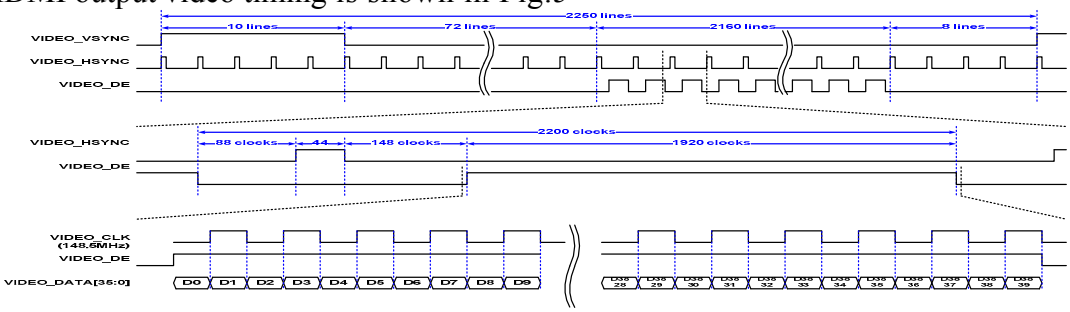

Fig.5 The HDMI1.4 output video timing

4.2 HDMI input control module HDMI_2_DDR3

Figure 6 shows the algorithm diagram of the HDMI input control module.This algorithm adopts Ping pang switch,one buffer is used as write buffer,the other buffer is used as read buffer.So that Ping pang switch can avoid write-read conflict[11].In order to realize 90 degrees rotation,Rotate Control module completes these functions:put the n(0-3839)column pixel address into the corresponding n line address inside DDR3 SDARM[12].Besides,write the effective pixels to DDR3 SDARAM with AXI4 bus timing.

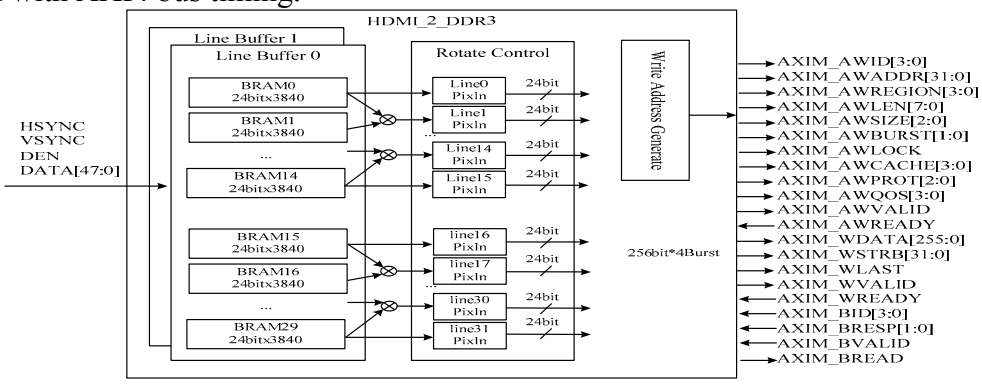

Fig.6 The HDMI input control module

4.3 HDMI output control module DDR3_2_HDMI

HDMI output control module realize three functions:1.generate 4K2K video timing,namely Video Timing Generator in Figure 8,so that the HDMI output interface can display the right pixels. 2.generate the AXI4 bus timing,read the 5 view pixels from DDR3 SDRAM .3. Read out the fusion pixels based on 4K LCD 5 view fusion mode.Figure 7 shows HDMI output control module.

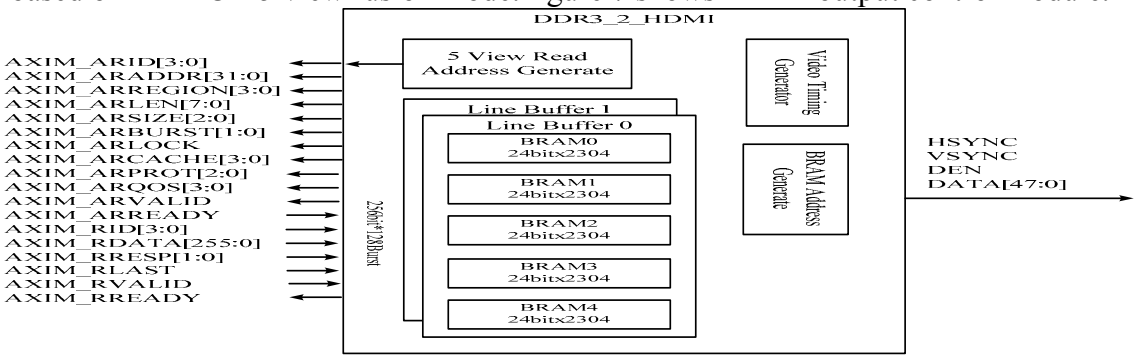

Fig.7 The HDMI output control module

4.4 HDMI input register configuration module and HDMI output register configuration module

HDMI input register configuration module HDMIRX_REG_CFG, HDMI output register configuration module HDMITX_REG_CFG respectively using IIC protocol to configure the HDMI1.4 video decoding chip and HDMI1.4 video encoding chip.

5. Experimental results

A set of system was established as Figure 8.First of all,the PC graphics output full view format video,this full view format video get into HDMI input card,the Kintex-7 motherboard completes the conversion algorithm from full view format image source to five view stereo format image.The five view stereo format image gets into HDMI output card.At last,the multi view stereo format video was displayed on 4K LCD. A shock stereo vision was achieved.

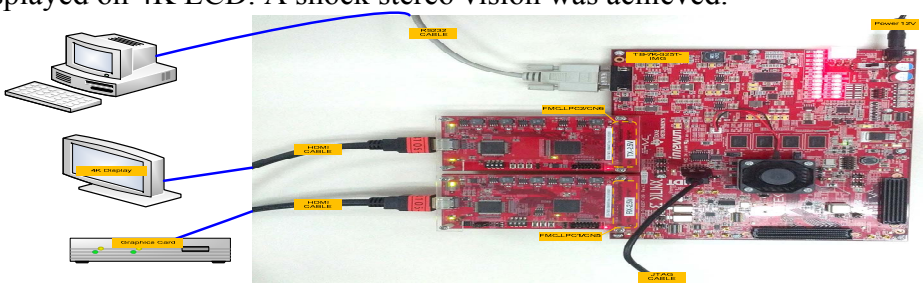

Fig.8 The system establishment

The full view format image before fusion is shown in Fig.9. The 5 view stereo format image after fusion is shown in Fig.10.

Fig.9 the full view format image

Fig.10 The 5 view stereo format image

6. Conclusions

This paper proposed a ultra high definition stereo video format conversion of five view. It meets people's need on multi view stereo format video on 4K LCD in a situation that 4K LCD are more

and more popular.Compared with tradictional software algorithm,this system has many advantages: low cost,strong stability,high speed and so on.From the previous sections we can see,this system can process high speed ,large capacity video stream via som technologies.The system test result also indicated that,this deign worked perfectly inside Kintex-7 FPGA.The system can be used in military field, medical field, home audio field, the field of machine vision, our future work is to optimize the design, design a better stereo video format conversion system board.

Acknowledgments

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Reference

[1]http://www.digitaltrends.com/home-theater/everything-you-need-to-know-about-4k-ultra-hd/

[2]Dodgson,N.A.(2005). Autostereoscopic 3D displays.Compute,38(8),31-36.

[3] Fei Zuo, Harm Belt, Marcel Krijn and Siebe Zwart,"Enabling eye-contact for home video communication with a Multi-view Autostereoscopic Display", Consumer Electronics (ICCE), 2010 Digest of Technical Papers International Conference, Jan. 2010, pp. 47 - 48.

[4]http://www.xilinx.com/products/silicon devices/fpga/kintex-7/

[5]Dodgson,N.A,Moore JR,Lang SR. Multi-view autostereoscopic 3D display[C]//International Broadcasting Convention. 1999, 99.

[6] http://www.hdmi.org/manufacturer/hdmi_1_4/4K.aspx

[7] Tao F, Wen-Lu X, Lian-Xing Y. An architecture and implementation of image scaling conversion[C]//ASIC, 2001. Proceedings. 4th International Conference on. IEEE, 2001: 409-410.

[8] Banerjee, S. ; Kuchibhotla, A. Real-time optimal-memory image rotation for embedded systems , Image Processing (ICIP), 2009 16th IEEE International Conference on , Publication Year: 2009 , Page(s): 3277 - 3280 .

[9] Istvan Andorko, Peter Corcoran, Petronel Bigioi, "Hardware implementation of a real-time 3D video acquisition system", Optimization of Electrical and Electronic Equipment (OPTIM), 2010 12th International Conference, May 2010, pp. 920 - 925.

[10]“Proposed VESA and Industry Standards and Guidelines or Computer Display Monitor Timing”, Version 1.0, Revision 12p, Draft 3, www.vesa.org.

[11] KANG Yan-xia, CAO Jian-zhong, TIAN Yan, CHE Rong, SUN Lei, "Ping-pang cache structure in real-time video processing system", Journal of Projectiles, Rockets, Missiles and Guidance, vol. 27, No. 4, 2007, pp. 218-221.

[12]“2G bits DDR3 SDRAM DATASHEET”, http://www.deutron.com.tw/pdf/D3_128x16.pdf.