A Novel Fast Transient Response Low Dropout Regulator with Multi-Loop Control Technique (MLCT)

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Keywords: Low-dropout regulator; transient response; low quiescent current; power management

Abstract. A new multi-loop controlled low dropout (LDO) regulator featuring with improved transient response and low quiescent current is presented in this paper. The proposed Multi-Loop Control (MLC) technique adopting both feed-back and feed-forward control methods to realizes the fast response ability by regulating the load current and output voltage through separate loops rapidly. In addition, adaptive controlled current tails are used to reduce the quiescent current. The proposed regulator is implemented in a 0.35um CMOS process. Simulation results show that, MLCT improves the line and load transient responses obviously, while maintaining low quiescent current and high current efficiency.

Introduction

The low dropout (LDO) regulators are widely used in a variety of electronic systems to provide the power from battery efficiently due to their low noise and small size [1-2]. In these applications, fast transition responses are required to keep their output voltage within a limited range. However, the trade-off among quiescent current (IQ), low-voltage operation, precision and transient responses imposes critical challenges on the design of LDO [3].

Various strategies have been discussed to resolve this problem recently [4-9]. LDO regulators with added current control loops are conceptually simple, have relatively fast transient responses to both line and load perturbations [4-5]. Unfortunately, to ensure a current-based control regulator can operate properly, a large equivalent series resistance (ESR) is usually required which causes loop instable problems [6]. As a result, LDO topology that combined Q-reduction compensation [7] and adaptive biasing [8-9] achieves the features of low quiescent current and extended loop bandwidth, are proposed. However, there is a trade-off exists between the biasing factor and stability according to the loop gain analysis. To overcome the problems mentioned above, a novel multi-loop control method is proposed as shown in Fig.1.

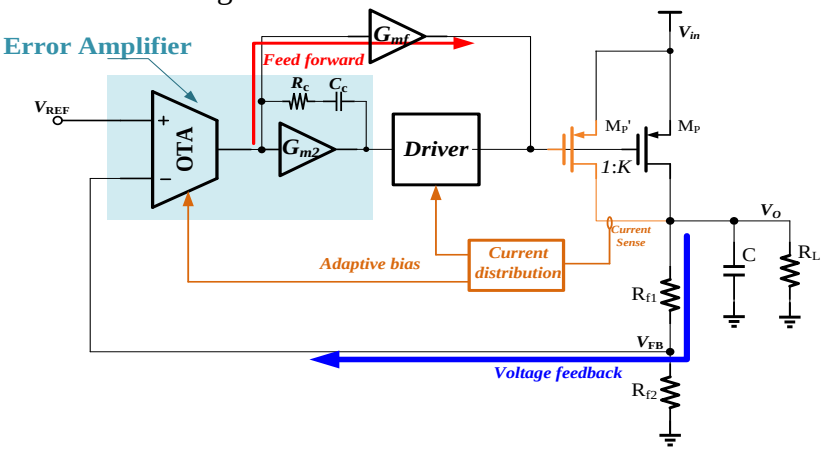


Fig.1 System architecture of the proposed MLCT LDO

Proposed MLCT Technique

The main concept of the proposed LDO topology is to increase the loop gain, loop bandwidth and slew rate at the gate of the power transistors adaptively. The LDO is composed of an error amplifier, driver, two parallel power transistors MP and MP', and a current sensing and distribution block.

As shown in Fig.1, there are three control loops in the proposed LDO, which are the feed-forward loop, the voltage control loop, and the current control loop respectively. The voltage control loop is the general case in the traditional LDO. The feedback voltage VFB is sent into the error amplifier (EA) and compared with reference voltage VREF. The added current control loop is fed by a current mirror (the feedback current IC is proportional to the load current IL) to adjust the bias current of EA and driver. Because the feedback path of the current control loop is faster than voltage control loop, as a result, the transient response is superior to conventional one. Moreover, the feed-forward loop is able to regulate the power transistor MP' when the input voltage or the load is varying.

Current sensing and distribution (CSD) is fed by a simple mirror, which can sense the change of load current and control the bias current to be proportional to the load current to improve the bandwidth and slew rate with high current efficiency. Therefore, In addition to the small fixed biasing currents Ib1 to the EA and Ib2 to the driver, the second adaptive bias currents Ic1 and Ic2 proportional to the load current are to the EA and driver respectively. So, at heavy loads, the larger bias currents of EA and driver increases the bandwidth of EA and slew rate at the gate of power transistors, whereas a smaller bias current maintain a high current efficiency when the load is light. Thus, this LDO topology can improve the transient response with high current efficiency. What's more is the feed-forward loop that adjust the smaller power transistor's output resistance directly and firstly to smooth the output voltage VOUT's variation when the load current varies and then the bigger power transistor supply the required current to the load quickly due to the adaptive bias current of EA and driver. Therefore a LDO with fast transient response with high current efficiency can be achieved.

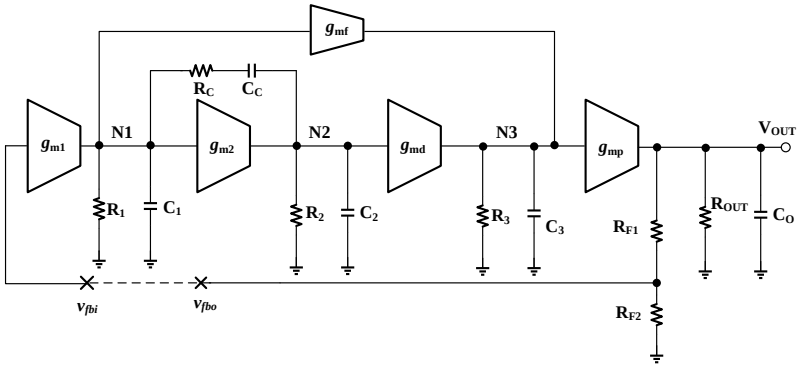


Fig.2 Small-signal model of proposed LDO

Fig. 2 depicts the small-signal model of the proposed LDO, consider the loop breaking at VFB, whereby a small input vfbi is injected into the gate of M2. The proposed LDO have to stable at all load conditions. The loop gain from is approximately given by:

$$T(s)=\frac{v_{fbi}(s)}{v_{fbo}(s)}=\frac{A_0\{1-s[(C_C/g_{m2})-R_CC_C]\}}{(1+sR_3C_3)(1+sR_{out}C_O)(1+bs+cs^2+ds^3)} \tag{1}$$

Where

$$A_o=g_{m1}g_{m2}g_{md}g_{mp}R_1R_2R_3R_{OUT}\frac{R_{F2}}{R_{F1}+R_{F2}} \tag{2}$$

$$b=(C_2+C_C)R_2+(C_1+C_C)R_1+g_{m2}R_1R_2C_C+R_CC_C \tag{3}$$

$$c=[R_1R_2(C_1C_2+C_CC_1+C_CC_2)+R_CC_C(R_1C_1+R_2C_2)] \tag{4}$$

$$d = R_1 R_2 R_C C_1 C_2 C_C \tag{5}$$

The whole LDO is shown in Fig. 3, which shows the detailed schematic of proposed LDO using Miller compensation (CC and RC). High precision output voltage requires a high-gain EA that can be realized by a multistage amplifier. The two-stage EA consists of M1– M12. Current source Ib1 provides the small bias current for EA. The Miller capacitor CC and series resistor RC are connected between the output node of the first stage cascode amplifier N1 and the output node of EA N2.M14, M15 and two small bias current resources form the power transistor driver.

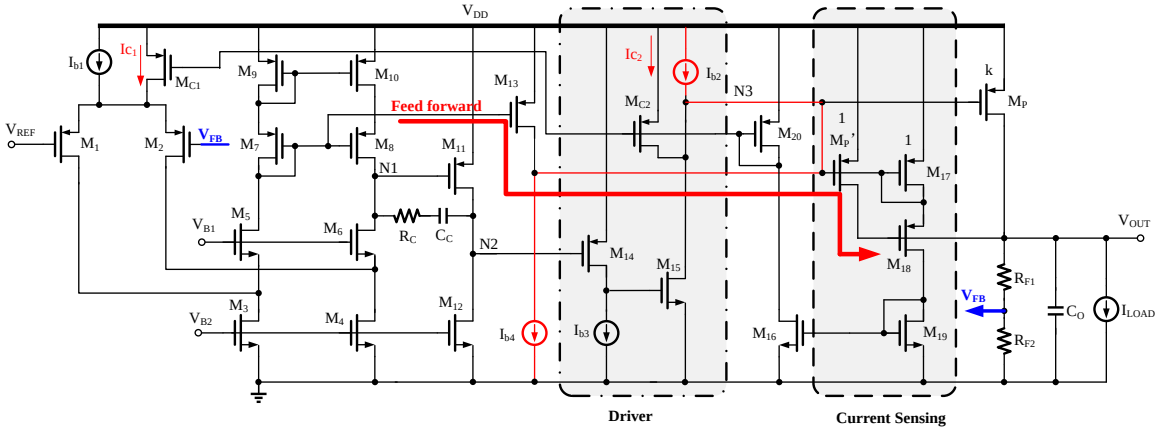


Fig.3 Schematic of proposed LDO

Results and Discussion

The LDO converter with MLCT technique was implemented in a 0.35μm CMOS process. The layout is shown in Fig.4, and the layout of the power MOS MP and its proportional transistor MP' which occupies about 59um*55um is shown in Fig.5. Simulation and measurement results have been carried out in order to establish the correct and stable operation of the proposed technique.

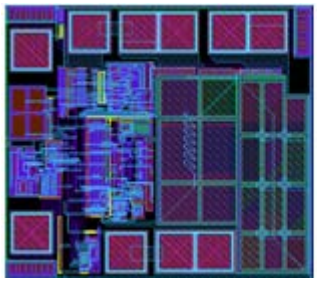


Fig. 4 Layout of the proposed LDO

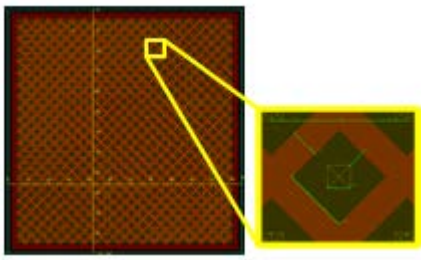


Fig. 5 Layout of the power MOS MP

Fig.6 shows the transient response for the 0-200mA transition, the amplitude of the ringing is less than ±95mV and setting time is approximately 5us. Fig.8 presents the frequency response of the proposed LDO. From Fig.7 (a), it is clear that the final LDO had full range stability with a GBW product greater than 300kHz. As shown in Fig.8 (b), the phase margin under these comers SS, FS, ST, TT and FF exceeds 30°.

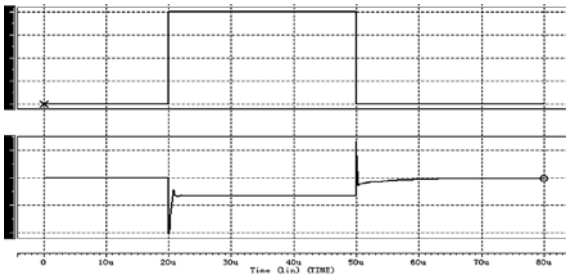
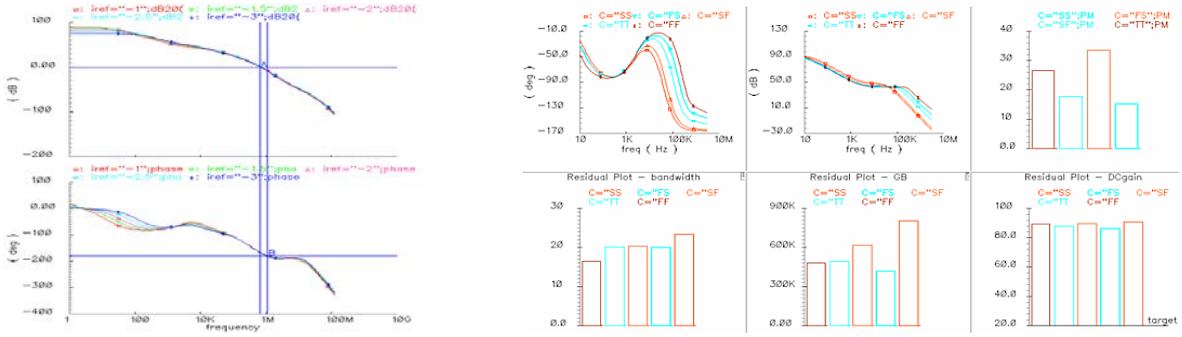


Fig.6 Simulated transient response



(a) Full range open-lop ac response simulation (b) Corner analysis

Fig.7 Frequency response of the proposed LDO

Conclusion

This paper proposes a MLC technique to improve the transient response and minimize the quiescent current of LDO. The feed forward loop successfully enhances the LDO's transient response and the current distribution block minimizes the quiescent current. And the current control loop improves the regulation accuracy. Test results verified the effectiveness of the MLC technique.

Acknowledgement

This work is supported by the National Natural Science Foundation of China (50977077, 51277149).

References

[1] N. Schemm, S. Balkir, and M. W. Hoffman, The design of an ultra-low power buck regulator supporting dynamic voltage scaling for wireless sensor networks, in Proc. IEEE Int. Symp. Circuits and Systems ISCAS 2009, 2009, pp. 828–831.

[2] Leung K N, Mok P K T. A capacitive-free CMOS low-dropout regulator with damping-factor-control frequency compensation. IEEE J Solid-State Circuits, 2003.

[3] Robert J Milliken. Full on-chip CMOS low-dropout voltage regulator, IEEE transactions on circuits and systems: regular papers, vol. 54, no. 9, Sep 2007.

[4] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sanchez-Sinencio, High PSR low drop-out regulator with feed-forward ripple cancellation technique, IEEE J. Solid-State Circuits, vol. 45, no. 3, pp. 565-577, Mar.2010.

[5] T. Coulot, E. Rouat, F. Hasbani, J.-M. Fournier, and E. Lauga, Highpower supply rejection low drop-out regulator for ultra-low-powerradiofrequency functions, IET Elec. Lett., vol. 47, no. 20, pp.1117–1118, Sep. 2011.

[6] Chave CK, Silva-Martininez: A frequency compensation scheme for LDO voltage regulators, IEEE Trans. Circuit and System I, vol.6 pp.1041-1050 June 2004

[7] Chenchang Zhan ,Wing-Hung Ki. Output-Capacitor-Free Adaptively Biased Low-Dropout Regulator for System-on-Chips. IEEE transactions on circuits and systems , vol. 57, pp.1017-1028, May 2010

[8] C Zhang, Z.J Yang and Z.P Zhang: Proc. International Conference on ASIC (Xiamen, China, October 25-28, 2011). Vol.978, p.918.

[9] Mohammad R. Hoque: Proc. The World Congress on Engineering and Computer Science (San Francisco, USA, October 22-24, 2008). Vol.2173, p.173.