Hardware System Design of Two story Intelligent Ethernet Switch

Fang Yuan[1,2,a], Wei Jiang[1,2,b], A-di Xi [1,2,c] and Jing Cui[1,2,d]

[1]Engineering Research Center of Nuclear Technology Application Ministry of Education, East China Institute of Technology, Nanchang, Jiangxi, China

[2]State Key Laboratory Breeding Bases of Nuclear Resources and Environment,East China Institute of Technology,Nanchang, Jiangxi, China

[a]455302348@qq.com, [b]jw186@163.com, [c]fyuan@ecit.cn , [d] 531339974 @qq.com

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Abstract. This paper designed a two-story intelligent Ethernet switch hardware system in order to meet the needs of Ethernet users. The system includes the secondary power supply module, CPU interface module, switching module, reset module, clock module and POE module. The experiment proved that the intelligent Ethernet switch has good performance and has broad market prospects.

Introduction

With the rapid development of VoIP, WLAN, network video surveillance technology, making the emergence of Wireless LAN AP, IP Camera, IP Phone and other IP terminal devices. The equipment is usually more than the number, routing data and power lines is more complex, more difficult to take power equipment, but also increases the cost of network construction, and building a network delay time. The two-story Smart Switch with POE function can solve every IP device installed on a separate power supply network terminal equipment problems, makes it unnecessary equipment deployed in the field for a separate power supply systems and large effortlessly, can greatly reduce the deployment and management costs wiring terminal equipment to bring, thus promoting the rapid development of related fields [1-4].

Hardware circuit design floor Smart Switch

Layer smart switch hardware system design with POE function as shown in Figure 1, the hardware part of the switch is mainly composed of several parts of the secondary power supply module, CPU module, switch module, reset module, clock module, POE modules and other components.

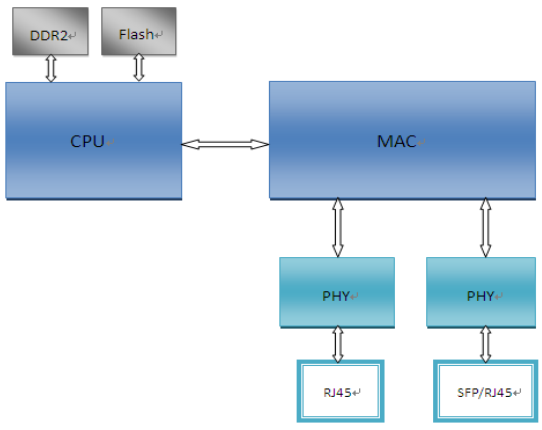

Fig.1 Structure of Switches

Secondary power supply module

The whole of the supply can be divided into primary and secondary power supply, a power supply is independent of the PCB board, turned 220V power supply voltage required by the PCB, switches with POE function, a 220V power supply needs to be transferred for two-way voltage, which way is converted into 12V power supply to the motherboard PCB, another way to convert 52V power POE function board. A secondary power supply on a PCB is converted into the 12V voltage necessary for the respective devices of the power supply.

Depending on the choice of the IC, the design needs to 3.3V, 2.5V, 1.8V, and a voltage of 1V, it is possible to select a reasonable 12V power conversion into chip to complete the work, the frame portion of the secondary power source drawing board.

Stability of the secondary power supply to the entire system is very important, into the desired device in 12V voltage when the voltage to each channel filtering to reduce the impact of ripple and noise on the machine, but also to consider to a power timing issues, the power requirements of the order is based on each of the major components needed to be adjusted to ensure the normal operation of the whole system of power. According to the power requirements of the major chip work on power-up sequence is 3.3V, 2.5V and 1.8V power simultaneously, whereas last 1V power. The time interval between 3.3V and 1.8V is less than 50ms.

CPU Module

Marvell's MAC 98DX1035 is integrated with the CPU, 98DX1035 through the interface can be an external DDR2, EEPROM, and Flash, CPU subsystem components. In 98DX1035 in its selection and configuration of the reference clock is pulled up or pulled down by the pins to achieve, clock 35MHz, with different types of memory interface 98DX1035, you can connect through different types of memory to achieve the system function, directly by external Flash as a boot device and its interior during boot ROM is disabled, external DDR2 and data buffers are run as system software code.

Switch Module

The system is composed by a PHY 88E3083, 88E1322 98DX1035 and switching subsystem, the design diagram shown in Figure 5. 98DX1035 through SSSMII interface 88E3083, SGMII interface is connected through to the interface through an SMI 88E1322, 98DX1035 88E1322 88E3083 and managed, MAC continue reading PHY through SMI bus status register to know the current state of the PHY, such as connection speed, duplex capabilities. You can also set the PHY registers to control purposes by SMI, such as opening and closing flow control, auto-negotiation mode or forced mode.

Clock Module

In this switch, the clock is more roads, such as CPU, MAC, PHY and other chips are needed clock. Active with 25 MHz crystal to give 98DX1035 and Gigabit PHY 88E1322 provides the clock, while the other 3 Mbps PHY 88E3083 chip's clock is provided by 98DX1035, the clock frequency is125MHz.

Reset module

In the system, including the use of reset button reset, power-on reset, software reset, JTAG reset, PHY reset, POE reset button reset, power-on reset, software reset. These methods can provide a reset signal resets the entire system, PHY reset the main PHY chip provides a reset signal, POE reset is a reset signal to the CPU for POE module provides for. Button reset signal is connected to 98DX1035 of GPP3, when you press the reset button when the switch restarts.

Reset signal generally has 3.3V pull GPIO output a reset signal for the CPU, due to the power, CPU has not yet started, and the signal will remain high. To avoid possible cause unreliable reset.

General reset signal is connected to the Buffer or the door and then output to the chip, rather than directly to the CPU and ASIC reset directly connected.

POE module

POE PD module via a cable to the power supply, in order to ensure that PSE can have good compatibility, to detect PD, PD and connect the power supply, PD monitor connected, PD disconnected. Start, PSE device small voltage output port until it detects a connection to a cable terminal supports the IEEE 802.3af standard receiving end device. PD terminal equipment Category: After receiving end device PD is detected, PSE device may be classified as a PD device, and the power required assessing the loss of this PD devices.

Start power: in a configurable period of time to start, PSE device starts from a low voltage power supply to the PD device until provides 48V DC power supply. Power supply: 48V to provide a stable and reliable DC power to PD device, the device does not meet the PD across 15.4W power consumption. Off: If the PD device is disconnected from the network, PSE will quickly stop for the PD power and repeat the detection process to detect the cable terminal is connected PD devices.

When connecting any network device to PSE, PSE must detect the device is not PD, in order to ensure that no equipment does not conform to the Ethernet standard POE provides current, it may cause damage. Such checks are provided by a cable to a small current-limited voltage to check whether the remote has a characteristic resistance to meet the requirements to achieve. It will be provided only to detect the resistance of all 48V voltage, but the current is still limited, in order to avoid terminal equipment in the wrong state. As an extension to the discovery process, PD can also require a power supply PSE classification, helps to PSE provides power in an efficient manner. Once the PSE started to provide power, it will continuously monitor PD current input, when PD current consumption drops to a minimum value, such as when you unplug the equipment or experience in the PD power consumption overload, short circuit, over load, such as power supply PSE, PSE will disconnect the power and start the testing process again.

PSE is allowed to line power before it must be tested with a limited power source to check the characteristics of the resistance, in order to avoid the 48V POE power is applied to the non-compliant network devices, inflicting harm. Before powering, PSE first used to detect the voltage of 2.8V ~ 10V to detect whether PD access. Once detected a valid PD, PSE need to understand the PD's power consumption, ease of system management of power, a process known as PD classification. This stage, PSE using a voltage 15.5V ~ 20.5V probe to detect the power level PD. Absorbed by a constant current from the line - grading characteristic signal, PD maximum power to the PSE show that they need. PSE measuring this current, in order to determine the PD belongs to which power level. PSE voltage source to be used during the grading is limited to 100mA, the failure to prevent damage to PD, and it can not exceed the connection time 75ms, in order to control the power consumption of the PD.

Summary

This paper presents the second floor of intelligent Ethernet switch hardware systems, including some of the secondary power supply module, CPU subsystem modules, switching subsystem module, reset module, clock module, POE module, the hardware system is practical, efficient data high-speed transmission provides a strong and stable guarantee.

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