An Efficient Acquisition Architecture for BOC-modulated Signal

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Abstract. Due to large search space and multiple peaks of autocorrelation function, fast acquisition of BOC- modulated GNSS signal is a time and resource consuming task. In this paper, a novel hardware architecture for BOC-modulated signal acquisition is proposed. The proposed architecture adopts sub carrier phase cancellation method to remove multiple peaks. By rearranging the correlation order and adopting time division technology, the proposed architecture reduces the hardware cost. Compared with the traditional structures, experimental results show that the number of adders is reduced by 75%.

Introduction

To provide more precise positioning and co-exist with BPSK signal, the binary offset carrier (BOC) modulation signal has been introduced to Galileo, modernized GPS and BeiDou system. The BOC-modulated signal has many advantages, including spectral separation and sharp autocorrelation function. However, the BOC-modulated signal has ambiguous problem in signal acquisition due to its multi-peak autocorrelation function.

Several unambiguous acquisition methods have been proposed. The BPSK-like method[1] considers the BOC signal as the sum of two BPSK signal and processes each side band separately. While single side band BPSK-like method [2] leads to 3dB degradation in SNR, and double side band BPSK-like method[3] need two sideband filters that increases the hardware cost. In [4], a novel method using recombination sub-correlations is proposed which keeps the sharp main-peak. However, the sharp main-peak increases the search space in acquisition. ASpeCT[5] method combines the incoming signal correlation with both replica BOC signal and pseudorandom noise (PRN) chips. While this method is only suitable for BOC(n,n)- modulated signal.

The Sub Carrier Phase Cancellation (SCPC) method[6] is developed from ASpeCT, which correlates the incoming signal with replica BOC signal modulated by in-phase and quad-phase subcarrier separately. The SCPC method maintains the wide autocorrelation function which reduces the acquisition search space.

In this paper, a novel hardware architecture is introduced based on SCPC method. The proposed architecture rearranges the correlation order and shares the previously correlation values to minimize the hardware cost and computation complexity in signal acquisition.

Background

(1) Signal Model

The BOC signal, donated as BOC(m,n), is generated by a square subcarrier modulation, where m, n are the ratio of subcarrier frequency(f_s) and pseudorandom noise (PRN) chip rate(f_c) to 1.023MHz respectively. The incoming pilot BOC(m,n) signal is :

$$R_r(n) = AC(nT-\tau)S_r(nT-\tau)\exp(j(2\pi f_r nT+\phi)+w(n) \quad (1)$$

$$S_r(nT) = sign(\sin(2\pi f_s nT)) \quad (2)$$

where $C(nT)$ is the PRN chip sequence, $S_r(nT)$ is the subcarrier, $w(n)$ is additive white Gaussian noise, and A, f_r, τ, ϕ, T are amplitude, signal frequency, time delay, carrier phase and sampling

period respectively.

The signal acquisition is a 2-dimensional signal search in the code dimension and the Doppler dimension. The combination of one code increment (δ_{chip}) and one Doppler increment (δ_{dop}) is defined as a "cell". To find coarse code phase and Doppler frequency, the receiver searches candidate cells until correlation value between the incoming signal and replica signal exceeds the threshold and passes validation. Because of multiple sharp peaks, the δ_{chip} is half of subcarrier chip typically. Increasing the code increment is one of the primary ways to decrease the number of search cells. In other words, we need to construct a wide correlation function.

(2) The SCPC Method

The SCPC method can provide a wide reconstructed unambiguous correlation function. Figure 1 illustrates the system model of SCPC method[6]. The receiver contains four channels and can be divided into two groups. In one group, the incoming signal is correlated with in-phase subcarrier modulated PRN code. In the other group, quad-phase subcarrier modulated PRN code is used. After integration and dump, the reconstructed correlation function is obtained by combining four correlation values.

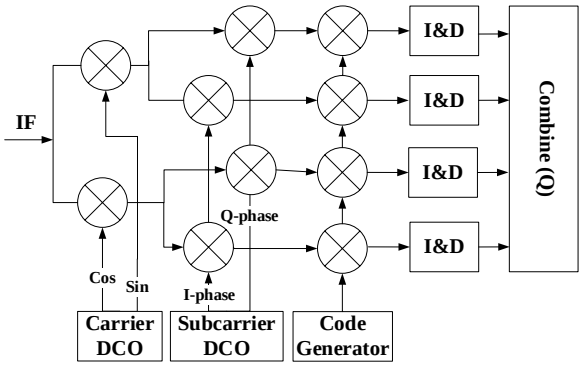

Figure 1: System model of sub carrier phase cancellation method

The four correlation values can be expressed as:

$$Y_{II} = \sum_{n=0}^{N} R_r(n) * S_{II}(n) \quad Y_{IQ} = \sum_{n=0}^{N} R_r(n) * S_{IQ}(n) \quad Y_{QI} = \sum_{n=0}^{N} R_r(n) * S_{QI}(n) \quad Y_{QQ} = \sum_{n=0}^{N} R_r(n) * S_{QQ}(n) \tag{3}$$

with

$$\begin{cases} S_{II}(n) = AC(nT)S_I(nT)\sin(2\pi(f_{IF} + f_d)nT) & S_{IQ}(n) = AC(nT)S_I(nT)\cos(2\pi(f_{IF} + f_d)nT) \\ S_{QI}(n) = AC(nT)S_Q(nT)\sin(2\pi(f_{IF} + f_d)nT) & S_{QQ}(n) = AC(nT)S_Q(nT)\sin(2\pi(f_{IF} + f_d)nT) \end{cases} \tag{4}$$

$$\begin{cases} S_I(nT) = sign(\sin(2\pi(f_s + f_d)nT)) \\ S_Q(nT) = sign(\cos(2\pi(f_s + f_d)nT)) \end{cases} \tag{5}$$

where N is the sampling number in coherent integration time, f_{IF}, f_d is the intermediate frequency, Doppler frequency of replica signal respectively.

The reconstructed correlation function (Q) is given by:

$$Q = Y_{II}^2 + Y_{IQ}^2 + Y_{QI}^2 + Y_{QQ}^2 \tag{6}$$

Proposed Scheme

In order to accelerate the acquisition process, parallel correlation channels are used. The direct implementation of SCPC method occupies large hardware resource that cannot achieve high parallelism. In this section, we propose an optimized hardware architecture.

In (3) ~ (5), most parts of computation are similar. For example, the different part of Y_{II} and Y_{QI} is only subcarrier sequence. Since the subcarrier is short-period sequence, the subcarrier correlation can be rearranged in the last and reuse the previous results. In that way, the PRN code correlation process can be merged into two channels, and save half of computation.

Secondly, to avoid signal distortion, the sampling frequency is at least twice of carrier frequency. For a certain δ_{chip}, there are more than two sample points. While subcarrier chip and code chip do not change in a δ_{chip}. If code chip correlates with every sample, the acquisition channel is inefficient.

To remove the redundancy, the correlation values in a certain δ_{chip} are accumulated, and then reused in all parallel channels.

Given all that, the equation (3) is rewritten as:

$$Y_{II}=\sum_{k=1}^{K}S_I(k)*M_I(k)\quad Y_{IQ}=\sum_{k=1}^{K}S_I(k)*M_Q(k)\quad Y_{QI}=\sum_{k=1}^{K}S_Q(k)*M_I(k)\quad Y_{QQ}=\sum_{k=1}^{K}S_Q(k)*M_Q(k) \tag{7}$$

with

$$\begin{cases} M_I(k)=\sum_{p=1}^{N/(KL)}\{AC[(Kp+k)T]T_I(p.k)\} & T_I(p,k)=\sum_{l=1}^{L}[R_r(t)*\sin(2\pi(f_{IF}+f_d)tT)] \\ M_Q(k)=\sum_{p=1}^{N/(KL)}\{AC[(Kp+k)T]T_Q(p.k)\} & T_Q(p,k)=\sum_{l=1}^{L}[R_r(t)*\cos(2\pi(f_{IF}+f_d)tT)] \end{cases} \quad t=L(Kp+k)+l \tag{8}$$

where K is the number of subcarrier chip in a PRN code, L is the sampling number in a certain δ_{chip}, and S_I, S_Q are the subcarrier sequence in a PRN code. Taking BOC(10,5) as example, K is 8, and S_I, S_Q are:

$$S_I=\{1,1,-1,-1,1,1,-1,-1\}\quad S_Q=\{1,-1,-1,1,1,-1,-1,1\} \tag{9}$$

The correlation process can be divided into three steps: integrating samples in a certain δ_{chip}; calculating the production of the integration values with PRN code chips; correlating with in-phase and quad-phase subcarrier respectively.

Since the integration in the first step isolates the code phase and subcarrier phase correlation, time division technology can be adopted to decrease hardware cost[7]. At the same CPU frequency, the hardware reuse ratio of proposed scheme to direct implementation is L (L >1).

Fig.2 depicts the hardware architecture of the proposed scheme. The incoming signal is correlated with replica carrier and integrated in a δ_{chip}. Then, the integrated values are correlated with PRN code. Based on the sample sequences, the correlation values are accumulated in corresponding register (Sum_I1...Sum_In, Sum_Q1... Sum_Qn). Then, the accumulated values are multiplied with in-phase and quad-phase subcarrier. Four correlation results are combined and compared with the acquisition threshold.

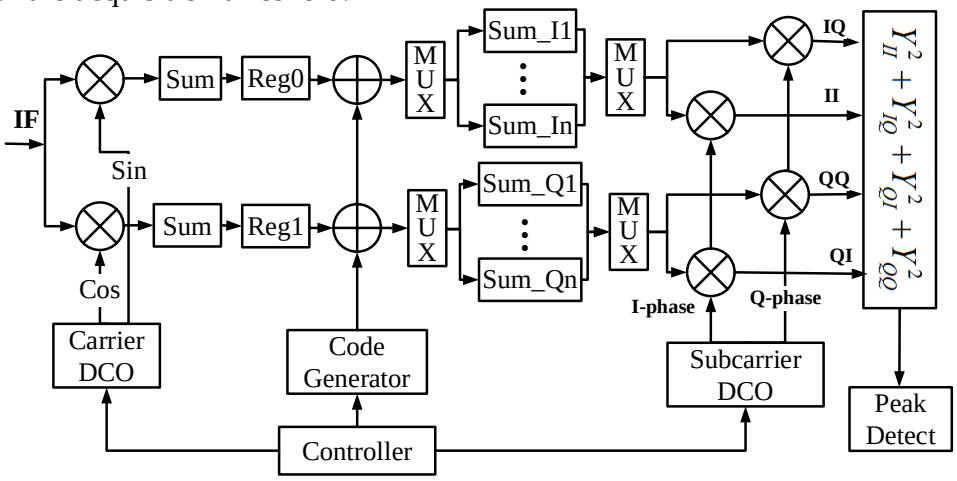

Figure 2: The proposed hardware architecture

Numerical results

The proposed architecture was implemented and compared with the direct implementation SCPC method[6] and double side band (DSB) BPSK-like method[1]. Those methods are tested for BOC(10,5)- modulated signal. The sample frequency is 81.84MHz, so L equals 4. Since most of the correlations are realized by sign inversions which require little resource, we use the number of adders as indicators of hardware usages.

The direct implementation SCPC method needs four hardware channels to realize single equivalent parallelism which is double of DSB BPSK-like method. By rearranging the correlation method and adopting time division multiplexing technology, the proposed method decrease the

hardware cost. Figure 3 summarizes the number of adders with different method. When the degree of equivalent parallelism is 400, the number of adders is reduced by 75% compared with direct SCPC, and by 50% compared with DSB-BPSK like method.

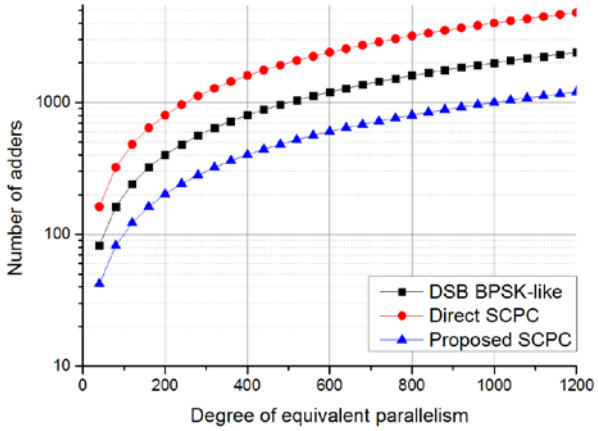

Figure 3: Number of adders for different methods with different equivalent parallelism

Conclusion

In this paper, a novel hardware architecture for BOC-modulated signal acquisition has been proposed. The proposed scheme adopts sub carrier phase cancellation method to remove the side peaks of autocorrelation function. By rearranging computation logic, the correlation process is divided into three steps. By using time division technology, the proposed scheme minimizes the hardware cost. Compared with direct implementation, the number of adders was reduced by 75% percent.

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