

Design of SPWM Generator IP Core Based on SOPC

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Abstract—A waveform circuit of SPWM based on SOPC is designed. In Quartus II 9.0 environment, Using Verilog HDL and module design method the design is completed. The selected FPGA model is EP2C35F672C6 in Cyclone series. According to the principle of sinusoidal PWM by irregular sampling, using the real-time overlapping of sine wave and triangular wave, the periodic adjustable SPWM wave is achieved. The results of simulation show that SPWM generator IP core could be embedded in special processor, and realize the driving of SPWM components.

Keywords—SOPC; FPGA; SPWM; sin wave; IP; simulation

I. INTRODUCTION

SOPC is a flexible and efficient on-chip system design's tools of Altera company [1]. It is essentially SOC (System on Chip) design technology, compared with other SOC design technology, it is characterized by programmability, i.e. the programmability of FPGA or CPLD devices is designed for SOC. The main ideas of SOPC is to provide an IP library, users can choose from the IP library components to assembly system [2]. With the improvement of the performance of SOPC and designers familiar with the system, the SOPC further expand the field of application. The ability to adapt to the complexity is improved, so that some complex digital circuits for high-level utility begin to tend to be designed based on SOPC methods [3].

II. PRINCIPLE OF SPWM WAVEFORM

SPWM (Sinusoidal PWM) control technology is a core technology in the field of research and application of the inverter. The inverter changes the equivalent output voltage by changing the output pulse duty ratios, so as to achieve the aim of changing from direct current(d.c.) to alternating current(a.c.). And the SPWM wave is widely used in motor's speed control and valve control.

SPWM is a widely used and more mature PWM method. According to an important conclusion of the theory of sampling control: when narrow pulse of equal impulse but different shapes bring to bear on a inertial link, its effect is basically the same. SPWM method is based on the theory of the conclusion, the PWM waveform which pulse width is changed according to the sine law and it's equivalent to sinusoid, namely the SPWM waveform, control the status of the switch device of inverter circuit, on or off, so that the area of the output pulse voltage equal to the area of the

output sine wave in the corresponding field. The frequency and amplitude of the inverter circuit's output voltage is adjustable by changing the frequency and amplitude of modulated wave [5].

The methods produced SPWM wave as follows, equal area method, hardware modulation method, software generating method, the natural sampling method, regular or irregular sampling method, and so on. Compared with the regular or irregular sampling, natural sampling is realized usually by analog circuit, the former is easy to use and advantageous for the digital control. When switching frequency is much higher than the grid frequency, the latter can achieve good control effect and replace the former [6]. The irregular sampling method is adopted here. The modulating wave is sine wave, an triangle wave is as the carrier wave for comparison, while the intersection of two waveforms, switch devices are on or off, this is right irregular sampling method. Its advantage is the SPWM waveform closest to sine wave. It is a kind of energy conversion form based the concept of equivalent area, its principle is very simple and intuitive, and has very precise mathematical basis, further its generality and operability is very strong [7].

Fig. 1 demonstrates the principle of SPWM pulse generation with a carrier's cycle T_c , V_{m} is the carrier's peak. At carrier's peak and valley point i.e. the time t_1 , t_2 , the sine wave is sampled respectively, and then, within a half carrier's cycle after each sampling, a trigger pulse is generated by comparing the sampling value with the carrier [6], namely SPWM wave.

In this paper, the digital method to realize irregular sampling has presented, the pulse width modulation is

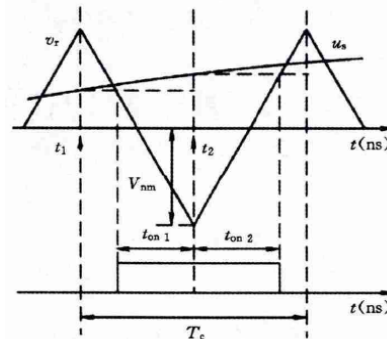


Figure. 1 SPWM pulse generation principle based irregular sampling

realized by using digitized way through comparing the triangle wave and sine wave in time, its principle as shown in fig. 2. By using digital method and look-up table method to generate triangle wave and sine wave respectively and input into the compare module. The method of comparison is to design the two digital modules. After comparing SPWM wave output generate.

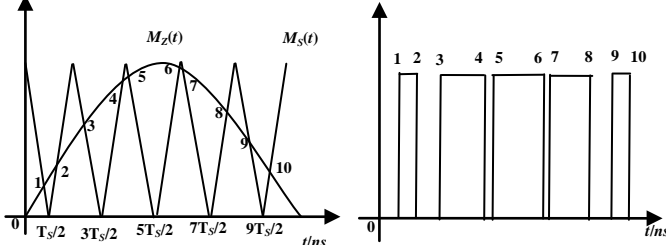


Figure. 2 The principle of SPWM pulse by digital method

III. THE DESIGN AND REALIZATION OF THE SPWM

A. Digitized triangle wave

The triangle wave generator was realized by the design up/down counter. Two 9 bits registers variables i.e. r and t

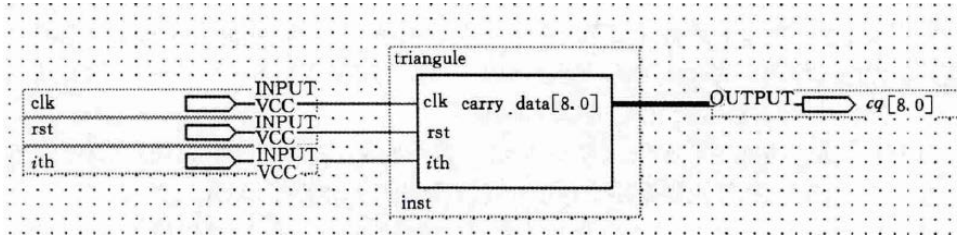


Figure. 3 The schematic diagram of the triangular

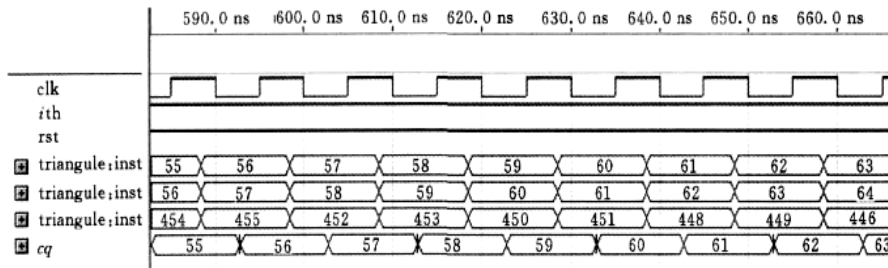


Figure. 4 The timing simulation of triangle wave in Quartus II 9. 0

B. Look-up table method for sine wave

The continuous sine wave has divided into uniformly distributed 1024 points, and these corresponding amplitude of the points stored in the ROM. The amplitude of the sine wave equals M_Z and the amplitude of triangle wave equals M_S , modulation coefficient $k = M_S/M_Z$. Because the amplitude of the sine wave must be less than the amplitude of the triangle wave, so modulation coefficient $k > 1$, if $k < 1$, the wave of pulse width modulation will appear saturation phenomenon, and enter into over modulated region [2].

, were defined, r increases from 0 to 511. Because r is defined as an unsigned number, when the next clock pulse CLK coming, r jumps to 0 and starts a new cycle. Similarly, t is also an unsigned register variables, it decrease from 511 to 0, when the next clock pulse CLK coming, t jumps into 511, circulate in turn. So it can be seen what the amplitude of triangle wave $M_S = 255$, cycle $T_S = 2 * 511 * T_{CLK}$, namely $T_S = 1024 * T_{CLK}$. The frequency of triangle wave can be expressed as $f = 1/T_S$, while M_S or/and T_{CLK} vary, the amplitude and frequency change to adjust the frequency of SPWM wave.

Program design was completed by using Verilog HDL. The principle of triangular wave generator shows in fig. 3. The simulation results in Quartus II 9. 0 as shown in fig. 4. The clk is the clock signal, ith is pause signal, rst is reset signal, the fifth is register variables t , the sixth is register variables r and the last cq is the data output of digitized triangle wave.

Take sine wave's amplitude $M_Z = 250$, cycle $T_Z = 1024 * 16 * T_{CLK}$. So the frequency of the sine wave can be expressed as: $f = 1/T_Z$. Here the values of triangle wave and sine wave which represent its amplitude are all positive. So in a two-dimensional coordinate system, triangle wave and sine wave locate in the y positive axis. The sine function is expressed as: $f(t) = M_Z \sin(\omega t + \theta)$. The sine wave is divided uniformly into 1024 points, and 1024 data are stored in the ROM corresponding address of 0-1023. While the data are taking, a 10 bits counter counts from 0 to 1023 repeatedly, and obtains the output data of the ROM from

corresponding address, so that you can get an approximate continuous sinusoidal wave. The principle of the sine wave generator in Quartus II 9.0 shows in Fig. 5, div as the clock divide module, counter as counter module, ROM as data

table for the sine wave. The simulation results of sine wave in the Quartus II 9.0 as shown in fig. 6. The clk is the clock signal, rst-n is reset signal, q is output signal.

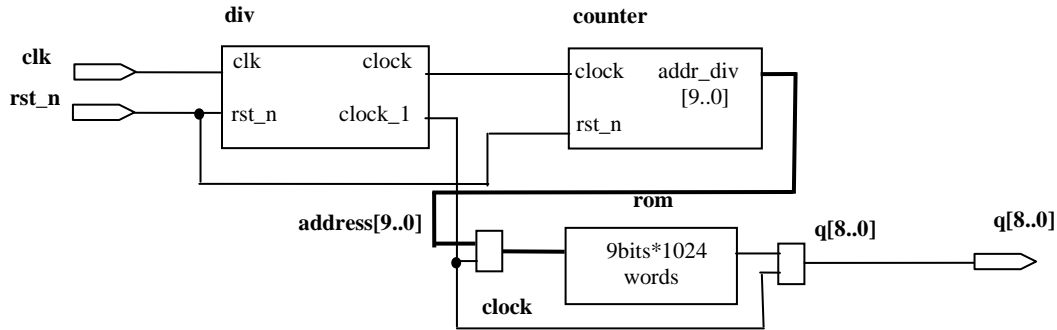


Figure. 5 The schematic diagram of single phase sinusoidal wave generator

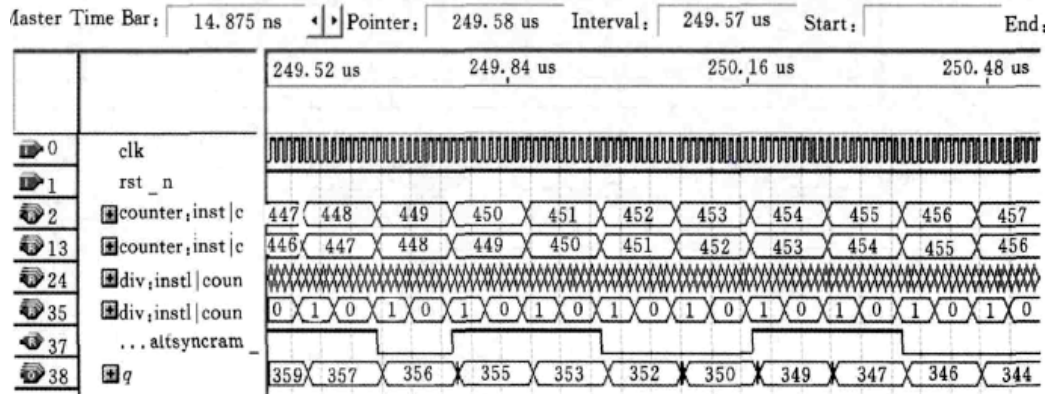


Fig. 6 The timing simulation of single-phase sinusoidal wave

C. The generation of SPWM wave signals

Get SPWM wave by using the method of comparison. Both produced digitized triangle wave and sine wave input into the comparator, namely me – compare. Whenever clock signal CLK arrives the comparator operates at once. As aforesaid, the triangle wave amplitude M_S and the amplitude of sine wave M_Z , if M_S Greater than or equal to

M_Z , then set agb=1, alb=0; On the contrary agb=0, alb=1; Then the results of the comparison transfer to the next comparator PWM-out, if agb=1 and alb=0, the PWM output is 1; If agb=1 and alb=0, then the PWM output is 1; Other cases, PWM output remains the same. The basic principle as shown in fig. 7 in the Quartus II 9.0. The compare and PWM-out perform comparison of triangle wave and sine wave and then output SPWM wave. It isn't calculate

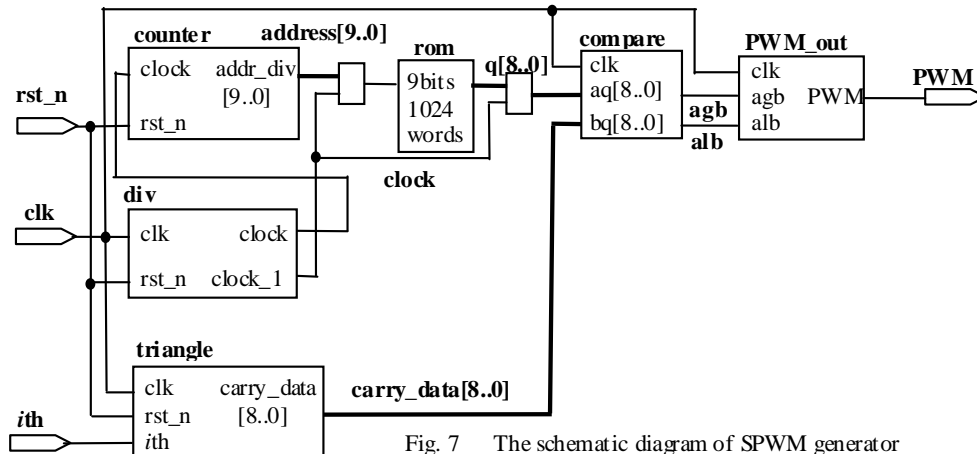


Fig. 7 The schematic diagram of SPWM generator

the transcendental equation about pulse width required for the traditional natural sampling[8], but compare the amplitude of triangle wave and sine wave at the same time to take SPWM output. The simulation results as shown in

fig. 8 using Quartus II 9.0. The clk defines as clock signal, rst-n as reset signal, PWM as output signals. A cycle's simulation shows that the results conform to the requirements.

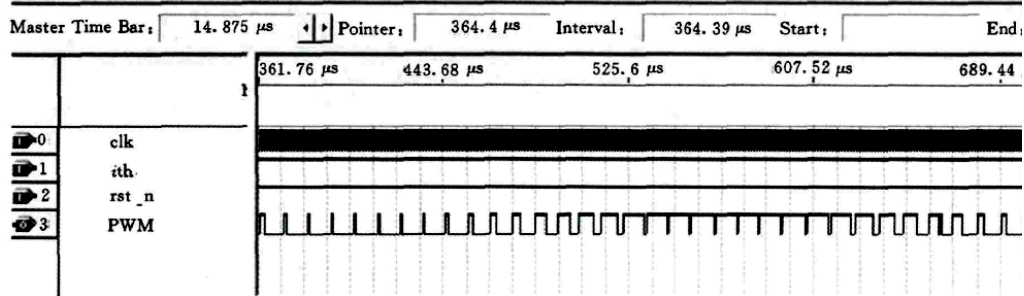


Fig. 8 The timing simulation of SPWM

IV. CONCLUSION

The paper elaborates the digitizing method to obtain SPWM by using irregular sampling. In Quartus II 9.0 environment the timing simulation results are verified and declare correctness and feasibility of the design. It avoids calculate the transcendental equation about pulse width required for the traditional natural sampling, saves the data processing device for traditional method needed, thus reduces the cost and improves the operation efficiency.

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