Improved Performance of Multilayer TiON/TaON Structure as Gate Dielectric for InGaAs Metal-Oxide-Semiconductor Capacitor

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Abstract. The interfacial and electrical properties of the multilayer TiON/TaON/InGaAs and TaON/TiON/InGaAs metal-oxide-semiconductor (MOS) capacitors fabricated by alternately RF-sputtering method are investigated and compared. Experimental results show that the former exhibits lower interface-state density, smaller gate leakage current, larger equivalent dielectric constant and higher device reliability than the latter. This is attributed to the fact that the ultrathin TaON interlayer formed on sulfur-passivated InGaAs can effectively reduce the density of defective states and unpin the Femi level at the TaON/InGaAs interface, thus greatly improving the interfacial and electrical properties of the device.

Introduction

InGaAs has been extensively investigated as alternative channel materials for next-generation nanoscale complementary metal-oxide-semiconductor (CMOS) device applications due to its intrinsic higher electron mobility than that of Si [1]. However, direct deposition of high-k dielectric on InGaAs yields poor electrical characteristics due to easy formation of native oxide on the InGaAs surface. So, the use of different interfacial passivation layer (IPL) prior to high-k deposition on InGaAs has been aggressively studied, achieving the improved interface quality and electrical properties of the device [2-4]. However, the device performance improvement comes at the expense of added processing time, scaling limitation, and complex IPL. To obtain a high-quality interface while negating an IPL, the multiple layers of alternate TaON and TiON are deposited on InGaAs by RF-suputtering Ti and Ta targets, and the interfacial and electrical properties of the prepared MOS capacitors with multilayer TiON/TaON or TaON/TiON as gate dielectric are investigated. As a result, excellent electrical properties are achieved with small gate leakage current, low interface-state density and high device reliability for the multilayer TiON/TaON/InGaAs MOS device.

Experimental

InGaAs MOS capacitors were fabricated on Si-doped n-$In_{0.53}Ga_{0.47}As/n^{+}$-InP substrate. The wafers were degreased using acetone, ethanol and isopropanol, and cleaned in diluted HF solution, followed by dipping in $(NH_4)_2S$ solution for sulfur passivation of the InGaAs surface and then dried by N_2. Subsequently, a high-k composite gate dielectric (~5 nm) composed of alternate TiN/TaN or TaN/TiN (~0.5 nm per layer) was deposited by RF-sputtering Ti or Ta target in Ar/N_2 ambient. A post-deposition annealing (PDA) was performed at 600℃ for 60 s in N_2 (500 sccm) + O_2 (50 sccm) to convert the TaN or TiN alternate layers into TaON or TiON to form two kinds of InGaAs MOS devices (denoted as TiON/TaON/InGaAs and TaON/TiON/InGaAs samples). Finally, Al was thermally evaporated and patterned as gate electrode and also as back electrode, followed by forming gas annealing at 300℃ for 20 minutes to reduce their contact resistance.

High-frequency (HF, 1-MHz) capacitance-voltage (C-V) and gate leakage current density vs. gate voltage (J_g-V_g) curves of the samples were measured using HP4284A precision LCR meter and HP4156A semiconductor parameter analyzer, respectively. All electrical tests were performed under a lighttight and electrically-shielded condition.

Results and discussion

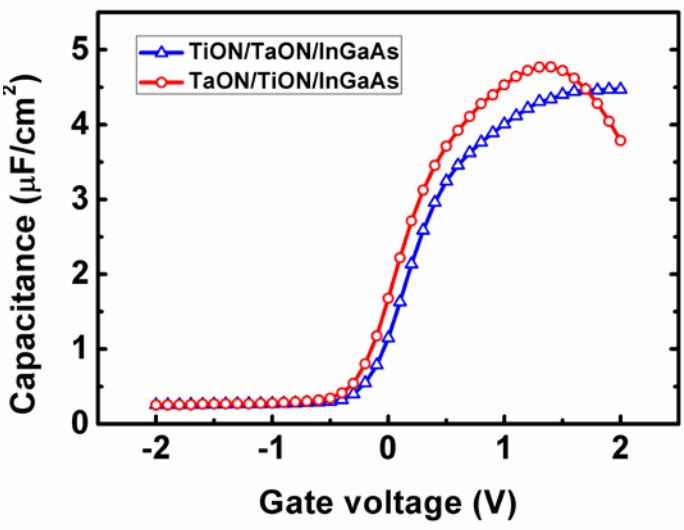

Fig. 1 HF (1-MHz) C-V curve for the TiON/TaON/InGaAs and TaON/TiON/InGaAs samples.

Fig.1 shows the typical HF (1-MHz) C-V curves of the two samples. It can obviously be seen that the accumulation capacitance drops for the TaON/TiON/InGaAs sample under high positive gate voltages due to the large leakage current, which probably comes from a high density of defective states at the TiON/InGaAs interface [5-6]. However, for the TiON/TaON/InGaAs sample, the accumulation capacitance exhibits a quasi-saturation as the positive gate voltage increases, which should be ascribed to the improved interfacial properties due to suppressed growth of low-*k* interfacial layer (In/Ga/As oxides) at the InGaAs surface by the ultrathin TaON IPL formed on InGaAs. The interface-state density (D_{it}) at midgap extracted from the 1-MHz *C-V* curve is ~1.0×10^{12} $cm^{-2}eV^{-1}$ for the TiON/TaON/InGaAs sample by using the Terman's method, which is lower than that for the TaON/TiON/InGaAs sample (~7.1×10^{12} $cm^{-2}eV^{-1}$). A smaller negative shift of the flatband voltage (V_{fb}) for the TiON/TaON/InGaAs sample (-0.32 V) than the TaON/TiON/InGaAs sample (-0.44 V) in Fig. 1 shows a reduced positive equivalent oxide-charge density (Q_{ox}) (4.9×10^{11} cm^{-2} *vs.* 4.0×10^{12} cm^{-2}) associated with the interface and near-interface traps. The equivalent *k* value of gate dielectric is calculated to be 19.8 and 19.6 for the TiON/TaON/InGaAs and TaON/TiON/InGaAs samples, respectively. A slightly larger equivalent *k* value is achieved for the former than the latter, due to suppressed oxygen diffusion from the high-k gate dielectric to the InGaAs surface by the TaON interlayer and thus less formation of the low-k interfacial oxide.

The gate leakage properties of the two samples are shown in Fig. 2. Large gate leakage current density is observed for the TaON/TiON/InGaAs sample. However, for the TiON/TaON/InGaAs sample, the leakage current density is greatly reduced. The smaller gate leakage current of the latter is closely related to its smaller Q_{ox} and D_{it}. In addition, a high-field stress at 3 MV/cm [= $(V_g - V_{fb})/T_{ox}$] for 3000 s is used to examine the reliability of the samples. The J_g-V_g properties are measured before and after the stressing, as shown in Fig. 3. On one hand, the increased gate leakage current after the stress for the two samples could come from carrier charging at the original traps of the oxide layer; and on the other hand, could come from the trap-assisted tunneling of electrons via newly-created interface and near-interface traps [7-8], as shown in Fig. 4. Obviously, the post-stressing increase of the leakage current is smaller for the TiON/TaON/InGaAs sample than the TaON/TiON/InGaAs

sample, which can be associated with less generation of interface and near-interface traps during the constant-voltage stressing due to reduction of the weak In-/Ga-/As-O bonds at/near the TaON/InGaAs interface.

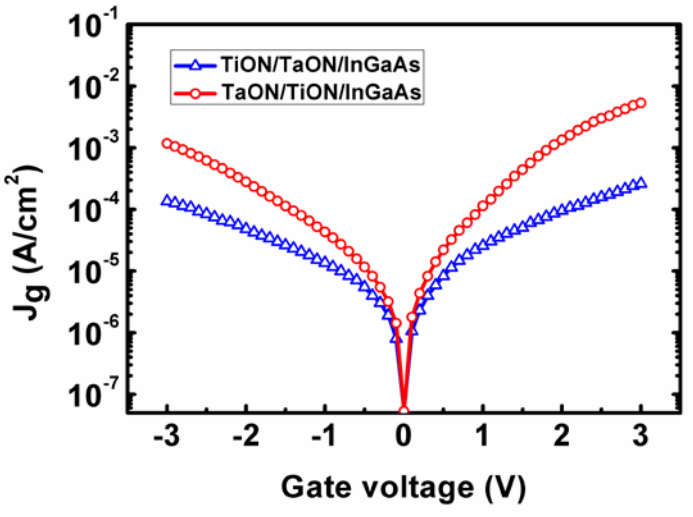

Fig. 2 Gate leakage current density (J_g) *vs.* gate voltage (V_g) for the two samples.

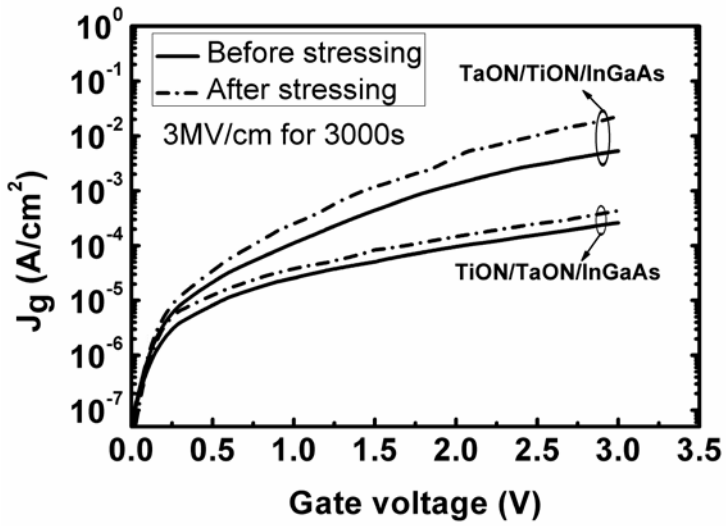

Fig. 3 Gate leakage current density (J_g) of the two samples before and after a high-field stress at 3 MV/cm for 3000 s.

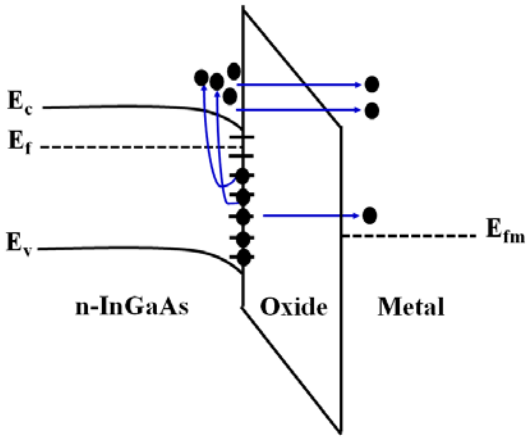

Fig. 4 the schematic diagram of interface-trap-assisted tunneling under positive gate voltage.

Summary

In summary, the interfacial and electrical properties of the InGaAs MOS devices with multilayer composite gate dielectric deposited by alternately RF-sputtering TaON/TiON or TiON/TaON have been investigated. It has been demonstrated that the multilayer TiON/TaON gate structure exhibits better performances than the multilayer TaON/TiON gate structure and good device reliability. All of these could be attributed to the fact that the ultrathin TaON instead of TiON interlayer formed on the InGaAs surface can effectively suppress the formation of the interfacial In/Ga/As oxides and remove excess As atoms, reducing the interfacial and near-interface traps and thus preventing the Fermi-level from pinning at the TaON/InGaAs interface.

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References

[1] J. A. del Alamo. Nature, Vol. 479 (2011), p. 317–323.

[2] I. Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and J. C. Lee. J. Vac. Sci. Technol. B, Vol. 25 (2007), p. 1491-1494.

[3] A. Molle, G. Brammertz, L. Lamagna, M. Fanciulli, M. Meuris, and S. Spiga. Appl. Phys. Lett., Vol. 95 (2009), p. 023507.

[4] H. C. Chin, X. K. Liu, X. Gong, and Y. C. Yeo. IEEE Trans. Electron Devices, Vol. 57 (2010), p. 973-979.

[5] L. S. Wang, J. P. Xu, S. Y. Zhu, Y. Huang, P. T. Lai. Appl. Phys. Lett., Vol. 103 (2013), p.092901.

[6] H. Zhao, J. Huang, Y. T. Chen, J. H. Yum, Y. Z. Wang, F. Zhou, F. Xue, and J. C. Lee. Appl. Phys. Lett., Vol. 95 (2009), p. 253501.

[7] F. Crupi, C. Ciofi, A. Germanò, G. Iannaccone, J. H. Stathis, S. Lombardo. Appl. Phys. Lett., Vol. 80 (2002), p. 4597-4599.

[8] W. Y. Loh, B. J. Cho, and M. F. Li. Appl. Phys. Lett., Vol. 81 (2002), p. 379-381.