Speed Control Scheme of Large-LED Display Screen

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***Abstract*—Take MCS-51 series as an example, introduced a high-speed control scheme of single- chip solutions for large LED screen display. The control of SCM for LED display screen generally start read data from data memory then write the data to LED dot matrix tablets. The innovation of this program are that use a pair of read instruction of external data memory to complete the read of the external data memory and the write of LED dot matrix tablets operations. This paper describes the design of high-speed control circuit solutions, briefly prompted software for points; Finally introduce the application of high-speed control scheme on LED large-screen display.**

Keywords-high-speed control; led display screen; large screen; MCS-51

I. INTRODUCTION

The basic working principle of LED display is dynamic scanning. Display control process start read font data from the data memory, then write the data through serial port or parallel port of SCM, finally scan it. Compared with static display program, dynamic scanning saves driving element, but requires refresh rate higher than 50 Hz to avoid display flickering images or text. Now the large screen LED display applications has become increasingly widespread. In order to achieve an orderly and rapid display control for hundreds, thousands of pieces of lattice LED tablets. a lot of people move their brains, and dual CPU, dual-RAM ,FPGA program have received successful applications; However, display control process of these programs read before write. The program propose a new thinking .It use a reading instruction to compete reading and writing in a single step. That can greatly improve the efficiency of the display control and simplified the circuit.

II. PRINCIPLE OF LED DISPLAY WORK

The basic working principle of LED display is dynamic scanning. Dynamic scanning is divided into and column scan, and row scan is frequently used. Line scanning method is divided into two 8-line scanning and scanning line 16.

By line scanning mode, each piece of LED lattice has a group of column driver circuit. The circuit must have a latch or a shift register for latching the contents of font data to be displayed. Under the line scanning mode, the same row LED lattice piece of the same name and line control pins are connected in a line. They are eight lines. That finally connected on a line drive circuit. Line driver circuit must also have a latch or a shift register for latching line scan signal.

The column driver circuit and line driver circuit of LED display generally use SCM to control, the common SCM is MCS-51 series. The displayed contents of LED dislay by fort is stored in MCU external data storage device and fort is an eight bit binary number.

SCM control process of LED display by reading before writing. According to the order LED tablets lattice on the screen, SCM first write read font data from the external data memory for the first section column driver latch of lattice LED in the first row, then the first 2, section 3 .....Until this row are finished after the last piece of font data, then SCM write scanning signal to this row line drive latch. So row 1, line 1 associated with the font data LED lights. Then 2nd row 1st row, 3rd row line 1 ..... lit until the last row of the first row. After the first line of each row is lit, keeping the delay period of time, and then become black screen, SCM have completely control a line scanning of LED display by this .

SCM control second row scan of LED display then control line 3until the line 8.The process is same to the first row, LED display also completed a full display image after all 8 lines are completed .

Although according to this way of working, LED display is lit line by line and only one line is lit every time, if each line can be lit more than 50 times per second which is higher than the refresh rate of 50 Hz, people see LED display is full-screen display of a stable image because of the human visual inertia.

III. TRADITIONAL CONTROL METHODS OF LED DISPLAY

The control circuits of LED display are summarized and compared in References [1] .Display control circuit work according to line-scanning. The column control circuit is divided into two categories. One use 74L S377 chip as latch column driver circuit, CPU write font data to latch column driver circuit through the parallel bus. Another use a shift register 74LS595 chip as a latch column driver circuit, CPU write font data to latch column driver circuit by the serial bus.

Neither parallel control bus nor serial bus control mode, the working process is give the data pointer DP TR assignment, and then accumulator A read font data from an external data memory RAM according to the data pointer DP TR point to .And when it is the parallel bus, give the data pointer DP TR assignment, then the CPU will write font data of the accumulator A to LED dot column driver chip latch circuit according to the data pointer DPTR point; serial when it is the serial bus, the CPU will write font data of the accumulator A to through the serial port latch column driver circuit.

Generally, MCS-51 is used frequently in the control of Display control. If Crystal frequency of the SCM system is 12 M Hz, the machine cycle is 1μs, all these two control

modes need a dozen μs to complete the display control a piece of lattice LED.

This paper proposed speed control scheme which need about 4μs to complete lattice LED display control chip. This calculation, an MCS-51 series can almost control more than 600 pieces display control of LED, Compared with the conventional control method, the efficiency of the display control is multiplied.

IV. HIGH-SPEED CONTROL SCHEME OF LARGE LED SCREEN

Schematic circuit diagram is shown in Fig.1,use The MCS-51 Series MCU to LED Display control, use RAM 62512 as a LED Display data memory, Store the type of data to display content, using 8 line scan mode, multichip LED Lattice slice sharing 1 group of line drive circuit; Each piece LED Lattice has a set of columns drive circuit, with 74lS377 as the column driver latch, The CPU through the parallel bus to columns power circuit of the latch letter data; Address decoding circuit used to generate the selected address of LED lattice line display driver circuit and column driver circuit.

This scheme has two characteristics: first, use the CPU control signal $\overline{RD}$ to latch Latches signals not signal $\overline{WR}$ .Although the CPU through parallel bus to column driver circuit latch letter data. The second, Address decoding circuit ensures the LED lattice column driver circuit of pills to choose address and data memory of a certain period of logical address overlap. Instead of regular use, address must separate the two groups.

Some of the simple change due to the circuit, MCU on the LED display screen display control efficiency obvious change will occur. The specific process is as follows: Assume that the data pointer DPTR is already loaded in the data memory address, An instruction to movx A,@DPTR, is The function of this instruction is CPU according to DPTR to read font data from external data memory, transfer to an accumulator A. But in this circuit, Because LED lattice column driver circuit of selected address and data storage of a certain period of logical addresses overlap, When executing instructions movx A,@DPTR, DPTR in addition to an address to the external data memory, also selected a LED lattice column driver circuit latch. If the selected the latches latch pin right into the pulse, The latch also would send the type of data from external data memory lock, this into the pulse with $\overline{RD}$. $\overline{RD}$ is the CPU when executing instructions movx A,@DPTR to the external data memory read control signals. Because of MCS-51 series single-chip microcomputer control signal $\overline{RD}$ read and write control signal $\overline{WR}$ of exactly the same sequence[2], There were no suspense that $\overline{RD}$ instead of $\overline{WR}$ function of latches. This instruction at execution time, at the completion of the data memory read at the same time, also completed for the LED lattice piece of writing, So speed up the process of the display control.

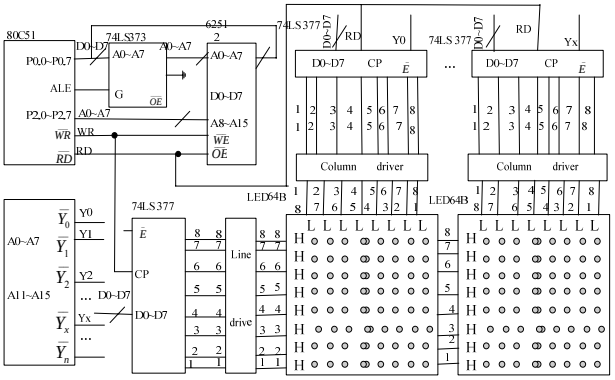

Figure 1. Schematic circuit diagram

This circuit in parallel bus CPU to 1 LED lattice column driver circuit of latch letter data application process as long as 4μs, Because now to 1 LED lattice column driver circuit of latch letter program as long as the two steps of data, First of all, give it an effective address data pointer DPTR, Then the CPU according to DPTR point to read font data from external data memory, At the same time also the font data passed LED lattice column driver circuit latch. 2 instruction, four machine cycle, 4μs. Special instructions, In the preparation of all ED lattice column driver circuit of latch letter data application, don't use cycle instructions , Because that each process have to add 2μs, Should adopt the method of programming LED lattice piece by piece , Made up of the program, although occupies a space, save the time. Methods with the design of space in time, Sometimes is also a method of design staff is surely worth a try.

This line drive latch circuit latches control, $\overline{WR}$ is written in the CPU control signal, Line drive latch piece also comes from address decoding circuit. With this set of address this part of the corresponding data memory storage space wouldn't have it.to avoid interference between data storage and LED dot matrix tablets.

Address decoding circuit design should guarantee the LED lattice column driver circuit of pills to choose address and data memory of a certain period of logical address overlap. Specific design examples below: Assume that a piece of LED screen with 240 LED lattice, It can display 60 characters by 16 x 16. For high-speed control in 1 piece of MCS-51 series single chip microcomputer. The 240 LED lattice column driver circuit of pills to choose address should be 240., Address decoding circuit must ensure that after the decoding of the effective address is greater than this amount. The address decoding circuit in figure 1, Enter the address of the signal is A0 ~ A7 and A11 ~ A15, There is no access to A8, A9, A10. With 74 l S138 decoder level 3 can get 256 valid address thread after decoding. The effective address thread 1 corresponding to 8 address of the external data memory, 0000 H, 0100 H, 0200 H, 0300 H, 0400 H, 0500 H, 0600 H, 0700 H. The effective address thread2 corresponding to 8 address of the external data memory, 0001H, 0101 H,

0201 H, 0301 H, 0401 H, 0501 H, 0601H, 0701 H. And so on, The effective address thread256 corresponding to 8 address of the external data memory, 00FFH, 01FF H, 02FF H, 03FF H, 04FF H, 05FF H, 06FFH, 07FFH. 240 of these effective address as the column driver circuit selected address, the rest of Line as drive circuit of the selected address, If not enough use, line driver circuit can consider instead the way of serial bus to control.

The results show that the above analysis. first, one piece of LED dot matrix piece of I/O interface address and data of 8 bytes of memory address overlap relationship is established. This is because every piece of LED lattice slice has eight lines, each line corresponds to one byte of data type. The second, All the LED dot matrix of I/O interface address and data storage of 0000 H ~ 07FF H address sets up the mapping relationship. In the data storage 0000-07FFH is a all the font data frames.

V. HIGH SPEED CONTROL SCHEME IN THE APPLICATION OF THE LED DISPLAY

Now on the business use hundreds, thousands, or even thousands of pills of LED lattice with large screen LED display. Single chip microcomputer control of LED screen, including MCU and PC communication, font data in the data processing and display control three parts.

In order to solve the problem of LED on a large screen display screen control, many documents to the design of control scheme for the success, Many solutions[3] [4] [5] [6]is the basic idea of data processing performed by a single chip microcomputer, display control by another piece of single machine Or a specially designed circuit is complete. The control efficiency of these schemes are high, but the circuit is more complex.

High speed control scheme especially suitable for bank exchange rate or interest rate screen using. LED lattice slice, for example, using the commonly used 6 cm x 6 cm outside profile size LED lattice for a little while, The screen area is less than 2 m^2, 1 piece of MCS-51 series single chip microcomputer can be completed.

VI. CONCLUSIONS

The basic idea of this scheme is MCU and PC communication, data processing and display control are performed by 1 piece of single chip microcomputer. Display control adopts high speed control scheme proposed in this paper, Circuit is simple, And display control efficiency is very high.

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