# Infrared Small Target Detecting Based on Parallel Streaming Pipeline Architecture

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**Abstract—The paper presents a design method for high-speed image processing system based on FPGA structure. A temporal/spatial fusion filtering algorithm is proposed for detecting infrared small target. The algorithm is composed of Top-hat filter, three frames difference filter (TFDF), or operation, closing operation and adaptive threshold. Pipeline is taken to improve the processing speed, which is determined by Top-hat filter that cost most processing time. Then parallel streaming pipeline architecture of Top-hat is proposed. Some Dual-port RAM and FIFO is taken to realize the parallel structure, which can realize real-time processing. Multi-Core Shared-Memory is proposed to tackle the problem of high speed parallel storage. The experiments show that infrared small target can be detected real-time.**

***Keywords-Infrared small target detecting; Pipeline architecture; FPGA; Temporal/spatial fusion filtering; Top-hat.***

## I. INTRODUCTION

The tracking and detection of small infrared targets has been a key technology in the field of satellite early warning, precise guidance, surveillance and detection. The detection of small moving target is one of the main focuses. However, because of lacking the shape, size and texture of the small target, it is hardly to distinguish the target in low SNR. As a result, the research of such problems becomes a challenging and meaningful task.

S.kim proposes a novel spatial filtering method to detect small targets in a cluttered background for infrared search and track. The filtering process of localised directional Laplacian-of-Caussion filtering, and the minimum selection can then remove false detections around cloud edges maintaining a small target detection capability. Experimental results validate the feasibility of the proposed method [1]. However he doesn't make use of the temporal charateristic information of small target. Wenjuan Dong introduces the design and engineering implementation of a portable IR target automatic detecting and tracking system. A project of real-time signal processor that is reconfigurable based on DSP+FPGA is proposed and implemented, which sends the images and detecting results to host computer by USB2.0 interface. However the project consumes too much resource, which will cost too much. And the area of PCB is large [2].

The paper presents a temporal/spatial fusion filtering algorithm detecting infrared small target that are easily realized in hardware, and then our infrared small target real-time detection system based on pipeline technology in low cost FPGA is introduced. Parallel streaming pipeline architecture of Top-hat and Multi-Core Shared-Memory are proposed. The experiment result was given as well; small target can be detected in real-time.

## II. INFRARED SMALL TARGET DETECTING SYSTEM BASED ON FPGA

### *A. Small target detecting algorithm*

A temporal/spatial fusion filtering algorithm is proposed for detecting infrared small target. The small target detecting algorithm consists of five sub-algorithms which can be named as top-hat, three frames difference, or processing, close, adaptive threshold segmentation.

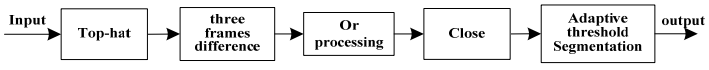



Fig.1. Detecting algorithm

The algorithm suppresses most of background and enhances targets by Top-hat filter [3, 4] in spatial domain, and suppresses high background profile and most of random noise by three frames difference filter [2] in temporal domain. There are only target and little noise in the image after temporal/spatial filtering. Then or operation is proposed to accumulate energy of sequence image. Target track can be detected after or operation. Morphological closing operation is applied to joint ruptured Target line resulted by three frames difference filter. At last adaptive threshold [5] is adopted for detecting target track.

Target and little random noise are left after temporal/spatial fusion filtering. Then a or processing algorithm is proposed. The algorithm can be described as follows:

$$f_{out} = \begin{cases} f_{in} & ,if \quad first\ frame \\ \max(f_{out}, f_{in}) & ,other \end{cases} \tag{1}$$

In above formula, $f_{in}$ is an input image, $f_{out}$ is an output image. As to random noise is irrelevant, and target is correlative between two coterminous images. Then target energy is accumulated, and target route and some random noise are left after or processing.

*B. The hardware for small target detecting system*

The all functions of small target detecting algorithm are realized in a single FPGA chip, and its peripheral circuit is extremely simple, showed in Figure 2.

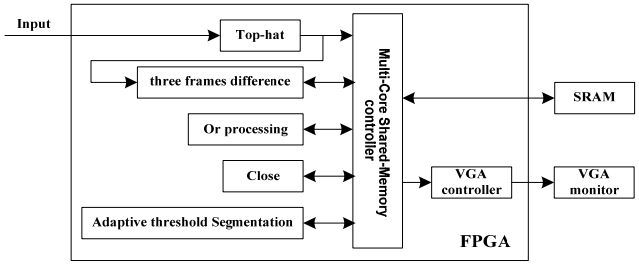



Fig.2. Overall systemic structures

The inner structure of FPGA is showed in Figure 2. All the five sub-algorithms are processing at the same time, and the data of the algorithms are read and stored at the same time. As traditional Top-hat will take most time of the five sub-algorithms, and it cannot be realized. Then parallel streaming pipeline architecture of Top-hat is proposed.

*C. Parallel streaming pipeline architecture of Top-hat*

The parallel streaming pipeline architecture of Top-hat is showed in Figure 3. The parallel streaming pipeline architecture of Top-hat can be realized bit by bit.

According to chain rule: if structuring element S is decomposed as

$$S = B_1 \oplus B_2 \oplus \ldots \oplus B_N \tag{2}$$

Then

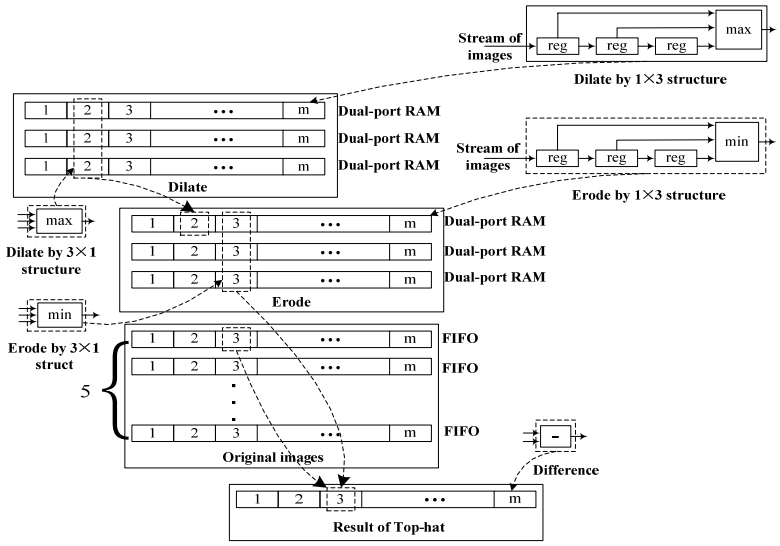



Fig.3. the parallel structure of Top-hat

$$A \oplus S = (\ldots(A \oplus B_1) \oplus B_2) \oplus \ldots) \oplus B_N) \tag{3}$$

$$A \Theta S = (\ldots(A \Theta B_1) \Theta B_2) \Theta \ldots) \Theta B_N) \tag{4}$$

Where $\oplus$ and $\Theta$ are dilation and erosion operations, respectively [6].

So, because of $\begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \end{bmatrix} \oplus \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$, for an m*n pixels image, the image can be dilated by 1×3 structure

firstly [7], and stored in an m bits dual-port RAM plugged in FPGA. Then the image will be dilated by 3×1 structure after first three rows image are dilated by 1×3 structure. The image will be eroded by 1×3 structure after first three bits image are dilated 1×3 structure. The image will be eroded by 3×1 structure after first three rows image are dilated 1×3 structure. All the data will be stored in six m bits dual-port RAM. Because the output of Erode will delay for 5*m bits compared with input image, then FIFO is taken to realize time-lapse function .At last difference is taken to realize Top-hat.

### *D. Multi-Core Shared-Memory*

As to the five sub-algorithms work at the same time, which results in eight data need to be read and stored at the same time. Then Multi-Core Shared-Memory is proposed, showed in Figure 4.

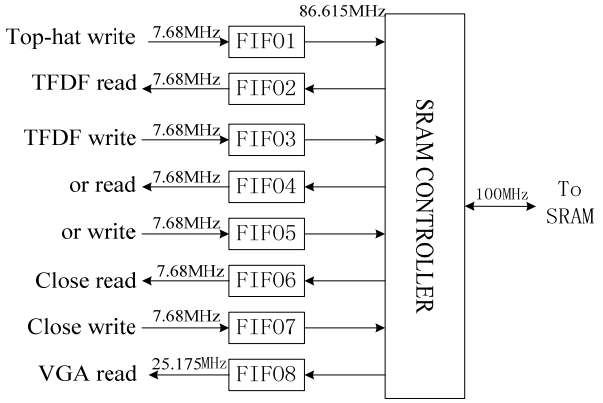



Fig.4. the structure of Multi-Core Shared-Memory

Eight FIFO are taken to store eight read/write signals from five sub-algorithms. SRAM controller is taken to determine which FIFO will be written /read to/from SRAM. For a 25 frame/s 640*480 pixels video stream, the frequency is 7.68MHz. And the frequency of VGA is 25.175MHz. Then the frequency of FIFO is 86.615MHz. As to read/write frequency of SRAM is 100MHz, which is higher than the frequency of FIFO. So Multi-Core Shared-Memory can realize reading and writing at the same time and real-time. The waveforms of Multi-Core Shared-Memory are showed in Figure 5.

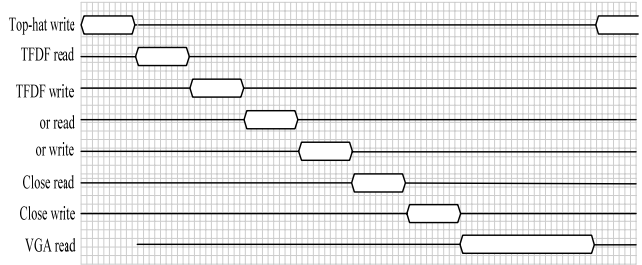
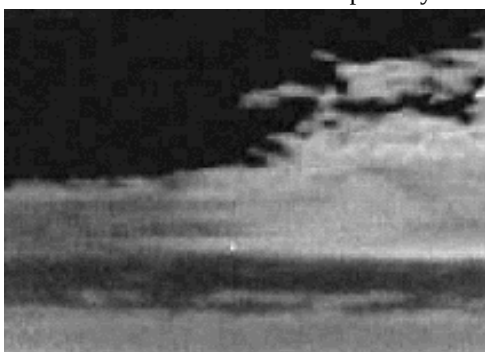



Fig.5. the waveforms of Multi-Core Shared-Memory

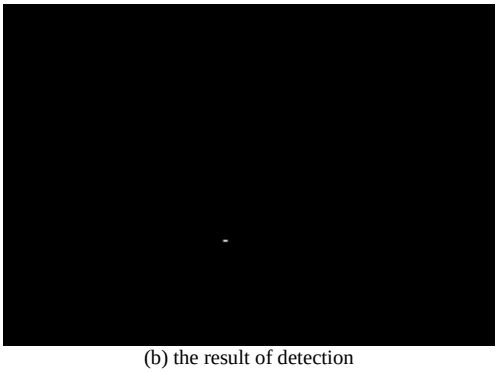
## III. THE PERFORMANCE TEST AND ANALYSIS

In order to verify the efficiency of the new method, five frames images are used to make the test. The technology parameters are: the size of small target is 2~7 pixels, and the SNR is low 1.4688. Here only gives two infrared images, one is first frame original image, and the result of detection is shown in Fig.6 (b).The result shows that small target is detected.

Data in four FIFO are written to SRAM, and data in other four FIFO are read from SRAM separately.



(a) First frame original image



(b) the result of detection

Fig.6. The result of infrared small target detection

## IV. CONCLUSION

This article designed parallel streaming pipeline architecture for Infrared small target detecting, which takes a temporal/spatial fusion filtering algorithm. The algorithm can realizes detect target in real-time. And parallel streaming pipeline architecture of Top-hat and Multi-Core Shared-Memory are proposed and realized.

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