Design of Microcomputer Monitoring System for Track Circuit

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Abstract—Microcomputer monitoring system for track circuit is used to monitor and record the operating state of the existing track circuit equipment. It also keeps a real time record of operating condition of equipment and provides accurate references for fault analysis. This paper introduces the design, debugging of hardware and software of communication board for monitoring and collecting, it also introduces the design, assembling and writing of communication protocol of circuit board and collecting group box, and system integration and test of collector and monitor upper computer. Finally this paper proposes a multi-channel monitoring of ARM-based collector, which has 16 channels for analog input and 48 channels switch signal collecting channel.

Keywords: Microcomputer monitoring system for track circuit; collector; communication board; CAN controller

I. INTRODUCTION

Computer monitoring system uses the latest modern sensors, computer network communications, field bus, databases and software engineering technology to monitor and record operating states of track circuit, which provides scientific references for electrical departments to master the historical states of the device, the current states and accident analysis. At the same time, the system also possess the characteristic of logic judgment, when the track circuit works abnormally or deviates from the predetermined limit, this system will give an alarm timely to avoid illegal operation or equipment malfunction to affect the safety and running of the train. Computer Monitoring System is an important railway modernization equipment, which is the basis of the signal equipment to achieve the state of repair and provides a convenient and accurate equipment maintenance tools for railway bureau.

By using of computer monitoring technology, the track circuit can be monitored and information of existing transmitters, receivers and relay states can be collected and judged logically, at the same time the state information and result of judgment also can be passed to the monitoring computer so as to achieve real-time monitoring and management of equipment, which facilitate the debugging and equipment maintenance and provide assistance to staff on duty if the track circuit fails.

Monitoring collector is the bridge to connect monitored high-temperature device and the PC. This paper presents a multi-channel selectable monitoring collector. Each monitoring collector can collect 16 analog and 48-way switch quantities. The user can distribute according to the specific requirements.

II. HARDWARE DESIGN OF MONITORING COLLECTOR

Monitoring collector mainly collects the state information of operating equipment and analyzes the collected data. Then it integrate the data according to the protocol format transmits the date to the upper computer. Monitoring collector is composed of two CPU board and communication board PCB.

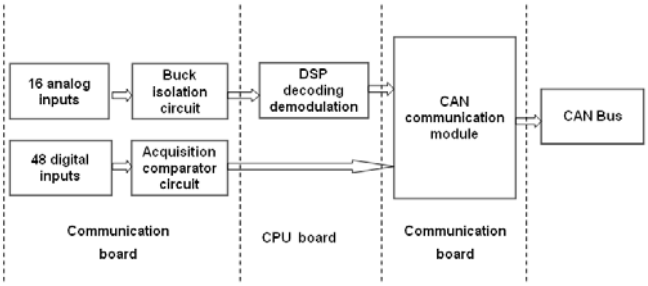

Figure 1 monitor acquisition hardware block

A. *Step-down isolation circuit*

Step-down isolation circuit uses transformer coupling or magnetic inductive coupling, and realizes effective isolation from master device. It collects information of ZPW-2000A transmitter output voltage, output current, limited input voltage of the receiver, and other analog quantities needed to be monitored. A single board can collect 16 analog quantities and identify analog amplitude and frequency.

B. *Sampling and comparing circuit*

Sampling and comparing circuit collects dynamically and timely information which are states of sending alarm relay (FBJ), the main rail relay (ZGJ), merged relay (BGJ), smoking alarm relay and power voltage.input monitoring acquisition, and the MAX973 voltage comparator compares the reference voltage settings, when more than equal to the reference when the voltage, the comparator output goes high, otherwise the output is low, in order to determine the relay state. Through the lower limit of detection of the relay voltage, the analog switch turned to maximize the expansion of monitoring acquisition acquisition capacity. A monitor collector can collect up to 48-way switch.

C. *DSP decoding and demodulating circuit*

DSP decoding and demodulating circuit processes the analog and identifies of its amplitude, the carrier frequency and the low frequency information and so on. It uses

WG-21A jointless track circuit which is mature digital circuits and usesTMS320VC33 DSP chip as CPU. Because it need demodulate 16 ways signal, 34K RAM in C33 is inadequate and a RAM chip (CY7C1021) as the storage of sampled data and two DACs (AD7865) chips are added. So 16 ways track signal can be sampled simultaneously, which use efficiently DSP processing function. In software, it uses WG-21A jointless track circuit receiver modules, including FFT,IFFT modules, low frequency and carrier frequency module, programmed external FLASH chip module and threshold inspecting module, etc. .

D. The CAN communication module

CAN communication circuit module uses embedded ARM chips LPC2119 and built-in 2-channel CAN controller which completes CAN controller initialization, CAN transceiver control and data communication between the upper computer and microprocessor. This design uses CAN1 controller which receives data from the upper computer for analysis by the CAN bus, and then passes them to control circuit in the lower computer to realize the control functions. when the CAN bus interface receives upload data from the lower computer, LPC2119 calls receiving interrupt program in CAN controller and filters and processes the data. If the data is matched, it will trigger transmitting interrupt processing program and reads the dual-port RAM data. Finally, it will assemble the data as message according to specific format and conventions of communication protocols ,then transmits timely them to upper computer

Because 16 analog voltage, carrier frequency, low frequency and 48-way switch states, are monitored in real-time, it is informative. This design uses multi-frame mode to transmit data, which is using 8 data frame with an ID address. The design assembles as large data packets by the processing of date domain number and continuous transmission, so that the amount of information expanded unlimitedly.

E. CAN bus

CAN-bus is a multi-master mode serial communication bus. The basic design specification of CAN bus requires a high bit rate, high resistance to electromagnetic interference, and can detect any errors that are generated. When the signal transmission distance exceeds 10Km, CAN-bus still can provide data transfer rates of up to 5Kbps. so it is good communication control method that possess an advanced technology, high reliability, perfect function, reasonable cost. CAN-bus has been widely applied to various automation and control systems. It has incomparable superiority and is applied in from high-speed networks to low cost multiplex wiring.

III. HARDWARE DESIGN OF MONITORING AND COLLECTING COMMUNICATION BOARD

A LPC2119

The Philips LPC2119 chip is applied in this design. LPC2119/2129 is based on a 16/32 bit ARM7TDMI-STM CPU which has real-time simulating and tracking function and a 128/256k bytes (kB) embedded high-speed Flash memory. 32-bit code width 128-bit memory interface and unique accelerator architecture can run at maximum clock rate. Because of strictly control of the application code size, 16-bit Thumb mode reduces code size of more than 30% while the performance loss is small.

Since the LPC2119/2129 posses a very small 64-pin package, low power consumption, more than 32 timers, four 10-bit ADC, 2-way CAN, PWM channel, 46 GPIO and up to nine external interrupt, these make them particularly suitable for automotive, industrial control applications, medical systems and fault-tolerant maintenance buses. With a wide range of serial communications interfaces, they are also well suited for communication gateways, protocol converters, and other types of applications.

B The ARM7TDMI-S processor

ARM7TDMI-S is a general 32-bit microprocessor, which offers high performance and low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles. Instruction sets and related decode mechanism is simpler than the complex instruction sets. Thus the use of a small, inexpensive processor core can achieve a high instruction throughput and real-time interrupt response. By using of pipeline technology, all parts of the processing and storage systems can operate continuously. Usually, in the process of the execution of an instruction, the next instruction is decoded, and a third instruction is fetched from memory.

Instruction length of THUMB instruction sets is 16 bits which achieve twice the density of standard ARM code and maintain the advantage on most performance ARM. 16 processors don't have these advantages, because THUMB code and operation is the same as ARM's and THUMB code is 65% ARM code size, but its performance is equivalent to 160% as the same ARM processor memory system performance with 16 bits processor.

C The power supply circuit design

In view of the project, the design uses a 24V DC external power supply voltage. LPC2119 uses two sets of power supply in which I / O port power supply is 3.3V, core and on-chip peripheral power supply is 1.8V.In the process of circuit, it must be considered that the 25V voltage is changed into 5V voltage, 3.3V voltage and 1.8V voltage which communication board needs.

As an application of the industrial embedded system products, the stability of the power system has a crucial impact on the system. Power filtering and protection circuits are added in order to improve power quality and system power supply circuit security system. The design uses a power module DC24D5-12W by which 24V DC power supply is introduced. A diode V50 prevents reverse power. 24V is changed into 5V by C9 and C11 and then through the

low dropout power chip LM1117MPX-3.3 and LM1117MPX-1.8 , regulated output voltages of 3.3V and 1.8V. The power supply circuit shown in Figure 2

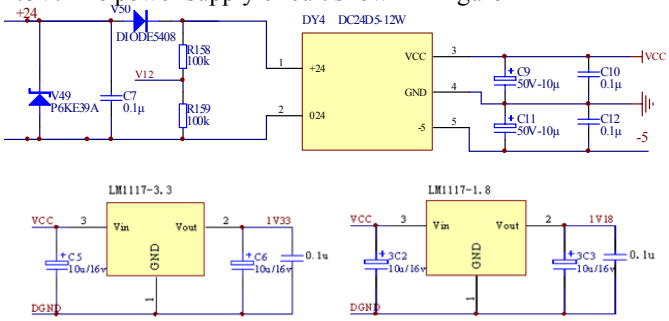

Figure 2 The Power circuit

Output current in LM1117 series chip is up to 800mA. Accuracy of the output voltage is ± 1%.The chip has a current limit and thermal protection function, which is available in a number of high efficiency and low-power small footprint designs. It has a very low quiescent current, low dropout voltage at full load it is only 1.1V, when the output current is reduced, the quiescent current is changed with the load. When used, its output requires at least one 10uF capacitor to improve the transient response and stability.

D The design of reset circuit

Because ARM chip has high-speed, low-power and low operating voltage, higher requirement in low noise tolerance limit, power supply ripple, transient response performance, stability of the clock source and reliability of power monitoring is put forward. The reset circuit in this design uses a dedicated microprocessor power monitoring chip MAX708SD in order to improve system reliability. Because during JTAG debugging, nRST and TRST is controlled by the JTAG emulator, a tri-state buffer gate 74HC125is used to drive, reset circuit shown in Figure 3

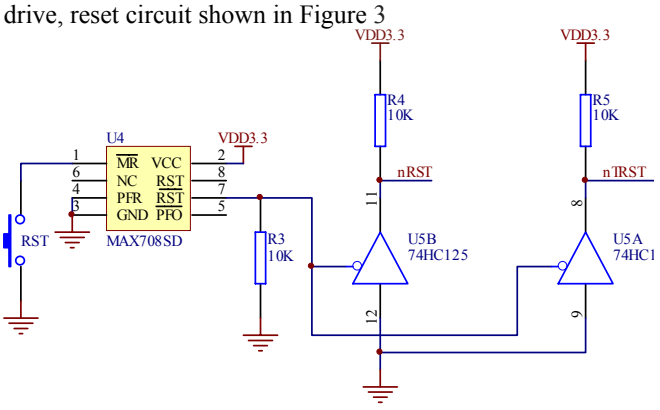

Figure 3 The Reset circuit

In Figure 3, the signal nRST is connected to the reset pin nRST and the signal nTRST connected to the LPC2119 chip JTAG interface circuit reset pin TRST. When RST reset button is pressed, MAX708SD immediately reset signal is output. The pin RST outputs low voltage leading to74HC125C and 74HC125D conduction and the signal nRST, and nTRST output low voltage to reset the system. Usually when RST in MAX708D outputs high level, 74HC125C and 74HC125D will end. By the pull-up resistor R4 and R5 signal nRST and nTRST is pulled high level, system will operate normally or JTAG emulation debug.

E The system clock circuit design

The clock circuit provide the system work clock. LPC2119 can choose internal clock circuit, the external clock circuit and real-time clock circuit as a PLL clock source. By default, the system uses an internal clock source until the software changes system settings. This design uses an external crystal oscillator as a clock source, the internal PLL circuit can adjust the system clock, which results in the system to run faster (CPU maximum operating clock is 60MHz). If the on-chip PLL function and ISP download function cannot be used, the external crystal frequency range from 1MHz to 30MHz and the external clock frequency range from 1MHz to 50MHz. If the on-chip PLL function or ISP download function are used, the external crystal frequency range from 10MHz to 25MHz and the external clock frequency range from 10MHz to 25MHz.

In the design, an external 11.0592MHz crystal is used, the circuit as shown below. 1M resistor R6 is merged to both ends of the crystal, which make the system easier to vibration. The communication baud rate is more accurately because of using of 11.0592MHz crystal, at the same time it supports the PLL function and ISP function of LPC2119 chip.

F The interface circuit of CAN

Built-in 2-channel CAN controller in LPC2119 independently complete the initialization, CAN transceiver control and data communication between the host computer and the microprocessor. This design uses the CAN1 controller, the main function of this circuit is to receive data from the host computer for analysis of recombinant via CAN bus, and then passed to the lower computer control circuit to realize control functions. When the CAN bus interface receives upload data from lower computer. LPC2119 call CAN controller interrupt program to filter and process the received data. When condition is matched , triggering transmit interrupt handler program reads the data fro, dual-port RAM, then the data is combined into a packet according to a specific format and communication protocol. Finally, the data is putdown to the host computer.

IV. SOFTWARE DESIGN OF MONITORING COLLECTOR COMMUNICATION BOARD

A The software design of communication board

CAN bus node should finish the communication task effectively and real-timely. The communication software includes three parts that are CAN initialization procedure, sending packets subprogram and CAN bus error handling routines and procedures. After completion of the initial

setting, CAN controller enters the operating mode and then it can transmit and receive data normally.

B The CAN controller driver

In order to quickly take advantage of the embedded ARM7 microprocessor LPC2119 to design CAN communication, the standardized CAN controller driver is modified on the basis of the original source code to meet this design needs.

C The structure of CAN controller driver

For microprocessor, CAN controller is entirely based on event-triggered, that is when the CAN controller will change in their own state, the results will tell the microprocessor. If microprocessor processes CAN controller, interrupt mode can be used and handle the CAN controller by check the CAN controller states

V. SUMMARY

After verification of more three years, track circuit microcomputer monitoring system can meet the needs of the plant for production use and accommodate existing WG-21A jointless track circuit maintenance and monitoring requirements. Because the system is based on proven technology and design thinking, with the continuous improvement on functions and user demand, the system needs to continue to improve in order to meet the requirements of the device and improve maintenance level. The monitoring system should be connected by the plant LAN system so that more departments can check the device states real-timely. This facilitates technology systems, production systems to grasp the situation and provide better technical services and reasonable production scheduling management. This will be the further problems to solve and future research directions.

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