The Analysis Research of Proximity Effect Correlation Algorithm for Accurate RF System

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Keywords: RF system, correlation algorithm, proximity effect

Abstract. In this paper, we propose a novel research of proximity effect correlation algorithm for accurate RF system. In summary, we have demonstrated an efficient approach for broadband modeling of millimeter-wave CMOS FETs by using a set of pre-measured and pre-modeled cells with varied gate width. This approach allows a scalable and flexible modeling process, and simplifies the modeling procedures. The method has been verified with experimental results measured from 65-nm RF CMOS devices, where the modeled data match well with the measured data in a wide frequency range up to 40 GHz and across a wide range of gate width. The experimental shows the feasibility of our method.

Introduction

The significant improvement in the advanced CMOS process has raised much interest in Si based millimeter-wave integrated circuit design during recent years [1-5]. It has also led to the development integration Œ power amplifier. In addition to the challenges of the circuit design, a general model for the mm wave device model still cannot be applied in many cases. Factory production equipment model of product development kit (since) target usually low gigahertz applications and do not take the mm - wave complex caused by high frequency effect and parasitic effect transistor, usually adopt complex dobby with large area layout. So in many cases, the designer must build their own model before designing a mm - wave integrated circuits [6-8]. Most previous reports concentrated in a fixed mode, are usually based on Berkeley short channel IGFET model (BSIM) parasitic sub - circuit. It requires a lot of modelling work such a fixed model extended to a scalable. Due to a lack of proper extensible model, for example, designers usually design circuit equipment, have been extracted from such a fixed model [9-11]. Limited by the available choice on device size, the MOSFETs used in each stage of a multi-stage amplifier are chosen to be the same in many reported circuits and this is not necessarily the optimal design choice. Retractable modelling challenges mm - wave field effect transistor mainly from local the parasitic capacitance and resistance of the wire connection through and contact a row of fingers, and the loss of the substrate. These parasitic effects is highly dependent on the layout and show the key influence equipment advanced performance is even higher than the inherent parasitic capacitance of the node capacitance. Therefore, accurate modelling of the parasitic effect is crucial. In general, a scalable model relies on a set of empirical equation will be two internal geometry dependent and parasitic effects.

These extensions equation is limited to insert a geometrical set the maximum and minimum of the scope of the measuring equipment. Need to make a lot of equipment, measurement and calibration to extract the empirical equation in order to achieve acceptable accuracy. As a result, it is rather difficult and time consuming to build such a set of equations covering both the intrinsic and parasitic effects over a wide geometry range. In this work, we took a further step by leveraging these modelling methods and developed a highly efficient approach for modelling of broadband mm-wave multi-finger MOSFETs with gate width scalability by using a set of pre-modelled cells.

System Layout and Material

In the proposed modeling approach of mm-wave multi-finger FETs, the device gate width is scalable while gate length is the minimum allowed size for high speed operation. Firstly, a group of devices with varied gate width are fabricated, measured and modeled. The layout of these devices are more arms, they are known as the pre - modeled the work cell. Then with the required equipment door width can be composed of several smaller equipment selection and the pre-modeled group of cells and the figure 1 shows this.

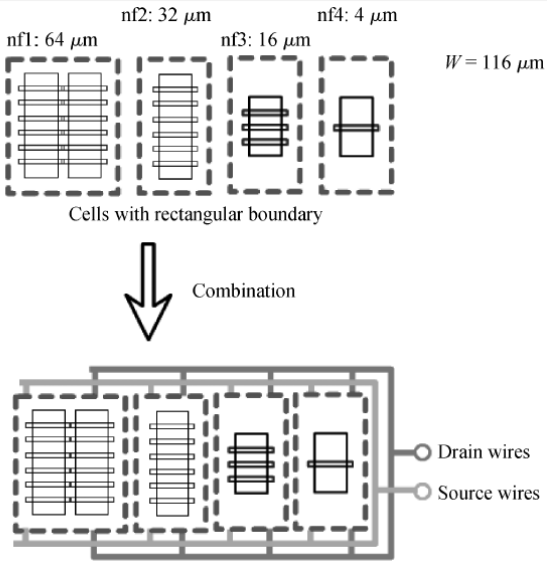

Figure 1: The Illustration of the layout approach using pre-modeled cells and the conventional layout approach

It is the main advantage of traditional layout extends all cell boundaries within the layout remains the same, then the corresponding performance and parasitic effects. And traditional scalable mode is difficult to capture the complex geometry dependent on equipment performance and the parasitic effect within the cell boundary, the method USES a highly accurate fixed model to describe the fixed cells and as a black box model scalable unit building blocks of the model. Don't know any geometry dependent cells don't hinder the method to generate a useful scalable ability of the model. This approach doesn't require extensive empirical equation development and needs much fewer devices to be fabricated, allowing for highly efficient modeling of mm-wave MOSFETs with gate width scalability. The figure 2 shows the feature.

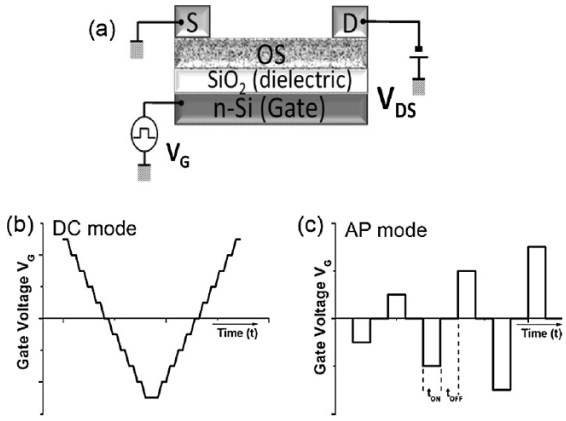

Figure 2: The Schematic Illustration of the BGTC OFET Device

The Modelling Procedure

Based on the proposed layout approach, a corresponding scalable modeling strategy is developed. As shown in Fig. 3(a), the parasitic effects of connection wires need to be described by a scalable model since the length of the wires that connect the cell terminals changes with different cell

combinations. But the cells only need to be described with fixed models because their layouts stay unchanged. Then according to the detailed layout and the parasitic effects of wires shown in Fig. 3(a), the fixed cell models and the scalable wire model are integrated to be a complete model as in Fig. 3(b) to model the final target device. Only the model of cell nf1 is shown in detail, other cells use the same model with their corresponding model parameters. The fixed model for cell devices in this work is plotted again in Fig. 3(c) for clarity. This cell model is based on models developed in Refs The simplicity and consistency in layout leads to reduced modeling efforts. The coupling effects between the connection wire and the cells are minimized by avoiding wires passing over cells. In this way, the cells and connection wires can be separately modeled without causing much inaccuracy.

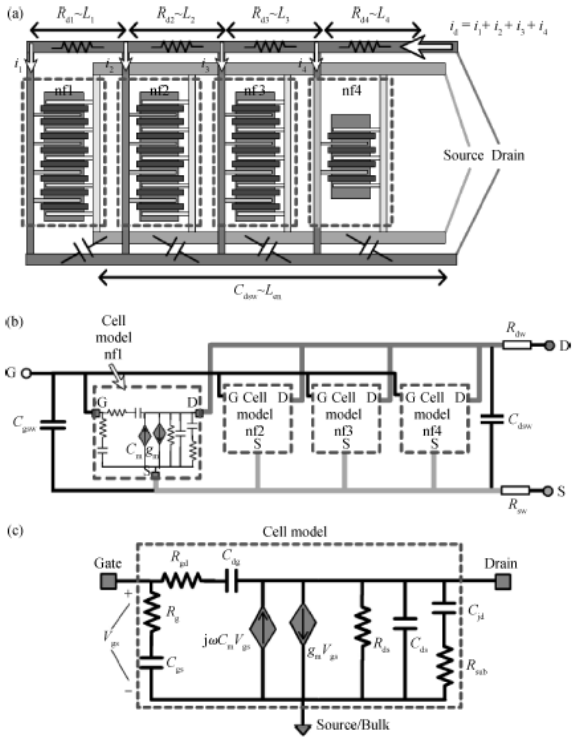

Figure.3: The (a) Schematic illustration of detailed layout for the parasitic capacitance and resistance modeling. The currents, parasitic resistance and capacitance in connection wires are overlaid in the layout.

(b) The scalable model constructed according to the layout in (a) by combining parasitic model of wires and fixed model of each cell. Only the model of cell nf1 is shown, other cells use the same model with different model parameters.

(c) The small-signal equivalent model of cells used in (b) is plotted in detail.

AP pulse mode sweeps the gate voltage from negative to positive values (or vice versa), thus allowing the charges trapped by the negative pulse to be immediately detrapped by the positive one. In this way, an intrinsic transistor response with negligible charge-trapping effect can be measured. Compared to all the above listed approaches of reducing hysteresis, the pulse mode can be applied to all types of FETs regardless of the configuration and materials involved in the fabrication. We find that by varying the pulse-on and pulse-off time of the applied gate voltage, the current's forward and reverse curves coincide and lead to a single value of mobility. We adopt the same approach to evaluate the transistor's stability under operation by recording the drain current (IDS) as a function of time, applying continuous and pulsed gate voltages. Furthermore, a comparison of the sensing performance of the OFET upon exposure to analyte-vapours when it is operated in time under continuous and pulsed mode is also presented.

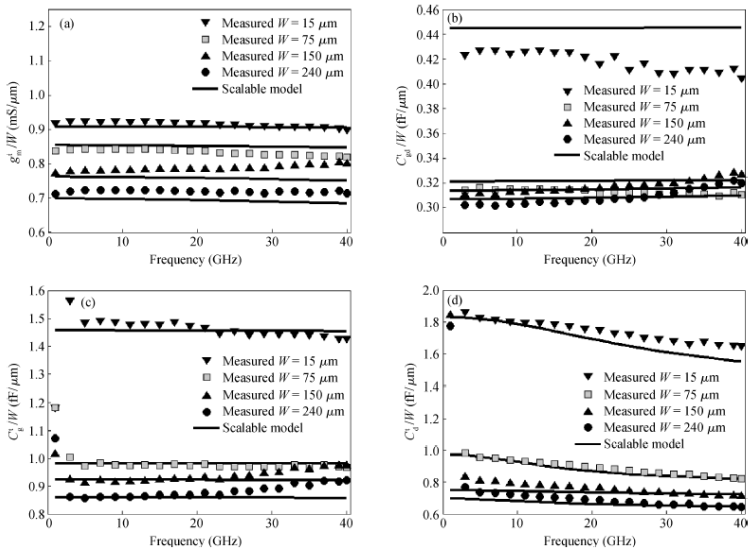

Figure 4: The measured (markers) and model simulated (solid line) frequency

The Simulation Procedure

Continuous Gate Voltages. Standard DC I–V measurement of a P3HT based OFET transfer characteristic curve is reported in Fig. 5. As it can be seen, the transistor exhibits hysteretic behavior. Hysteresis appears as a mismatch between the forward (from OFF to ON state) and reverse (from ON to OFF state) current curves under the respective voltage sweeps. The reverse sweep current curve is lower than the forward sweep curve and there is a negative shift of the threshold voltage. Furthermore, by reducing the sweep rate, a slight increase in the hysteresis width is observed, along with a decrease in the maximum on-current. In this case, when sweeping the voltage from the ON to the OFF state the amount of mobile charges in the channel is less than in the forward sweep. It seems that part of the mobile charges at the interface have become immobile. According to the field-effect transduction principle, charges are accumulated in the semiconductor/dielectric interface by application of the gate voltage. Both free and trapped charges are present in the channel, but only the free charges and those occupying shallow traps can contribute to the transport. Charges occupying deeper traps are actually immobile, or they do move but with extremely low mobility. Furthermore, the hysteresis loop between forward and reverse sweeps depends on the distribution of traps, the energy of trap states, and the rate at which carriers can escape from the traps.

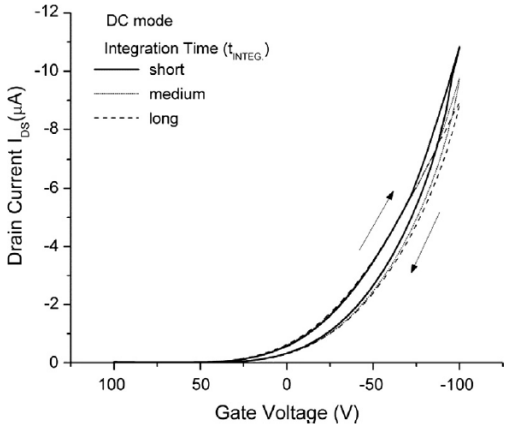

Figure 5: The characteristic curves

Pulsed Gate Voltages. It has been more recently showed also by Lin and Tiwari that by pulsing the gate voltage, the hysteresis width can be minimized. The pulsed measurement methodology relies on the fact that the gate voltage is applied for a short time, leaving less time available for charge traps to be filled. Recovery is usually a slower process and, therefore, requires more time. Under no bias, the trapped charges have enough time to relax, thus detrapping is achieved. However,

gate voltage pulses of the same polarity can still cause accumulation of trapped charges [11]. In a normal DC sweep measurement, the charges remain trapped until the gate bias is reversed. A common method to partially detrap charges is by gating the device from positive voltage values, instead of zero for p-type materials [6], and from negative values for n-type. In this way, the OFF current is often reduced but hysteresis appearance is difficult to be avoided. Moreover, the illumination of the transistor at certain wavelengths has been addressed as a recovery method, but this technique requires complicated instrumentation set-up [2]. Instead, pulsed measurements can be carried out by sweeping the gate voltage in a symmetric way, from negative to positive values or vice versa. In this way, by applying for example an exact opposite VG pulse after each negative VG pulse, the trapped charges can be immediately detrapped by the positive voltage. Fig. 6 shows a transfer characteristic curve by applying gate pulsed voltages of alternating polarity. Eventually, hysteresis is effectively suppressed, leading to a hysteresis-free transfer characteristic curve of the OFET device. Depending on the pulse duration and pulse-off time, reverse and forward current curves can appear as a single line. To further investigate the hysteresis dependence in pulsed measurements, a set of AP pulse sweeps for different tON and tOFF were conducted.

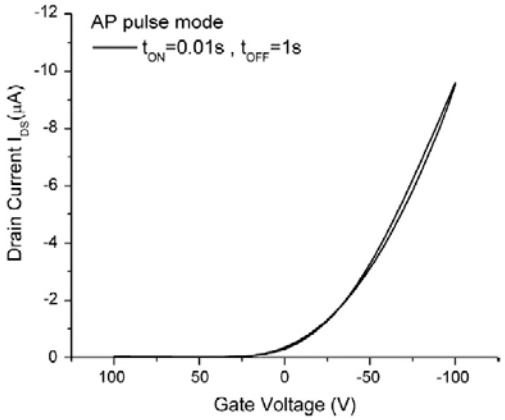

Figure 6: The characteristic curve

The Summary and Conclusion

In summary, we have demonstrated an efficient approach for broadband modeling of millimeter-wave CMOS FETs by using a set of pre-measured and pre-modeled cells with varied gate width. This approach allows a scalable and flexible modeling process, and simplifies the modeling procedures. The method has been verified with experimental results measured from 65-nm RF CMOS devices, where the modeled data match well with the measured data in a wide frequency range up to 40 GHz and across a wide range of gate width. This method enables the circuit designers to choose the optimal device size according to specific design target instead of being limited by several fixed devices.

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