

Design of a Missile Test Simulation and Training System

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Abstract. In this paper, a missile test simulation and training system based on CPLD is designed to implement the test and other training mission of a missile. The implement project is given; the hardware structure and software of the system are introduced. The research of this system has greatly developed the universality and extensive of the test system, and realized the intelligent automatic test of the control system of missile.

Introduction

The test simulation and training system of a missile is the corollary equipment of the missile testing equipment, which is used to self-test and test train for testing s equipment. The system can simulate the basis electrical characteristic and testing interface of a missile, and can be connected the testing system with testing cables. Controlled by self-testing program, the test system can check the validity of all the hardware interfaces and software programs, at the same time it can respond the fault with advance arranger.

Design of hardware system

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A. *Hardware component*

Fig 1 is the hardware frame of system, it is composed of the controlled programmable logic device (CPLD), the signal forming and driving circuits, the simulation circuit of starting and spinning winding, the unsaturated voltage forming circuit, the initiating explosive device resistance simulation circuit and power supplies.

CPLD is the control center of the whole circuit. Using the crystal oscillator output as the time base, it can produce different time and frequency signals exactly, such as the gyro frequency, the linearization period and the missile rotation signal etc [1]. Besides, by controlling time of gyro frequency, CPLD can implement the simulation of gyro starting and spinning time.

For watching the state of aim simulation turn table, a serial data receiving circuit within the CPLD can intercept the command and data from IPC in testing system, which are sent for turn table. Then it can decode the command and implement the control of target information (Uxx) signal and seeker zero (Udy) signal based on the coding of command.

At the same time, CPLD can test the phase reference signal to control the frequency of rudder control signal to be the linearization frequency signal or pulse width modulation signal. In addition, a debug circuit in the CPLD can simulate different signals by controlling debugging switches to debug and test circuit board.

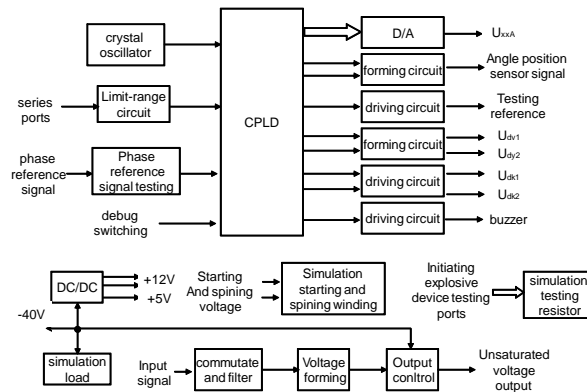


Figure 1. Hardware frame of the system

B. Principle of circuit

The information signal is produced by D/A converter, which is formed target information signal according to sinusoidal rule or small square signal to simulate noise of infrared seeker. The system is used of 8 bits D/A converter DAC0832, the output voltage of which is changed by the output data of CPLD [2].

The angle position sensor signal forming circuit is composed of switches and limit-range circuit, as is seen in Fig 2. By controlled of CPLD output signal, the two transistors are conducted alternately. During the conduction state, the output signal is limited $\pm 1.5V$. The switching frequency of angle position sensor is controlled by conduction time, within 2seconds the frequency is 60Hz; after 2 seconds it is 100Hz, which can simulate the starting and spinning course of gyro.

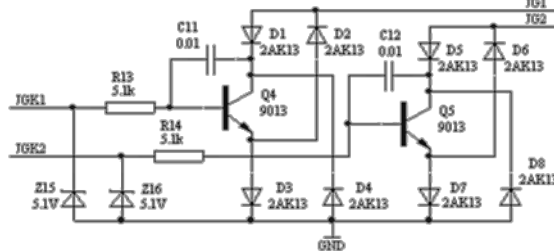


Figure 2. The angle position sensor signal forming circuit

The unsaturated voltage forming circuit is composed of commutated circuit, filter circuit, voltage forming circuit and output controlled circuit, as is seen in Fig 3. After commutated and filtered, the input voltage (7V or 22V) is formed direct voltage in a dot, and then other output voltages are formed through regulators and resistor networks according to different demands of missile testing.

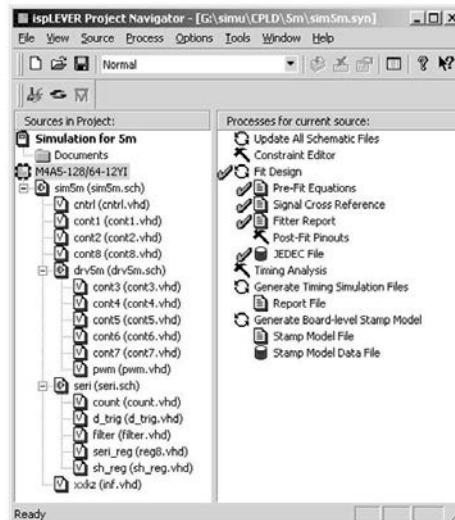


Figure 3. The unsaturated voltage forming circuit

When the output voltage of power supply is zero, the voltage +12V is not exist, transistor Q6 is conduction, diode Z3 and Z6 are worked, and the -80V output port is output -6V voltage, the -40V output port is output -2.7V voltage.

When the output voltage of power supply is -40V, transistors Q6 and Q7 are cut off, and the -80V output port is output -16.5V voltage.

When the output voltage of power supply is -43V, transistor Q6 is cut off, while transistor Q7 is conduction and the -80V output port is output -9V voltage.

The action of transistor Q8 is preventing unsaturated voltage forming circuit from error output by over loading. Apparently, when the -80V output port is not given -40V voltage, transistor Q8 is not conduction, the load of unsaturated voltage forming circuit is two 20K resistances series, other circuits can not affect the output of this circuit.

The $\pm 12V$ and +5V power supplies are produced by DC/DC converter and linear regulator. Firstly, the DC/DC module (PKF4713) change -40V input voltage to +12V output voltage, then 7805 chip change +12V voltage to +5V output voltage. The -12V power supply can be produced from -40V power supply by linear regulator.

Initiating explosive device conduction resistor is simulated by exact resistance. Namely, the required resistors are prepared on the conjunctive pots of corresponding pins in missile testing system.

Function module of software

The programmable logic chip of CPLD is ispM4A5-128/64 produced by Lattice Company [3]. The design tool is used LEVER 2.0, which is CPLD design tool in the company. Fig 4 is the inner logic structure of the software, in which sim5m is the top module to define the pins of chip and signals of different function modules. The function modules in the chip are including:

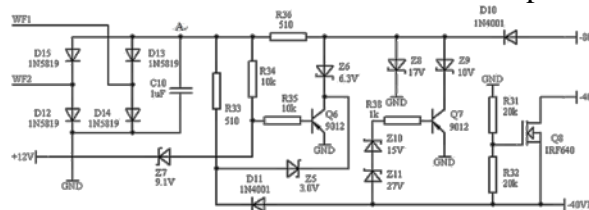


Figure 4. The inner logic structure of the software

C. Signal driving module (*drv5m*)

This module can produce the rudder control signal (DK), the seeker signal (DY), angular position sensor control signal etc [4]. Controlled by phase reference signal, the rudder control signal is the square which period is 30ms or pulse signal; Controlled by series command, the seeker signal is one or two squares output; Controlled by series command, the frequency of the angular position sensor control signal seeker signal is 60Hz or 100Hz.

D. Information data forming module (*xxkz*)

Using VHDL language and controlled by series command, the module can simulate information signal or noise signal through forming sin signal or square signal data.

E. Series command receiving module (*seri*)

The module can receive asynchronous series data by 2400bps baud rate, then filter invalid data and receive valid aim simulation turn table command.

F. Series command coding module (*cntrl*)

Using VHDL language, the module can code the series command and form command to control signal driving module and information data forming module.

G. Counter module (contX)

Using VHDL language, the module can count and time the time base signal and form all the different codes to drive other modules working [5].

H. Assistant module: including buffer

Register and multi-selector etc. the assistant module can complement some simple function such as controlling buzzer etc.

Acknowledgment

The test simulation and training system of a missile not only can replace the missile as a test system debugging、 verification and self testing object, but also can reduce the testing cost of missile. Because of using the CPLD, the system has the advantages such as better generality, higher automaticity, easier maintainability etc. By testing, the test simulation and training system can work with the test system harmoniously, and is proved useful.

References

- [1] Yang Bo,Wang Hongke, Zhu Yanli.Parallel Design Method and Realization of General Missile Test Simulation and Training System[J]. Computer Measurement & Control 2012,20(7): 1904-1909.
- [2] Du Jiang,Chen Tao,Zheng Jianhui.Study and Application of Adaption Means of Measurement &Control Signals in Missile Launch Control system[J]. COMPUTER MEASUREMENT & CONTROL,2010,18(1) :104-106.
- [3] Qi Xiaolin, Ji JuanZhao.Principle and Realization of Missile Simulator for a Fighter[J].FIRE CONTROL & COMMAND CONTROL, 2002,27: 48-49.
- [4] LI Gao-sheng,LIU Pei-guo. Design of Simulation and Training System for Antiaircraft Forces[J].RADIO ENGINEERING OF CHINA,2011,41(1):47-50.
- [5] XUE Xiao-bo,LI Zhi-bin,PENG Xue-feng.Design of Missile Simulator Based on 1553B[J]. ORDNANCE INDUSTRY AUTOMATION.2006, 25(11) : 19-20.