Research on High-speed PCB Design Based on Signal Integrity Analysis

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Abstract. With the development of manufacturing techniques and hardware devices, the need for high-speed chips is bursting. As a review report, we analyze the fundamentals and latest progress of modeling, analysis, and design technologies for signal integrity and electromagnetic compatibility on PCB and package in the past decades. Most results in this area are very rich and highly education during his long scientific career based on Professor Clayton Paul's literary creation also consider the inclusion variability of parameters, it is shown how statistical simulation can be affordable by the recently introduced stochastic method. As the final conclusion, we take into consideration of the necessity of practical training of designers and an experience relying on realistic PCB demonstrators is illustrated and discussed.

Introduction

Electromagnetic compatibility and signal integrity are one of crucial technologies in the future for electronic product design. The main reasons are high data bandwidth demand for next generation high performance computing (100+ Gbps), cloud communication/computing (50+ Gbps), and client devices (20+ Gbps). EMC and SI technologies on PCB or package will be one of the bottlenecks to achieve such high data bandwidth. Clayton Paul a few EMC and SI field has made a pioneering contribution. He condensed the basic theory and requires knowledge of the EMC and SI two masterpiece design book [1], [2]; and then, in more recent times, he published a series of more books [3], especially the design of high speed digital system. This information not only guided electromagnetic compatibility and PCB in the past few decades, some new techniques of silicon research direction and inspiration, but at present still unmatched, many years of electronic systems development influence. In this paper, the fundamentals and latest progress of EMC and SI design technologies on PCB are overviewed. In addition, methods and tools for the simulation of a circuit, with the inclusion of parameters' variability effects on its electrical behavior, are needed to avoid very expensive re-fabrication. Finally, EMC engineering education is a fundamental step to achieve well-designed and performing devices. “Seeing is believing” particularly applies to design for EMC, where most effects are felt as “black magic” and teaching using only texts and equations is insufficient. The IEEE EMC Education Manual proved to be a powerful tool for teaching practical skills and Clayton Paul was a great contributor for the EMC community also in this respect.

Link-path Model and Differential Signal

Link-path Modeling and Analysis. A link path includes a whole electrical interconnect starting from a chip sending a signal and terminating at a chip receiving the signal. Signal integrity can be if the link path can be represented as a lossless transmission line to maintain perfect. In reality, the link path usually consists of several different conductor geometry. Figure 1 shows an example of a link path. It begins with a transmitter chip, through the micro convex, the package substrate, BGA ball, holes or stripline, microstrip circuit board, and at the end of the receiver chip. The signals will be distorted both in amplitude and timing due to the nonideal effects of the link path, such as frequency-dependent loss of package and PCB substrate, impedance variance, crosstalk coupling, etc. An eye diagram is a common way for evaluating the quality of signals propagating on a link path. It is constructed by slicing a long stream of Pseudo-Random Bit Sequences (PRBS) and superimposing

the different segments of symbols with one or two bits in length. Fig. 2 shows an example of a received eye diagram. Two metrics, eye height and timing jitter, are used to characterize quantitatively the voltage and timing errors, respectively, as shown in Fig. 2.

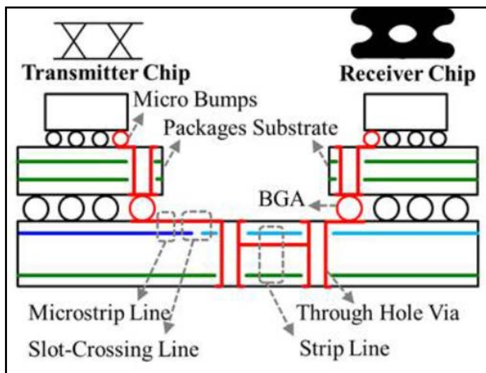

Figure. 1 The Link-Path Example

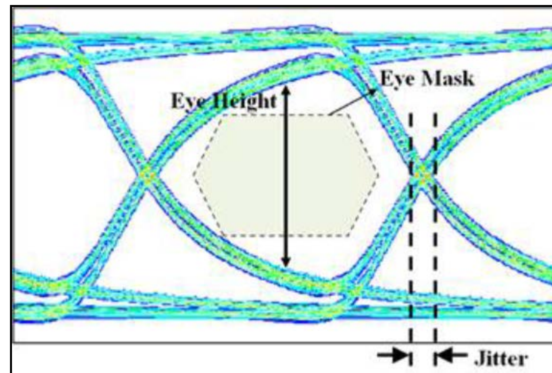

Figure. 2 The Eye Diagram Example

The Differential Signaling. The differential signaling scheme has become required in high-speed digital systems due to its high immunity to noise and high tolerance to link path discontinuities [4]. Figure 3 shows the signal in the PCB or cable poor data rate trends, such as serial advanced technology attachment, peripheral component interconnect Express (PCIe), universal serial bus, projection is 20 Gbps in the next ten years. Typically, a differential (or balanced) line is composed of three conductors (two signal conductors and one ground conductor) that support two fundamental modes, differential (or odd) mode and common (or even) mode [2]. In the differential signal system, common mode signal is usually regarded as noise, thereby reducing the signal integrity and electromagnetic interference problem caused by. The difference of link asymmetry is the main reason for a common mode noise excited by the. The asymmetry includes the rising/falling time mismatch or amplitude difference in the I/O driver circuit, trace length mismatch between two signal conductors, unavoidable imbalance routing such as bending or via transition, etc. [4], as illustrated in Fig. 4.

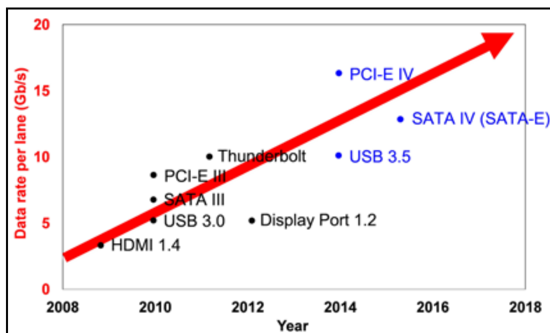

Figure. 3 The Latest High-speed I/O Interfaces

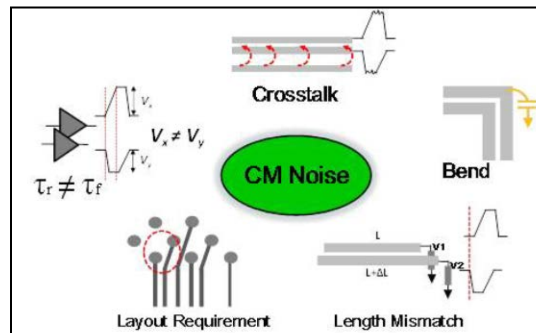

Figure. 4 The Root-cause of common-mode noise

Mathematical Analysis and Modeling

Link-path Modeling and Analysis. In order to account for uncertainties affecting the wave propagation along distributed transmission lines, we refer to the theory of telegraph equations, to which Clayton Paul significantly contributed and rigorously and elegantly described in [2]. The transmission line governing equations in the Laplace domain:

$$\frac{d}{dz}\begin{bmatrix} V(z,s) \\ I(z,s) \end{bmatrix} = -\begin{bmatrix} 0 & Z(s) \\ Y(s) & 0 \end{bmatrix}\begin{bmatrix} V(z,s) \\ I(z,s) \end{bmatrix} \tag{1}$$

Become stochastic differential equations, leading to randomly varying voltages and currents along the line. In (1), s is the Laplace variable, while in turn, (1) becomes a stochastic differential equation, leading to randomly-varying voltages and currents along the line. Any function H, carrying the effects of variability, can be approximated by means of the following truncated series [3].

$$H(\cdots,\xi)=\sum_{k=0}^{P}K_k(\cdots)\cdot\sigma_k(\varsigma) \tag{2}$$

As far as the solution of the stochastic problem is concerned, the augmented chain parameter matrix, relating the coefficients of the voltage and current variables at the line extremities, becomes:

$$T_{TL}(L,s)=\exp m\left(-\begin{bmatrix}0 & Z(s)\\ Y(s) & 0\end{bmatrix}\cdot L\right) \tag{3}$$

The Application Example. The proposed technique is applied to the analysis of the structure of Fig. 5, where the transmission lines have lengths L1 = L2 = 5 cm and the cross-section of Fig. 6. The randomness is provided by the substrate parameters that are considered to be the same for both the transmission lines, as well as by the lumped capacitance C. These parameters are considered as three independent Gaussian random variables with a relative standard deviation of 10%. The total number of terms P +1 (corresponding also to the magnification of the size with respect to the original system) is given by the following formula 4:

$$P+1=\frac{(p+n)!}{p!n!} \tag{4}$$

where n is the number of random variables and p is the order of accuracy, that represents the maximum degree of the polynomials used for the expansion[5]. Three augmented models are built for the distributed lines and the intermediate lumped section, which are indicated by their transmission matrices TTL and TC, respectively.

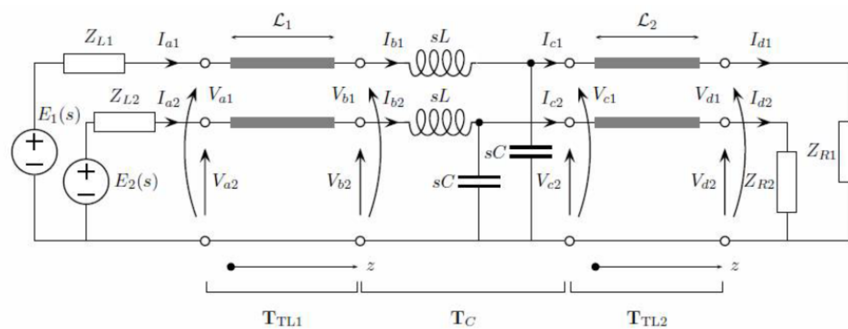

Figure. 5 The Example of high-speed data link

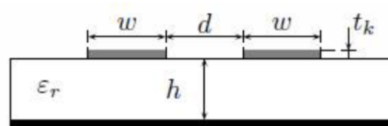

Figure. 6 The Micro-strip Cross-section

Experimental Analysis

Although the analysis is valid only for properly terminated lines, which is almost never the case in digital boards, at least there is a lot of insight to be gained from this experiment. Fig. 7 illustrates the cross-section of the experiment board (2:7 mm wide traces are needed to achieve a 50 impedance to match the available standard test cabling). The two cases -20 dB and -30 dB have been designed for the crosstalk board in the experiment set. The experiment is performed using a spectrum analyzer with tracking generator that is first calibrated to 0 dB with the input interconnected to the generator.

The result for the two traces is shown in Figure7. This demonstration is intended for helping layout engineers to determine their trace separations, once they know how much crosstalk their design can afford. This information can then be extracted from signal levels, susceptibility thresholds and the bandwidth of the system active signals.

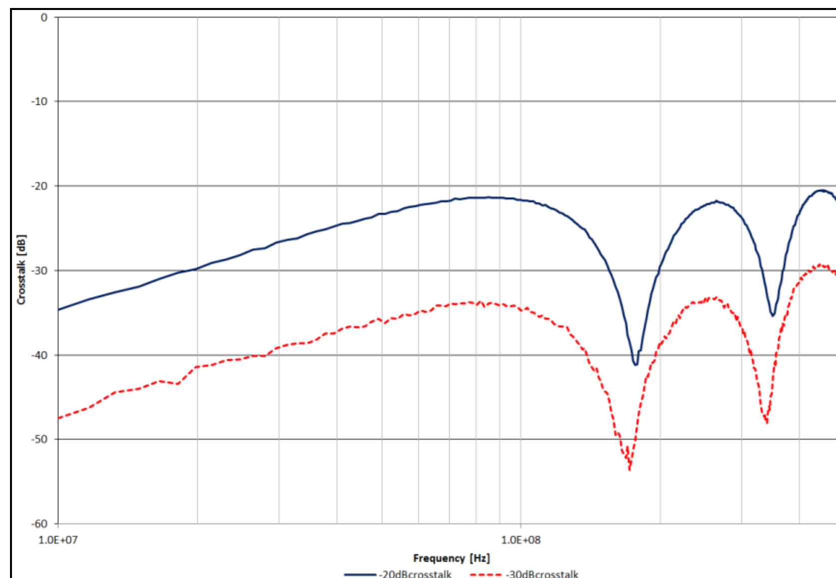

Figure. 7 The Experiment Analysis

Conclusion and Summary

In this paper, three main topics (link path, differential signal, and discontinuities) related to SI and EMC for PCB or package have been outlined and reviewed from the points of view of modeling, analysis, and design. Influence of parameter variability of inclusions are also considered, it has been shown, several statistical parameters of random simulation method recently introduced to allow the interconnection of. Finally, the PCB design education experience are described, and describe the demo board a small sample provided. In future, further research for the co-simulation and code sign to take signal integrity, power integrity, EMC, RFI into account will be one of the crucial directions that both industry and academia should pursue.

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