Research of All Digital Demodulation Technology for QPSK

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Abstract—The principle of QPSK modulation and demodulation is described and the detailed explanation and theoretical on DDC, carrier synchronization and bit synchronization principle is analyzed. A QPSK digital demodulation structure based on FPGA is proposed after detailed theoretical derivation for Costas loop carrier synchronization module.The entire system is completed on a single FPGA and use the Verilog programming language in Modelsim platform to simulate its function. Finally, a system test platform is built and the demodulated pattern is observed by an oscilloscope. The test result shows that the designed system can meet the basic requirements.

keyword-QPSK; digital demodulation; carrier synchronization ;symbol synchronization;FPGA

I. INTRODUCTION

Because of wide bandwidth, high speed transmissing rate, free space optical communication has more favorred. But the signal transmitted in atmospheric channel, it is susceptible to affected by atmospheric turbulence, strong light flashing and dispersion effect, therefore, find a suitable modulation technique is the key to space optical communication. QPSK is four phase shift modulation, this kind of modulation method has two bits of information in a symbol. Because of its technical perfect, easy to realize, strong anti-interference capability , higher band utilization advantages, it has become the one of main schemes in the modulation and demodulation technology. Therefore, this paper present a digital modulation technology for QPSK based on FPGA used in space optical communication system, omplexity when demodulation be reduced and has the characteristics of high data rate, high efficiency, it satisfies the requirement of system.

II. QPSK MODULATION PRINCIPLE

QPSK is the Quadrature Phase Shift Keying, the modulation method is that the discrete digital signal is transferred by four different carrier phase [1].By the principle of communication, expression of QPSK orthogonal modulation signal as follows: $S_{QPSK}(t) = a_n g(t)\cos w_c t - b_n g(t)\sin w_c t$ .Here, a_n , b_n is the information that modulated after serial to parallel transfer at the sender, and in the form of a binary 0 and 1 extisted, $a_n g(t)\cos w_c t$ represents in-phase component, $b_n g(t)\sin w_c t$ is the quadrature component. We can seen that the QPSK signal that after modulate can be consider as the linear superposition by two orthogonal carrier of Binary Phase Shift Keying. Assuming that the bit rate of QPSK R_b ,so the signals for I and Q after serial to parallel transferred can be regard as the binary phase shift keying signal which the bit rate is $R_b/2$. Making average power spectral density of linear superposition for the binary phase shift keying signal I and signal Q, which constitutes the average power spectral density for QPSK [2].
Block diagram for QPSK modulation as shown in Fig .1.

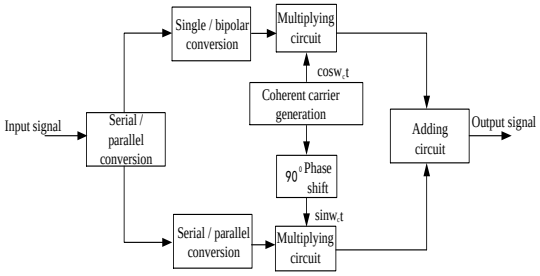

Figure 1. Block diagram for QPSK modulation

III. DESIGN FOR QPSK DEMODULATION

The purpose of demodulation is making the original baseband signal restored from modulation signal of high frequency band. Corresponding carrier frequency deviation and phase deviation existed when the signal transmissing, considing only under the condition of

phase deviation,QPSK demodulation system consists of the digital down conversion, the carrier synchronization loop and bit synchronization loop, the block diagram is shown in Fig .2.Under the digital down conversion,it realized frequency conversion from high to low that is facilitated subsequent processing, the effect of carrier synchronization loop is to obtain relatively stable carrier signal, the effect of the bit synchronization loop is acquiring the clock that has the same frequency with the transmitting signal from received signal.Both the carrier synchronization and bit synchronization are the core issue of all-digital QPSK demodulation, its performance is good or bad directly affectted the communication quality.

A. Design for digital down conversion

DDC refers to the frequency of processed signal lower than original signal, it is consisted of low pass filter (LPF), the mixer (multiplier), digital controlled oscillator (NCO) [3].Block diagram of digital down conversion as shown in Fig .2.

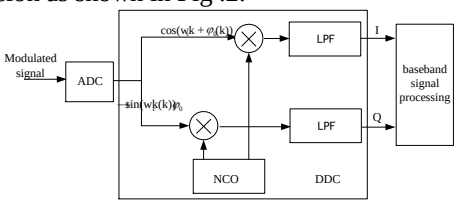

Figure2. Block diagram of digital down conversion

The orthogonal component and synthetic carrier from the local digital control oscillator repectively multiply the digital intermediate frequency signal that after sampling, then LPF used to remove noise and high frequency components for output after multiplying, the final output of DDS is a dual-channel based signal. According to law of bandpass sampling, phenomenon of spectrum overlapping is avoided as long as meetting the sampling frequency. That will be realized by signal $x_a(t)$ multiplied the complex rotation vector:

$$x_b(t) = x_a(t)\, e^{j2\pi f} \qquad (1)$$

Here f_c is the frequency of the linear moving that is carrier frequency, f_c can be either a positive or negative value, the real part of rotating vector is the in-phase component, also the image part is the orthogonal component [4].Making the (1) digital processing, and using the complex form respresents each conversion signal and the complex vector。T is sampling period, the digital frequency conversion formula is:

$$x_b(\mathrm{KT}) = x_n(\mathrm{KT})\, e^{j2\pi f_c KT} \qquad (2)$$

Formula (1) and (2) have the same meaning ,positive and negative points of f_c to distinguish up-conversion and down-conversion.

Assuming the sampling signal after AD is $s(k) = 2a(k)\cos(w_c n + \phi_c(k)) + n_k$. $2a(k)$ represents the signal amplitude of every moment, ϕ_c and w_c represents phase and frequency of the carrier signal respectively, n_k represents the additive white gaussian noise that unilateral power spectral density is $N_0/2$.The intermediate frequency signal for down-conversion realized through receiving signal s(k) respectively multiply by local oscillator signal from local NCO $-\sin(w_c k + \phi_0 k)$ and its quadrature component $\cos(w_c k + \phi_0 k)$,the two baseband signals are got ,there are $Q(k) = -s(k)\sin(w_c k + \phi_0 k)$ and $I(k) = s(k)\cos(w_c k + \phi_0 k)$,then the two baseband signals by LPF filter the high frequency components are filtered:

$$I(k) = a(k)\cos(\Delta w k + \Delta\varphi(k)) + n_{jk}$$
$$Q(k) = a(k)\sin(\Delta w k + \Delta\varphi(k)) + n_{\Omega k} \qquad (3)$$

Here,

$$\Delta\varphi(k) = \phi_c(k) - \phi_0(k)$$
$$\Delta w = w_c - w_0 \qquad (4)$$

The carrier signal got by reducing the phase difference $\Delta\varphi(k)$ and carrier frequency offset Δw until reduce to 0 using carrier synchronization modulation.

B. Carrier synchronization design

Owing to instability of the oscillator and the channel characteristics when signal transtting, it will lead to the phase error and frequency deviation extist between local carrier and received signal. The role of carrier synchronization is to obtain relatively stable carrier signal.

Usually, carrier synchronization design used Costas loop, four Costas loop used for QPSK signal, it can reduce demodulation loss and guarantee stability of system. Consider having no carrier component between phase shift keying signal that suppressed carrier and double sideband signal. In this design ,a digital phase four Costas loop is used to get synchronous carrier signal [5]. It contains four coherent demodulators, each including numerical control oscillator (NCO), phase detector, loop filter, and the input signal is the same, the principle block diagram is shown in Fig .3.

Assuming the QPSK after AD is :

$$S_{QPSK}(k) = \sqrt{\frac{2E_s}{T_s}}\cos(w_c k + \varphi_i), i = 0,1,2,3$$

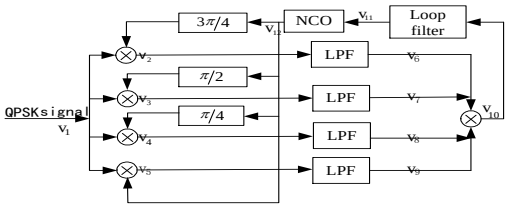

Figure3.Block diagram of Costas carrier synchronization

Here, $S_{QPSK}(k)$ is discrete signal after AD sampling, w_c is center frequency of the carrier signal. Assuming that: $v_{12} = \cos(w_c k + \varphi)$ represent outputs of discrete signal from local NCO ,it is phase difference between input signal of modulation and output of local carrier[6]. Making $S_{QPSK}(k)$ multiply by

the local signal and phase shift signal respectively, the output is:

$$v_2 = \cos(w_c k + \varphi + \frac{3\pi}{4}) \cdot \sqrt{\frac{2E_s}{T_s}} \cos(w_c k + \theta_0) =$$
$$\frac{1}{2}\sqrt{\frac{2E_s}{T_s}}(\cos(\varphi + \frac{3\pi}{4} - \theta_0) + \cos(2w_c k + \varphi + \frac{3\pi}{4} + \theta_0))$$

$$v_3 = \frac{1}{2}\sqrt{\frac{2E_s}{T_s}}(\cos(\varphi + \frac{\pi}{2} - \theta_0) + \cos(2w_c k + \varphi + \frac{\pi}{2} + \theta_0))$$

$$v_4 = \frac{1}{2}\sqrt{\frac{2E_s}{T_s}}(\cos(\varphi + \frac{\pi}{4} - \theta_0) + \cos(2w_c k + \varphi + \frac{\pi}{4} + \theta_0))$$

$$v_5 = \frac{1}{2}\sqrt{\frac{2E_s}{T_s}}(\cos(\varphi - \theta_0) + \cos(2w_c k + \varphi + \theta_0))$$

Through a LPF to eliminate the high frequency components, the output is:

$$v_6 = \frac{1}{2}\sqrt{\frac{2E_s}{T_s}}(\cos(\varphi + \frac{3\pi}{4} - \theta_0)$$
$$v_7 = \frac{1}{2}\sqrt{\frac{2E_s}{T_s}}(\cos(\varphi + \frac{\pi}{2} - \theta_0)$$
$$v_8 = \frac{1}{2}\sqrt{\frac{2E_s}{T_s}}(\cos(\varphi + \frac{\pi}{4} - \theta_0)$$
$$v_9 = \frac{1}{2}\sqrt{\frac{2E_s}{T_s}}(\cos(\varphi - \theta_0) \qquad (7)$$

The above four baseband signal through multiplier:

$$V_{10} = V_6 V_7 V_8 V_9$$
$$= \frac{1}{16}(\frac{E_S}{T_S})^2(\cos^2(\varphi - \theta_0) - \sin^2(\varphi - \theta_0) - 2\sin(\varphi - \theta_0) - 1)$$

Owing to $\sin(\varphi - \theta_0) \approx \varphi - \theta_0$, when $\varphi - \theta_0$ is smaller, making v_{10} that after approximating into the digital loop filter and than realize capture and trace. In the NCO,adjusting the local carrier frequency continuously, making the phase difference $\varphi - \theta_0$ tend to be 0, until the loop state be stability, it achieve $\varphi \approx \theta_0$ 。

C. Design of bit synchronization

Synchronization refers to the process of extracting clock signal from received signal , and the clock be synchronous as the symbol rate of received baseband signal, then accurately sampling or judging accord to the sampling clock rate on the best sampling time in order to ensure the best signal to noise ratio, the initial sending data can be demodulated exactly . There are many methods to obtain bit synchronization signal, comprising envelope detection method, differential rectification method and the digital phase locked loop method [8].Digital phase-locked method is used in this system. Data that from I and Q after matched filtering into this module, the sampling clock as input clock .At receiver , output of phase discriminator is error voltage signal that linear relationship with the synchronization error signal. The error signal is generated when two phases lag or lead time，the pulse will be deducted or plused from the digital pulse signals or pulses to be transmitted using the control modulation , thereby changing the phase of the bit synchronization signal is applied to the digital phase detector , bit synchronization output signal can be accurately tracked. Bit synchronization module structure as shown Fig .4.

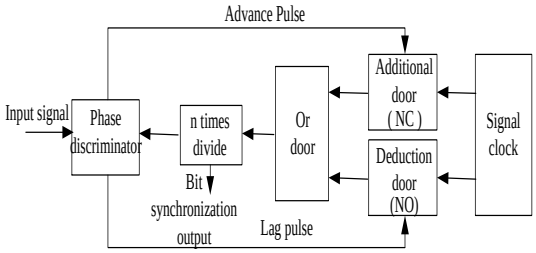

Figure4.Block diagram of the synchronization module

IV. SYSTEM SIMULATION TESTING

Through numbers of simulations to verify performance for system. Using Verilog language coded and in Modelsim software platform ,making functional simulation for QPSK modulation and demodulation signal . Logic relationship for phase encoding shown in Table 1 [9] [10].

TABLE I QPSK MODULATION PHASE ENCODING LOGIC RELATIONSHIP

Digital input	carrier phase	carrier waveform
00	0	
01	$\pi/2$	
10	π	
11	$3\pi/2$	

In Modelsim platform , port of QPSK modulation as follows :

ModeMod_QPSK (clk,reset,DataIn,Mod_QPSK);
input clk;
input reset;
input DataIn;
output Mod_QPSK;

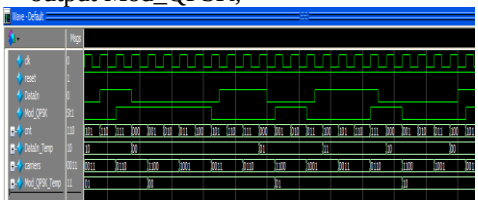

Figure 5. QPSK modulation module simulation

QPSK modulation simulation module is shown in Fig .5, noting that delays caused by register when assigned. Here ,the output signal Mod_QPSK is delayed 4 clock cycles than the input signal DataIn. QPSK

demodulation module port settings as follows:

```
   //Module Name: QPSK_DE
module
Demod_QPSK(clk,reset,DataIn,Demod_QPSK);
      input clk;
      input reset;
      input DataIn;
      output Demod_QPSK;
```

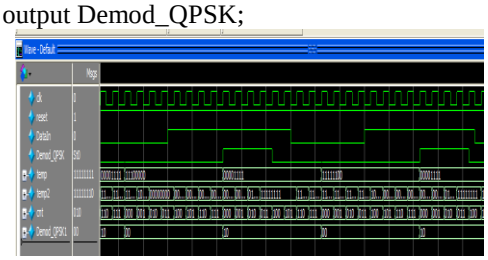

Figure 6. QPSK demodulation module simulation

Fig .6 shows the simulation results of the QPSK demodulation signal , there is a delay the same as modulation signal, from the simulation results shows demodulation function be implemented from this design.

V. HARDWARE CIRCUIT STRUCTURES AND EXPERIMENTAL TEST

The core of QPSK demodulation system is FPGA . First , modulated analog QPSK signal into the ADC is converted to a digital signal ,and then ,into the digital down conversion module ,then the I and Q two orthogonal discrete signals are available through multiply the two orthogonal signals that from the NCO output. Output signal from the matched filter contains I, Q two synchronization clock signal, the clock signal is extracted after bit synchronization module , let I, Q two orthogonal signals do interpolated output sampling judgment using this clock signal . Realizing carrier frequency difference extracted through the carrier synchronization module for the bit synchronization module output. Finally, carrier frequency difference eliminated using the NCO
phase-locked loop.

QPSK modulation signal frequency is 5GHz,
the symbol transmission rate is 5Gbps, modulated signal be amplified into ADC, the analog input signal is converted to a digital discrete signal into the FPGA chip , achieving QPSK digital demodulator. The following figure shows the waveform of QPSK demodulation from oscilloscope, as can be seen from the waveform the demodulation results consistent with the initial transmission symbols, in addition to the presence of transmission delay, achieve the demodulation function achieved by this design.

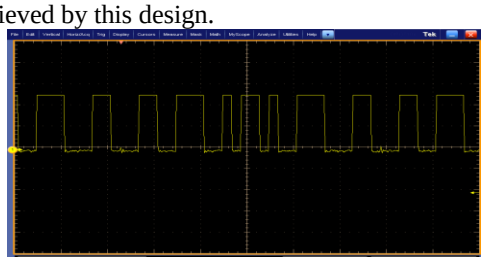

Figure 7. Waveform of QPSK demodulation

VI. CONCLUSION

This paper introduces the QPSK digital demodulation scheme based on FPGA, the system and each module has good reliability and real-time verified By system simulation and analysis using Modelsim and Matlab. From hardware test can be seen , the system can be very good for the baseband signal reduction . This design meet the requirements and has good prospect .

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