Analog Circuit Fault Simulation Approach Based on Pspice Engine

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Abstract—Pspice engine which possesses powerful modeling and simulation functions is widely used to analog circuit simulation, while can not be provided with fault simulation function. This paper addresses the problem of how to performance analog circuit fault simulation by calling Pspice engine. Firstly, the principle of the fault simulation was introduced. Under the supervision of the controller, the system carries out fault injection automatically into the target circuit, calls kernel spice3f5 simulation engine and realizes analog circuit fault simulation. Secondly, after analyzing the typical failure mode of components and the way to trigger fault, two methods of the substitution method and the equivalent circuit method are used to build the fault model libraries which conform to the simulator. At last, an experiment is designed to validate the validity and practicability of the proposed method, proving that the method can reduce the computational complexity and improve the simulation speed and the degree of fault isolation.

Keywords-analog circuit;fault simulation;fault injection; fault model; Pspice

I. INTRODUCTION

The analog circuit fault simulation method is the system verification method which on the basis of the normal circuit internal simulation system conducts fault simulation and investigates the regulation function of the system[1]. Through functional model of the system and the modeling of failure mode and influence factors of various components, the component fault simulation model within the circuit is injected into nominal simulation model to form the circuit fault simulation model[2]. Then the normal circuit model and fault circuit model after the fault injection are simulated respectively to obtain the corresponding response results. Finally it analyzes the data of the circuit simulation and verifies the robustness and fault-tolerant capability of system, which provides the basis for the design to improve system and fault diagnosis[3] .

II. DESIGN AND IMPLEMENTATION OF ANALOG CIRCUIT FAULT SIMULATION APPROACH

Fig .1 shows the framework of analog circuit fault simulation. The full system simulator is composed of several models including the CPU controller, simulation engine spice3f5, fault injector and data analyzer .Each model completes the different function through mutual coordination work between them[4]. Among them, the controller CPU is supervisory program of the whole fault simulation system[5]. It provides interface program for users and fault simulation system, as well controls the fault injector by choosing fault from fault library combined with the user fault list to inject into the target circuit on the operation of the application[6]. The analyzer will get the fault report and compare with the fault model. By comparing the data before and after the fault injection, we can verify the effectiveness and correctness of this approach.

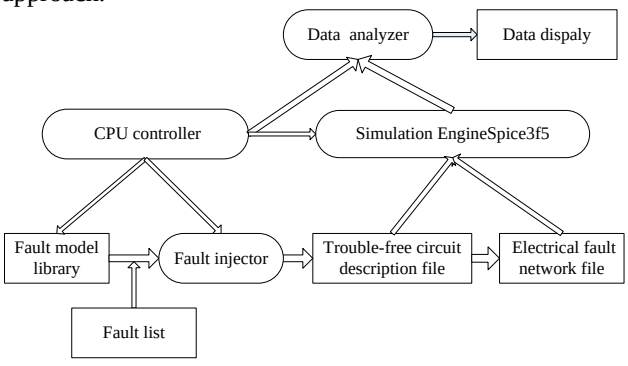

Figure 1. Analog circuit fault simulation framework

The method adopts the technological process in which it injects device fault primarily, performs simulation procedures, and verifies simulation results. The process is shown in Fig .2, and can be divided into three steps of fault injection, fault simulation and result analysis. In particular, the method starts from the bottom of the system structure to set their failure mode conforming to each specific

component failure, and then simulates the fault circuit by calling Pspice engine. Eventually it judges whether fault results simulation meets the requirements or not. Through the circuit fault simulation, preliminary results often do not agree with the ideal goal. It also needs to modify system principle and mathematical model making validation through the analysis research, as well as further compare and test to improve the fault simulation model. The established fault model must be validated and qualified after circuit fault simulation analysis[7].

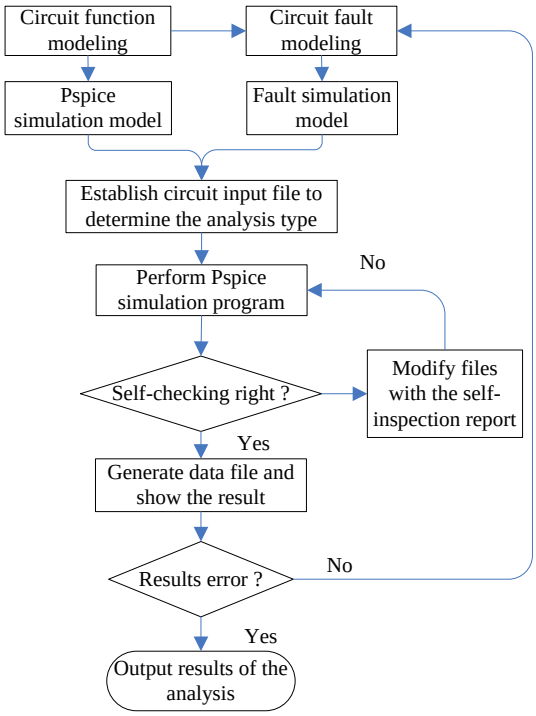

Figure 2. Flow chart of the fault simulation

A. *Fault Injection*

Fault injection technology plays a key role in analog circuit fault simulation[8]. By injecting specific fault into the system, we can observe the behavior of the analog circuit fault. Based on the spice system platform, there are three generic fault injection methods: modifying the circuit principle diagram, modifying the network topology file (netlist file), and changing model definition. The method to modify the circuit principle diagram is more visualized. Simply, the designed fault model can be directly injected into the specified location of the failure components, generating circuit fault simulation model. As fault device information was properly involved in the network topology file, the method to modify fault injection is practicable to perform the electrical fault topology network. The method to change the model definition is mainly to modify device model in the circuit model definition file to inject needed fault model[9]. After comparing and analyzing of the generic fault-injection methods, we can come to a conclusion that the essential of fault-injection methods is that designed fault models of component model are substituted for fault-free device models, thus forming a circuit network topology described by the fault factors. In consideration of requirements of the different fault types, different methods of fault injection are applied in simulation system based on Pspice[10].

The principle of fault injection is demonstrated in Fig .3. Specific steps are shown as follows.

- The injector extracts target information from the netlist including target category, the name of the table, the connection method and even the parameters.
- Data representation of various components is to use the c++ data structure to store the target information in the previous step in order to utilize the data representation of components to constitute the needed fault model further.
- According to the information of pin and injection type, the data format of the failure model is injected into the fault-free netlist file.

In accordance with the replacement addition operation and series-parallel requirements when the fault being injected, the connection mode of pins is defined to make the fault model accessible to inject faultlessly any position of circuit. With these pin connection operation fault model can be added automatically to the target circuit by consulting the specified fault list to get the corresponding fault injection circuit model.

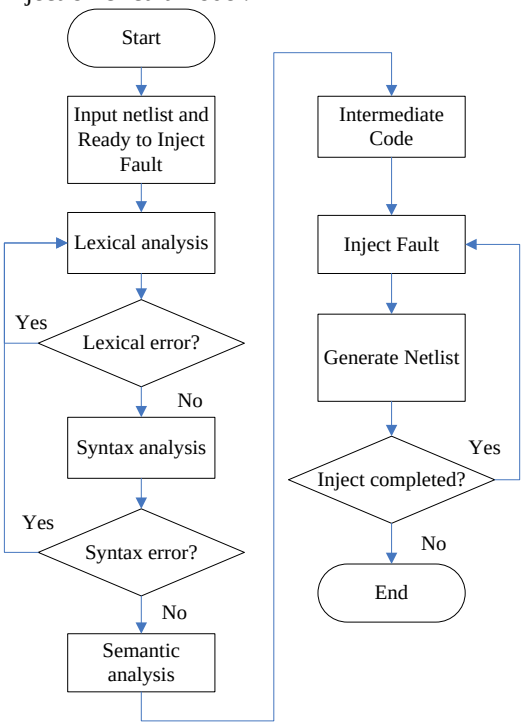

Figure 3. Principle of fault injection

B. *Fault Model*

The process of designing fault mode is closely related to circuit fault simulation. The established failure model makes preparations for accurate and quick circuit fault simulation accordingly to obtain the fault feature data to validate fault simulation further. When establishing a new fault model of high-level abstraction, the simulation accuracy of fault circuit in the low-level, which generally refers to the transistor-level fault circuit, directly determines the accuracy of the established model,

especially in the process of the analog integrated circuit fault model.

Fault modeling intends to establish failure model by taking multitudinous failure behaviors of diverse components when simulated for reference .It is general that analog circuits failure mode are divided into hard failure containing open-circuit and short-circuit fault and soft fault given priority to the parameter drift . This paper adopts the substitution method and the equivalent circuit method to analyze the typical failure mode of the components and the way to trigger fault. In general, the design of fault model follows the two standards that the designed model should conform to the requirements of the simulation accuracy and should be able to been simulated in Pspice simulation environment[11].

1) Substitution method

Two-terminal elements normally contain resistors, capacitors, inductors and diodes under circumstances of open-circuit or short-circuit. To avoid dangling node, we adopt the fixed resistance of low nominal value to simulate those resistances whose theory simulation impedance is 0 or the fixed resistance of high nominal value to simulate those resistances whose theory simulation impedance is infinite.

But minimum and maximum resistances can not observe the second standard. As is shown below in Tab.1, under the condition of DC inductance and capacitance can be used to represent resistance respectively in short-circuit and in open-circuit. Nevertheless, the error of the fault response produced by adopting the modeling method of simulating short -circuit fault and open-circuit fault with low resistance and high resistance is entirely adamantly deemed the tolerance of other components.

TABLE I. RESISTANCE FAULT MODEL

Device types	Normal parameter	Fault mode	Fault parameter	Fault model describes
Resistance	R1 RP RN Xk	DC short-circuit	LR1 RP RN 1	Inductance simulation in short circuit.
		DC Open circuit	C RP RN 1U	Capacitance simulation in open circuit.
		AC short	R1_ASHORT RP RN X_AOPEN k	A low resistance simulates the short circuit.
		AC open	R1_AOPEN RP RN X_AOPEN k	A high resistace simulate the open circuit
		Parameter drift	R1_DRIFT RP RN X_DRIFT	X_DRIFT is resistance after the drift

The capacitance of the open-circuit fault and the inductance of the short-circuit fault in DC can't be diagnosed, while other situations are similar to the resistance. By contrast, the set resistance in open-circuit instead of the resistance nominal value can be achieved by nominal value of normal resistance divided by the fault coefficient. And as for capacitors, inductors and diodes, the set resistance in open-circuit instead of their nominal value can be achieved by nominal value of the highest resistance in circuit divided by the fault coefficient. In a similar way, the set resistance in short-circuit instead of their nominal value can be achieved by nominal value of the lowest resistance in circuit divided by the fault coefficient.

2) Equivalent circuit method

In terms of the integrated circuit, since its internal structure is very complex and physical faults differ in thousands ways, equivalent circuit method is used to model .This method does not consider the inside structure of the components only except components failure pin, therefore it possesses a strong universality.

Take UA741 for example. It could be carried on the comprehensive test applying the above fault injection model. Finally, from the outside of the device views， the failure of the model has been divided into four kinds of circumstances as follows.

- Internal fault has no obvious change to the function of device.
- The output voltage varies near the power supply voltage or negative power supply voltage.
- Operational amplifier disorders.
- The output voltage will be limited to a certain region.

The first three fault modeling account for more than ninety percent of the failure, so they can cover most of the phenomenon.

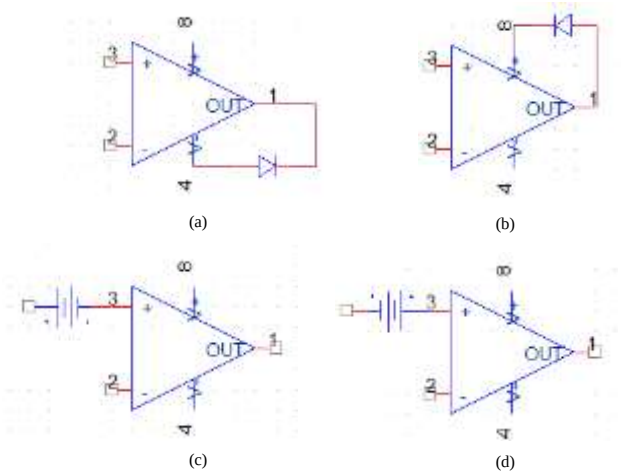

Figure 4. Fault models of UA741 device

In Fig .4(a), the diode is connected to the positive power supply, while the cathode being connected to the output terminal. With the diode conducted in this method fault model output is always stable near the power supply voltage. Similarly, in Fig .4(b), the failure model can guarantee the stability of output to maintain the negative power supply voltage. The faults of input offset voltage in Fig .4(c) and (d) are in the same way. So for integrated operational amplifier circuit, the function fault model of output voltage limited to the power supply voltage and exorbitant offset voltage can be solved completely by drawing on the volt-ampere characteristics of the diode phase combined with the characteristics of the integrated circuit itself[12].

After a great deal of experiments and analysis, now there are 17 kinds of very-frequently used fault simulation model, including R_SHORT, R_OPEN, R_DRIFT Q_OPEN, Q_SHORT, D_OPEN, D_SHORT, GUGAO, GUDI, D_ERR, D_DELAY, D_CMOS_IN_ERR,

D_CMOS_OUT_ERR, D_TTL_IN_ERR, D_OUT_RES_DRIFT, D_IN_RES_DRIFT, D_TTL_OUT_ERR. In order to facilitate inquire and injection, the model would also be classified into simulation failure and integrated fault, and respectively encapsulated in analogy-fault and integration-fault library files. In the subsequent fault injection, it is convenient to find the corresponding fault in the established model libraries[13].

III. THE FAULT SIMULATION INSTANCE

In order to validate the effectiveness of this fault simulation tool, an experiment was designed in Fig .5. The experiment is like this: with LM111 oscillator producing square-wave and applying Fourth-order low-pass filter for smoothing, window comparator is finally used to process waveform adjustment. The simulation runs on transient analysis. In the meanwhile a set of parameters transient analysis are that start time is 0 ms, end time is 5ms, and step width is 1us.

The correct output of square-wave is as shown in Fig .6. However, when the low-pass filter circuit triggers fault that the output of the LM358 chip is kept in the power supply voltage. The simulation waveform is demonstrated in Fig .7. After analysis, the simulation waveform is consistent with the actual data.

The above fault simulation test shows that the software can satisfy the requirement of most board-level circuit fault simulation, since the transient fault simulation needs a higher requirement for CPU and machine memory.

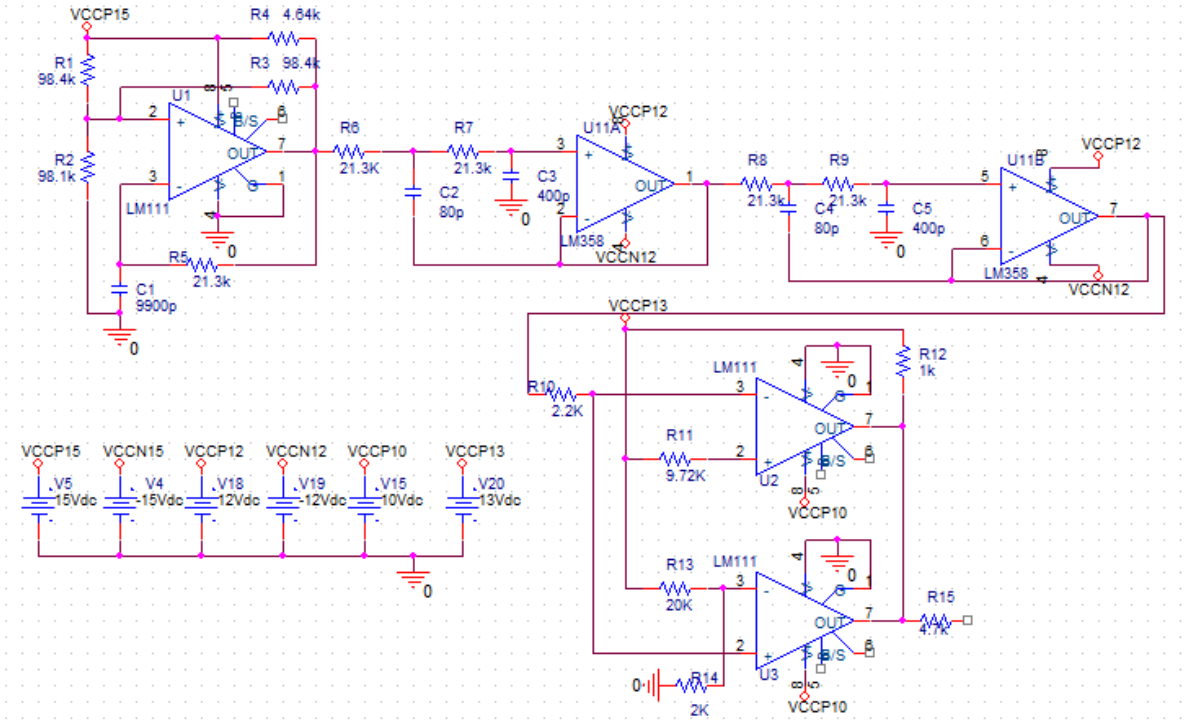

Figure 5. Simulation circuit of square-wave generator

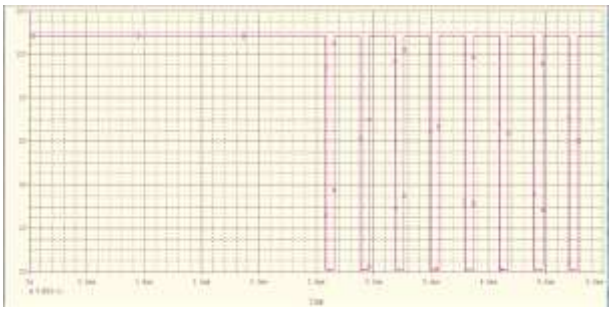

Figure 6. Transient analysis results of normal cicuit

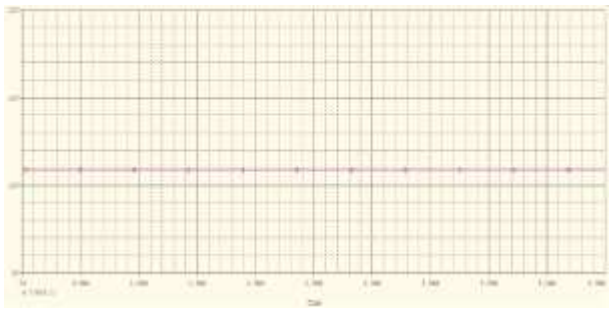

Figure 7. Transient analysis results of fault circuit

IV. CONCLUSIONS

This paper proposes a simulation framework for analog circuit simulation by means of the automation injection and calling kernel spice3f5 simulation engine. The method has established the fault library based on Pspice software. The method automatizes the process of fault simulation acquisition, can reduce the acquisition workload of human knowledge, and also has pushed a more complete, comprehensive and practical analog circuit fault simulation. As a result, our vision for the future of analog circuit fault simulation based on spice certainly includes more fault model libraries. And the system is hoped to have more comprehensive and powerful fault simulation function.

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