Research of Automatic Generating Analog Circuits Fault Tree Based on IEEE 1232

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Abstract--In analog circuit automatic generating fault tree field, several problems are as below: currently the fault tree model had not strong structural to provide the detail realization method to automatic generating fault tree and only used Support Vector Machine algorithm to automatic generating fault tree the accuracy and stability are insufficient, the generating fault tree method is non-portable. Paper combines the SVM algorithm and the fault tree model based on IEEE 1232, analyzes the characteristics of the new fault tree model, designs and put forwards the automatic generating fault tree method, the stability and the accuracy of the generated fault tree are improved, and the portability of the automatic generating fault tree method is strengthened. Paper designs and implements the automatic generating fault tree model based on IEEE1232; the results show that the feasibility of the plan, the accuracy and the stability of the new fault tree model are improved.

Keywords--analog circuit; IEEE1232; fault tree; support vector; automatic generate

I. INTRODUCTION

In analog circuit test and fault diagnosis field, the fault tree of the under test model reflect the relationship directly between each node and correspond fault, to ensure the tester could judge the fault nodes and the cause of the problem in time. Automatic generating a stable and accurate fault tree is the problem to be solved urgently. Currently the fault tree had not strong structural to provide the detail methods to implement automatic generating fault tree, when automatic generating the fault tree only through the SVM algorithm, because of the fault tree is limited by the using intelligent algorithm and the ability is not available to identify data, the fault tree is not accuracy and non-portable. Paper presents an analog circuits automatic generating fault tree method based on IEEE1232, the method combines the IEEE1232 fault tree model with the SVM algorithm, realizes stability model system to invoke the SVM algorithm, by the new fault tree model the accuracy and portability are improved.

II. AI-ESTATE

The Artificial Intelligence Exchange and Service Tie to All Test Environments (AI-ESTATE) standard was developed by the IEEE Standards Coordinating Committee 20 (SCC20) on Test and Diagnosis for Electronic Systems to serve as a standard for defining interfaces among diagnostic reasoners and users, test information knowledge bases, and more conventional databases. In addition to interface standards, the AI-ESTATE standard includes a set of formal data specifications to facilitate the exchange of system under test related diagnostic information [1] [2].

A. AI-ESTATE architectural

The diagnostic reasoners which are conformed the IEEE1232 standard invoke Dynamic Context Model's lower model-- Fault Tree Model to automatic generating the fault tree, the model automatic analyzes the tree of nodes data to complete test and conclude the fault conclusion. Fig .1 shows the AI - ESTATE structure model and universal model, including IEEE1232 standard diagnostic reasoners, the information management system, the system supports application, test environment and the Common Element Model (CEM) contained in the four kinds of models: the Fault Tree Model, Bayesian Networks Model, Diagnostic Logic Model, Dmatrix inference Model [3].

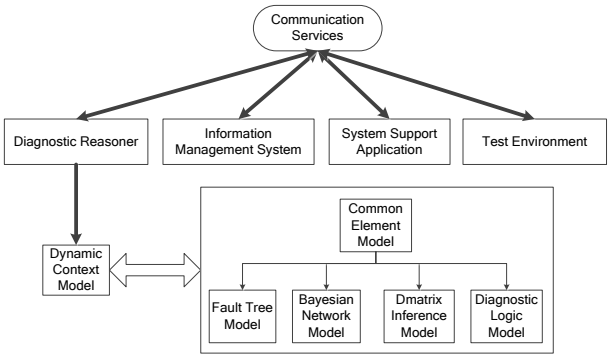

Figure 1. AI-ESTATE architectural

B. AI-ESTATE Fault Tree Model

AI - ESTATE fault tree model provides the special structure of the fault tree system test and the diagnostic methods, it does not need to use the test strategy of reasoning system and it uses the test steps of AI_ESTATE_CEM: a node or steps corresponds to a test entities, Each branch from a node corresponds to one of the possible outcomes for that test. Diagnostic reasoner uses fault tree to recommend an entry point (node under test) to the client application. After the confirmation from client, diagnostic reasoned handling the fault tree messages from the entry point, executing the test associated with that step and proceeding with the actions prescribed for the outcome those results. When all of the steps finished, the test will determine the diagnosis; if there is no other fault tree steps the test is completed.

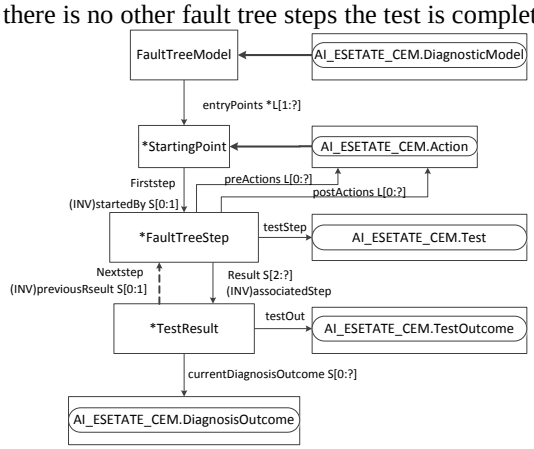

Figure 2. AI-ESTATE Fault Tree Model

C. AI_ESTATE_FTM invoke SVM

Support vector machine algorithm can be used in the data feature extraction, and analyzes the data to automatic generating fault tree. Through the studies and analyzes the SVM algorithm can build its special model, but there is not a standard to constraint the method, the fault tree is non-portable and inaccurate which is built in this method.

Embed the SVM algorithm in the AI_ESTATE_FTM structure, not only solved the problem that AI -ESTATE did not give a detail methods to generate the fault tree, also solve the problem that the exclusive model which is created by SVM algorithm is inaccurate and non-portable. Fig .3 shows the whole process of the AI_ESTATE_FTM invoke SVM.

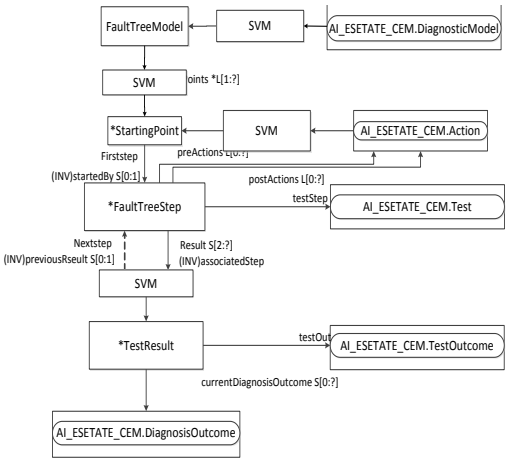

Figure 3. AI_ESTATE_FTM invoke SVM

The part EXPRESS code of AI_ESTATE_FTM invoke SVM algorithm is below：

EXPRESS *specification:*

*)

ENTITY FaultTreeModel

SUBTYPE OF (DiagnosticModel)；

int FaultTreeModel::invoke SVM(const int node, float **data, int len);

entryPoints：LIST [1：？] OF UNIQUE StartingPoint；

END_ENTITY；

(*

III. AUTOMATIC GENERATING ANALOG CIRCUITS FAULT TREE MODEL

By calling the SVM algorithm, AI_ESTATE_FTM modified the fault tree test steps, the initial node, test rules, the test results, the results outcome and several modules, provided a detail realization method of the automatic generating fault tree, and made the framework of AI_ESTATE_FTM perfectly. The automatic generating fault tree method had strong portability; it can be applied to most of the analog circuit fault diagnosis. Fig .4 shows the process of analog circuit fault diagnosis invoke fault tree module automatically: firstly, feature extract the simulation data, then import the data in automatic generating fault tree module, the module invoke AI_ESTATE_FTM to generate the fault tree to test and get the fault node automatically, finally, contrast the fault node and the known fault index table to get the conclusion that whether the automatic generating fault tree is correct.

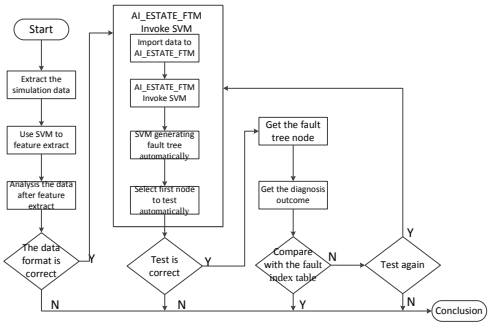

Figure 4. Flow chart of an Analog circuit fault diagnosis invoke AI_ESTATE_FTM automatically

The process of AI_ESTATE_FTM invoke SVM algorithm to generate fault tree as shown in Fig .5, firstly, determine whether the first node is failure, then iterate through all the data select node to judgment automatically, finally summarized the total error data to inference fault nodes and fault type.

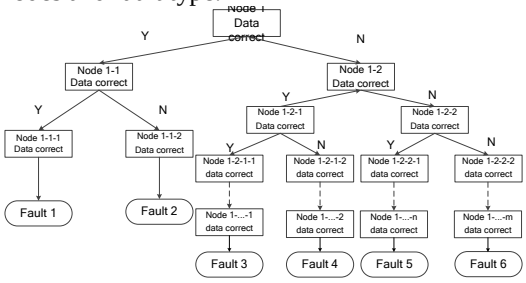

Figure 5. The specific methods of AI_ESTATE_FTM invoke SVM algorithm to test fault

IV. EXPERIMENT

TABLE I. SHOWS FAULT COVERAGE PERCENTAGE.

Fault Num.	Original Method	Using AI_ESTATE_FTM
F1	Success	Success
F2	Success	Success
F3	Success	Success
F4	Fail	Success
F5	Success	Success
F6	Success	Success
F7	Success	Success
F8	Success	Success
F9	Fail	Success
F10	Success	Success
F11	Success	Success
F12	Success	Success
Normal	Success	Success
Percentage	84.6%	100%

In order to prove the feasibility of this method, using the Fig .6 shows the four operational amplifier high pass filter as the test circuit, and inject13 kinds of fault including Normal status, using SVM algorithm to extract the feature data. Fig .7 shows the feature data which are used by AI_ESTATE_FTM to invoke SVM algorithm to generate fault tree automatically.

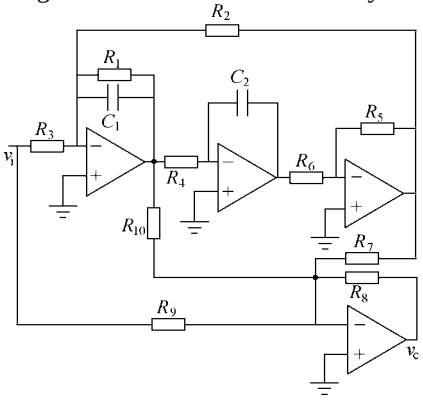

Figure 6. The circuit of four operational amplifiers high pass filter

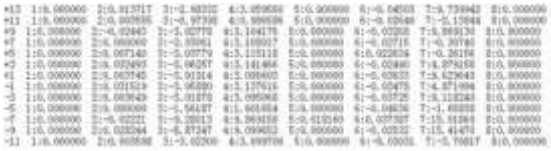

Figure 7. The feature data is used to generate fault tree automatically

AI_ESTATE_FTM combined SVM algorithm analysis the feature data which are shown in Fig .7 automatically, get the first node and the test steps, automatic generating the fault tree is shown in Fig .8.

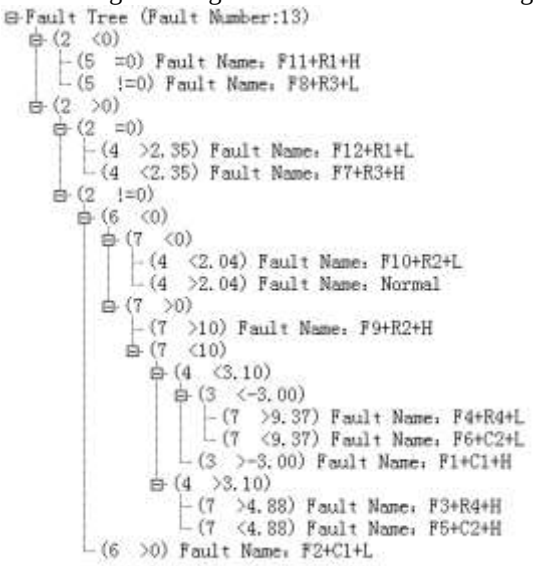

Figure 8. Automatic generating fault tree by AI_ESTATE_FTM combined SVM

Compare the original automatic generating fault tree method with the automatic generating fault tree method by AI_ESTATE_FTM invoke SVM. It proves the feasibility of this method.

V. CONCLUSION

This paper researches the analog circuit automatic generating fault tree, currently any structure could not provide the detail method to generate fault tree and the fault tree which is generated by SVM algorithm the accuracy rate is not stable, and the method to generate fault tree is single. Paper puts forward that use AI_ESTATE_FTM to invoke SVM algorithm to generate fault tree automatically, improved the accuracy rate and the portability of automatic generating fault tree method.

REFERENCES

[1] The Institute of Electrical and Electronics Engineers,“IEEE Standard forArtificial Intelligence Exchange and Service Tie to All Test Environments(AI-ESTATE),”.New York

[2] IEEE Std 1232-2010, IEEE Standard for Artificial Intelligence Exchangeand Service Tie to All Test Environments (AI-ESTATE). Piscataway, NJ:IEEE Standards Association Press, 2011.

[3] Sheppard J W;"Orlidge L A Aitifical Intelligence Exchange and Service Tie to All TestEnvironments(AI-ESTATE)-A New Standard for System Diagnostics"1997

[4] H. Goto, Y. Hasegawa, and M. Tanaka, “Efficient Scheduling Focusing on the Duality of MPL Representatives“ Proc. IEEE Symp. Computational Intelligence in Scheduling (SCIS 07), IEEE Press, Dec. 2007, pp. 57-64, doi:10.1109/SCIS.2007.357670.

[5] Jiang Huixia, Meng Chen and Fan Shuyi,"Information Model ofBinaryTreeFaultDiagnosisBasedonAl—Estate"ComputerMesurement&Control 2010.18(9)

[6] Li Nainnian and Wang Houjun;"Develop of Analog Circuit Fault Diagnoit based on Fault Tree",University of electionic science and technology of China.2012.5

[7] Wang Caihuang and Wang Jiali,"The Fault Diagnosis of Analog Cricuits based on Fault Tree"Xidian University2006.1

[8] John W. Sheppard." An integrated view of test an

[9] d diagnosticinformation standards." AUTOTESTCON Proceedings, 2002 IEEE:PP.445-455.

[10] M. Schuh, J. Sheppard, S. Strasser, R. Angryk, and C. Izurieta, “Ontology-guided knowledge discovery of event sequences in mainte-nance data,” in IEEE AUTOTESTCON Conference Record, 2011, pp.279–285.

[11] S. Strasser, J. Sheppard, M. Schuh, R. Angryk, and C. Izurieta, “Graph-based ontology-guided data mining for D-matrix model maturation,” inProceedings of the IEEE Aerospace Conference, 2011, pp. 1–12.