Research on the Fault Test Method of Digital Circuit with Microprocessor

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Abstract—The method of microprocessor circuit fault diagnosis is mainly discussed in this paper. In order to test circuit faults, this paper introduces a method of combining general bus simulation with Ant algorithm. The method is used to test the ROM of the circuit and detect the fault of the ROM by comparing the data of trouble-free ROM. But this method can't completely simulate a microprocessor, and it did not test the microprocessor itself. This is a problem that needs further research .This way need not change the hardware circuit, and bus simulation has nothing to do with the simulated bus, so this method can be used in all sorts of microprocessors, and has good generality.

Keywords-Circuit with Microprocessor Digital;Ant Algorithm;Bus Simulation Test ;Emulator ;ROM

I. INTRODUCTION

With the development of science and technology, compared to the past electronic equipment, great changes have taken place in modern electronic equipment. Large scale integrated circuit which uses the microprocessor to control is mostly adopted in modern electronic devices. The circuit is getting more and more digital, intelligent, integration, and becomes more complex [1].In some large digital equipment, integrated circuit not only plays a key role in the entire device, but also is expensive. Once fault occurs, the consequences will be very serious.

By adding large amount of microprocessors, the modern digital circuit testing is different from the previous circuit test. For example, Modern digital circuits have bus structure, so the simulation test can be used for fault diagnosis [2]. At present, the following four simulation test methods is the most used: Processor simulation test, Memory simulation test, DMA simulation test and Bus cycle simulation test [3].However the above four methods have some of disadvantages. Because the circuit under test of microprocessor need be unplugged, it is limited to use the processor simulation test. Since the memory simulation is limited by the processing speed of the microprocessor, the test processing takes a long time. DMA simulation requires a microprocessor with DMA on the circuit tested. However, it is less versatile, in many cases. With bus cycle simulation, the functions of different microprocessors are variation, so it is difficult to write test program basing on different microprocessor. Compared with the above 4 methods, This paper adopted a kind of universal bus emulation test method [4] based on Ant Algorithm which overcome the problem of poor universality, save memory, and enhance efficiency.

II. THE INITIALIATION OF SEQUENTIAL CIRCUITS BASED ON ANT ALGORITHM

A. Ant Algorithm

It is very important to have a correct initialization sequence before testing circuit. The ant algorithm is applied to initialize the generation of sequential circuits by its efficiency. The theory was put forward by Marco Dorigo in his doctoral thesis in 1992[5]. Ants have the ability to find the shortest path between the nest and food.

B. Sequential initialization method

In Automatic Test Pattern Generation (ATPG), A test sequence represents a binary string which is composed of "0" and "1". The test sequences are found for initializing the trigger. It is used as a stimulation to join the circuits in the process of test generation. Binary string is been defined as the path ant to go through. The "0", "1" is as a path to the node. The change of "0""1" means altering path. Such as "10010…, 00010…, 11110…" respectively represent different paths. As shown in Fig .1.

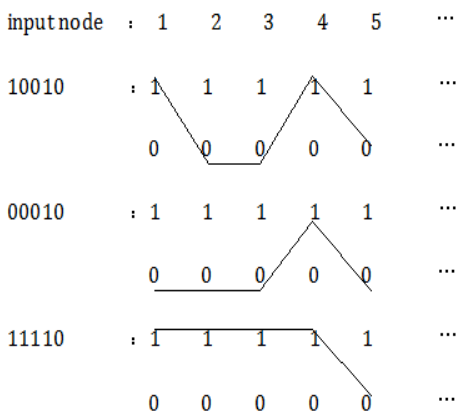

Figure 1 path representation

Supposing that the whole path consists of N nodes, each node is composed of "0" or "1" which are also the choice of ants, that is to say, choosing between"0" and "1".It is not successful until the end of N node selection. After the selection of N nodes was completed in a path and the result of the selection reflected in the circuit, a time frame conversion was finished.

Algorithm steps are as follows：

(1)Preprocessing circuit structure, the stack of input out-fan in each PI node is partitioned.

(2)The number of ants (M) is initialized .As the first ant setting out, the probability of selection "0" or "1" is equal in the PI node, because there are no clues to be depended.

(3)If the one ant succeeds in getting food, the path will be added to a series of initialization assemble. The results of simulation are updated by the pheromone updating rule. According to the rule of the state transition, the next one selects the path as the next PI, and the state of the circuit updated. Otherwise, the ant is deemed to end or called giving up this sequence. Therefore, it is necessary that the other ant is released for routing selection.

(4)For all ants, the steps (3) don't stop working until the M ant has (ants have) completed the path selection and all triggers have been initialized. Then the initialization process is ended. Finally, various test results are reported.

III. FAULT TYPES

A. *Bus Fault*

Bus structure is an important part in the circuit with microprocessor. It is the public information channel of CPU, memory, input and output. Typically, there are many multiple devices hanging on the bus, whether the bus is articulated directly affect the normal operation of the device on the bus, so the bus fault is the most important failure in a microprocessor system. Failure bus is usually static faults, it is divided into fixed faults and bridging faults [6].

The bus fault is generally static, and divided into fixed level faults and bridging faults. Fixed level fault (including fixed at "0" fault, fixed to "1" fault).

Fixed level fault, also known as sluggish fault, the main performance is a signal of a system or circuit in a signal line in the work process always maintain a certain level. Bridging faults (including "or" bridging faults, "and" bridging faults), also known as the adhesion failure, are caused by wire short circuit failure.

Test principle:

(1) If a signal line on the bus will respond to different test patterns have been fixed to 0, then the signal line is considered as fixed 0 fault;

(2) If a signal line on the bus to respond to different test pattern has been fixed at 1, then the signal line fixed 1 fault.

(3) If two or more signals on the bus line to respond to different test pattern is always the same, the occurrence of bridging faults between them.

In order to determine which bus fault has occurred, Scholars have put forward some bus test pattern, such as Abraham JA and Thatte SM proposed bus test pattern matrix for the bus to be tested. However, this test method cannot be more than large ones to judge "and" failure. As used herein, the excitation matrix bus test pattern can distinguish various bus faults. Provided the stimulus matrix is matrix T.

$$A=\begin{Bmatrix} 0 & & & \\ & 0 & 1 & \\ & & \bullet & \\ & 1 & & \bullet \\ & & & 0 \end{Bmatrix}_{N*N}$$

$$B=\begin{Bmatrix} 1 & & & \\ & 1 & 0 & \\ & & \bullet & \\ & 0 & & \bullet \\ & & & 1 \end{Bmatrix}_{N*N}$$

$$C=\{1 \quad 1 \quad \bullet \quad \bullet \quad 1\}_{1*N}$$

$$D=\{0 \quad 0 \quad \bullet \quad \bullet \quad 0\}_{1*N}$$

Excitation matrix: $T=\begin{Bmatrix} A \\ B \\ C \\ D \end{Bmatrix}$

N is the bus routes. A, B is a diagonal matrix. C, D is the rows of the matrix.

Using the incentive matrix T, and analysis the output test can accurately determine the level of fault, and bridging faults [7].

B. *Microprocessor Fault*

The chip fault mainly shows by pin connection fault and structure fault of the chip inside. The same as bus fault, the pin connection fault divided into fixed level faults and bridging faults [8]. In the actual fault diagnosis, due to the internal structure of the chip complexity, it does not require a diagnosis of chip which part is in trouble, the chip just need functional test.

IV. EXPERIMENTAL METHODS AND EXPERIMENTAL RESULTS

A. Experimental Methods

When the circuit with a microprocessor using simulation tests for trouble shooting, the simulator replaces the microprocessor on the circuit board, being competed the fault diagnosis of the devices which hang on the bus by gaining control of the bus,

Because the initial state of the circuit cannot be determined, firstly the method of Ant Algorithm is used to make the circuit fast initialization, then facilitating the testing of the circuit. In order to operate simulation software for downloading the data bus simulation test, analyzing the test results and judging the fault, the simulator replaced the microprocessor control circuit .If analysis results indicate that all circuits are normal, the CPU will be deemed to failure[9].

The simplest microprocessor system consists of microprocessor and memory components. It is chiefly detection step for this system can be to read data of program memory. So in this paper, the correctness of the method is verified by checking the ROM

Checking fault in ROM/EPROM can be judged wheth er the data read from ROM/EPROM is correct or not. At pr esent, there are many methods to check the ROM/EPRO M, such as the original value comparison method, the odd/ even calibration method, the checksum check, and the CR C calibration method. Each of which has its own characteri stics. The methods of the odd/even calibration and the che cksum check exists the situation of false negative. Both o f the CRC calibration method and the original value compa rison method are accurate [10]. Because the test system ha s enough storage space, and the method of original value c omparison which is simple and accurate was selected .Its d iagnostic flow chart shown in Fig .2. Firstly, the original c ode are stored .Secondly, the data code in the real test are c ompared with standard code. Lastly, the diagnosis result w ill be got [11].

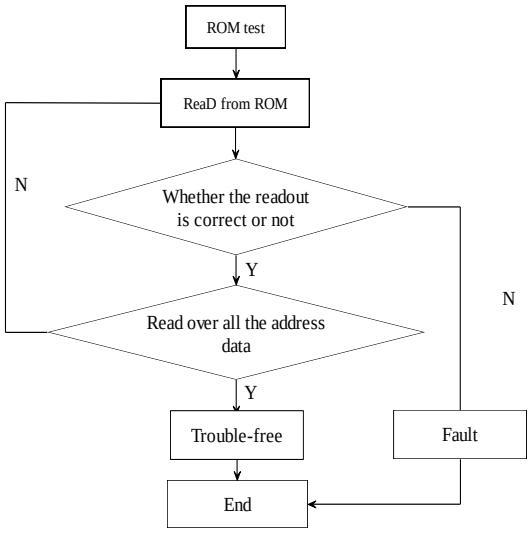

Figure2 Diagnostic Flow Chart

B. System Composition

This test system includes PC, the simulator, the circuit to be tested, etc. Test system diagram as shown in Fig .3.

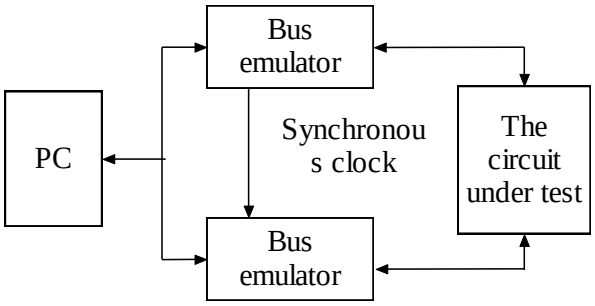

Figure 3 test system block diagram

In the test system, the function of the upper machine is to test monitoring, program writing and instruction of sending, etc. It is convenience for doing experimental that the minimum system circuit of the processor is made by stm32 and ROM and RAM of external expansion. When testing, the bus emulators and the bus analyzer work at the same time, Bus analyzer collects the response data by bus probe. Test patterns are loaded to plate detected by the microprocessor simulation head. Synchronous clock and the signal are applied to coordinate the two devices for working. The schematic diagram of ROM Bus Analyzer is Fig .4 as shown.

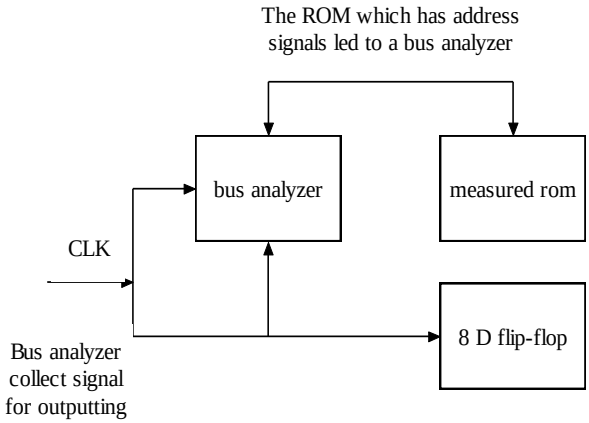

Figure 4 T he schematic diagram of ROM Bus Analyzer

C. Experimental Results

Logic analyzer is sampled the information which are obtained by bus analyzer. The response data which is read by the ROM saved to computer in binary file (rom. test), then open application software by WinHex, judged fault. As shown in Fig .5 for trouble-free ROM response data. As shown in Fig .6 for defective ROM the response data.

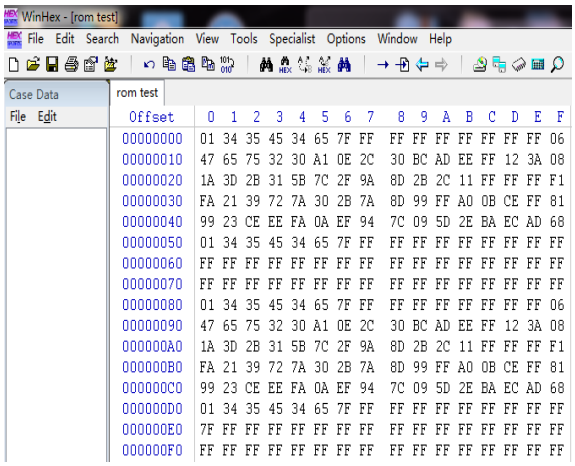

Figure 5 ROM data trouble-free

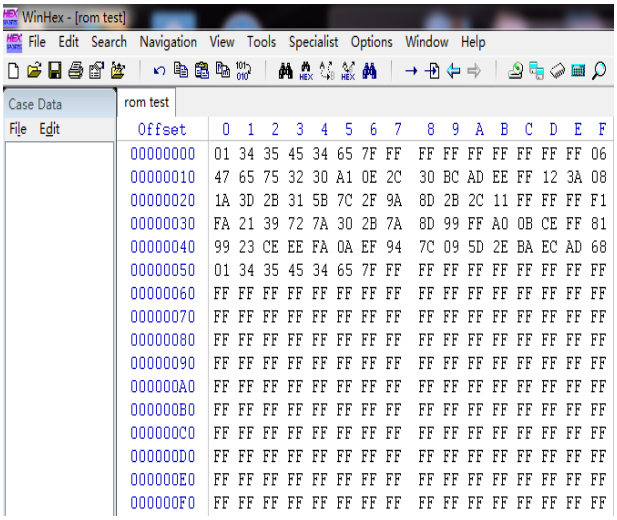

Figure6 Defective ROM data

Compare to the two images, it is easy to find the different between 80H ~FFH unit values in Fig .5 which is similar to 00H ~ 7FH replication cell values and 80H ~ FFH unit values in Fig .6. According to the method of judging bus fault, the ROM address line occurred fault of fixed 0. The process of fault judgment is also finished by computer.

V. CONCLUSION

This paper mainly introduces a kind of universal bus emulation test method. Moreover, it is method for testing the ROM to test the minimum system in a STM32. This method is still feasible to other parts of the circuit testing. To verify the feasibility of the method, ROM was only tested in this paper. The ant algorithm was used in the process of test, which has accelerated the pace of circuit initialization, and improved the efficiency of the test. And, to compare datum of the differences between fault ROM and trouble-free ROM data, fault location was realized and then, the validity of the method was verified in this paper.

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