

# High-Efficient Architectures for 2-D Lifting-Based Forward and Inverse Discrete Wavelet Transform

Tze-Yun Sung<sup>1</sup> Chun-Wang Yu<sup>1</sup> Yaw-Shih Shieh<sup>1</sup> Hsi-Chin Hsin<sup>2</sup>

<sup>1</sup>Department of Microelectronics Engineering, Chung Hua University, Hsinchu, Taiwan 300-12

<sup>2</sup>Department of Computer Science and Information Engineering, Formosa University, Hu-Wei, Taiwan 632-08

## Abstract

In this paper, high-efficient lifting-based architectures for the 5/3 discrete wavelet transform (DWT) are proposed. The proposed parallel and pipelined architecture consists of a horizontal filter (HF) and a vertical filter (VF). The system delays of the proposed architectures are reduced. Filter coefficients of the biorthogonal 5/3 wavelet low-pass filter are quantized before implementation in the high-speed computation hardware. In the proposed architecture, all multiplications are performed using less shifts and additions.

The proposed architecture is 100% hardware utilization and ultra low-power. The architecture has regular structure, simple control flow, high throughput and high scalability. Thus, it is very suitable for new-generation image compression systems, such as JPEG-2000.

**Keywords:** 5/3 discrete wavelet transform (DWT), IDWT, horizontal filter (HF), vertical filter (VF), lifting-based architecture, JPEG-2000.

## 1. Introduction

In the field of digital image processing, the JPEG-2000 standard uses the scalar wavelet transform for image compression [1]; hence, the two-dimensional (2-D) discrete wavelet transform (DWT) has recently been used as a powerful tool for image coding/decoding systems. Two-dimensional DWT demands massive computations, hence, it requires a parallel and pipelined architecture to perform real-time or on-line video and image coding and decoding, and to implement high-efficiency application-specific integrated circuits (ASIC) or field programmable gate array (FPGA). At the kernel of the compression stage of the system is the DWT.

Swelden proposed using the wavelet transform based on lifting scheme for lossy compression [2]. The symmetry of the biorthogonal 5/3 filters and the fact that they are almost orthogonal [2] make them good candidates for image compression application. The coefficients of the filter are quantized before hardware

implementation; hence, the multiplier can be replaced by limited quantity of shift registers and adders. Thus, the system hardware is saved, and the system throughput is improved significantly.

In this paper, we proposed a high-efficient architecture for the even and odd parts of 1-D DWT based on lifting scheme. The advantages of the proposed architectures are 100% hardware- utilization, multiplierless, regular structure, simple control flow and high scalability.

The remainder of the paper is organized as follows. Section 2 presents the lifting-based 2-D discrete wavelet transform algorithm. In Section 3, the high-efficient architecture for the 5/3 2-D lifting-based DWT is proposed. Section 4 presents the high-efficient architecture for the 5/3 2-D lifting-based IDWT. Finally, comparison of performance between the proposed architectures and previous works in 2-D DWT is made with conclusions given in Section 5.

## 2. The Lifting-Based 2-D DWT

Usually the Lifting-based DWT requires less computation compared to the convolution-based approach. However, the savings depend on the length of the filters. During the lifting implementation, no-extra memory buffer is required because of the in-place computation feature of lifting. This is particularly suitable for the hardware implementation with limited available on-chip memory. Many papers proposed the algorithms and architectures of DWT [4], [5], [6], [7], [8], [9], [10], but they require massive computation. In 1996, Sweldens proposed a new lifting-based DWT architecture, which requires half of hardware compared to the conventional approaches [2].

The basic principle of the lifting scheme is to factorize the polyphase matrix of a wavelet filter into a sequence of alternating upper and lower triangular matrices and a diagonal matrix [3].

Let  $h(z)$  and  $g(z)$  be the lowpass and highpass analysis filters. The corresponding polyphase matrices are defined as [3]

$$P(z) = \begin{bmatrix} h_e(z) & h_o(z) \\ g_e(z) & g_o(z) \end{bmatrix} \quad (1)$$

$$g(z) = g_e(z^2) + z^{-1}g_o(z^2) \quad (2)$$

$$h(z) = h_e(z^2) + z^{-1}h_o(z^2)$$

(3)

A factorization of  $P(z)$  can lead to upper and lower triangular matrix multiplication as

$$P(z) = \begin{bmatrix} 1 & \alpha(1+z^{-1}) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \beta(1+z) & 1 \end{bmatrix} \quad (4)$$

where  $\alpha = -1/2$  and  $\beta = 1/4$ .

The architecture of DWT based on lifting scheme involves splitting module, lifting module and scaling module is shown in Figure 1.

### 3. The High-Efficient Architecture for 5/3 2-D Lifting-Based DWT

The equations of the 5/3 1-D DWT based on lifting scheme is represented as

$$H(i) = x(2i+1) + \alpha(x(2i) + x(2i+2)) \quad (5)$$

$$L(i) = x(2i) + \beta(H(i) + H(i-1)) \quad (6)$$

According to eqs. (5) and (6), the architecture of 5/3 1-D DWT based on lifting scheme is shown in Figure 2.

The 5/3 2-D DWT is a multilevel decomposition technique, that decomposes into four subbands such as  $HH$ ,  $HL$ ,  $LH$  and  $LL$ . The mathematical formulas of 5/3 2-D DWT are defined as follows:

$$HH(i, j) = H(2i+1, j) + \alpha(H(2i, j) + H(2i+2, j)) \quad (7)$$

$$HL(i, j) = H(2i, j) + \beta(HH(i, j) + HH(i-1, j)) \quad (8)$$

$$LH(i, j) = L(2i+1, j) + \alpha(L(2i, j) + L(2i+2, j)) \quad (9)$$

$$LL(i, j) = L(2i, j) + \beta(LH(i, j) + LH(i-1, j)) \quad (10)$$

According to eqs. (7), (8), (9) and (10), the architecture of 5/3 2-D DWT based on lifting scheme can be derived and shown in Figure 3. The proposed system architecture is shown in Figure 4. In system architecture, the architecture of horizontal filter and the architecture of vertical filter are shown in Figure 5 and 6, respectively. Figure 7 shows architectures of line delays LD1, LD2 and LD in vertical filter. The architectures of  $PE(\alpha)$  and  $PE(\beta)$  in horizontal filter and vertical filter are shown in Figure 8. The proposed architecture for 5/3 2-D lifting-based DWT is described clearly.

In the proposed architecture of DWT, the data flows of the horizontal filter and the vertical filter can be derived. The architecture performs in  $(4N^2(1-4^j) + 9N)/6$  computation time, when the size of the input image is  $N \times N$  and the number of compression level is  $j$ . The architecture of 5/3 2-D DWT involves four processor elements,  $3.5N+8$  registers and seven multiplexers. The hardware utilization is 100%.

### 4. The High-Efficient Architecture for 5/3 2-D Lifting-Based IDWT

The equations of the 5/3 1-D IDWT based on lifting scheme is represented as follows [3]:

The vertical filter is represented as

$$L(2i, j) = LL(i, j) - \beta(LH(i, j) + LH(i-1, j)) \quad (11)$$

$$L(2i+1, j) = LH(i, j) - \alpha(L(2i, j) + L(2i+2, j)) \quad (12)$$

$$H(2i, j) = HL(i, j) - \beta(HH(i, j) + HH(i-1, j)) \quad (13)$$

$$H(2i+1, j) = HH(i, j) - \alpha(H(2i, j) + H(2i+2, j)) \quad (14)$$

The Horizontal filter is represented as

$$x(i, 2j) = L(i, j) - \beta(H(i, j) + H(i, j-1)) \quad (15)$$

$$x(i, 2j+1) = H(i, j) - \alpha(x(i, 2j) + x(i, 2j+2)) \quad (16)$$

According to eqs. (11), (12), (13) and (14), the architecture of the vertical filter (IVF) for IDWT is derived and shown in Figure 10. From eqs. (15) and (16), the architecture of the horizontal filter (IHF) for IDWT is derived and shown in Figure 11. In the horizontal filter for IDWT, the architecture of  $PE(\alpha/\beta)$  is shown in Figure 12.

In the proposed architecture of IDWT, the data flows of the horizontal filter and the vertical filter can be derived. The architecture performs in  $(4N^2(1-4^j) + 9N)/6$  computation time. The hardware utilizations of the vertical filter (IVF) and the horizontal filter (IHF) are 100%. The architecture of 5/3 2-D IDWT involves four processor elements,  $2N+15$  registers and ten multiplexers.

### 5. Conclusions and Discussions

Filter coefficients are quantized before implementation using the biorthogonal 5/3 wavelet. The hardware is cost-effective and the system is high-speed. The architecture reduces power dissipation by  $m$  compared with conventional architectures in  $m$ -bit operand (low-power utilization).

In this paper, the high-efficient and low-power architectures for 2-D DWT and IDWT have been proposed. The architectures for DWT and IDWT perform compression and decompression in  $(4N^2(1-4^j) + 9N)/6$  computation time, where the time unit is an addition operation. The control complexity is simple. The comparison between previous works and this work in 2-D DWT is shown in Table 1 [11], [12], [13], [14]. So far, the papers of 5/3 2-D lifting-based IDWT are rarely published. The proposed architecture for 2-D IDWT is very suitable for VLSI implementation. The design analysis of the proposed architecture is valuable for the future research.

The proposed architectures have been verified by Verilog-HDL and implemented on FPGA. The hardware code can be reused and become as IP. The advantages of the proposed architectures are 100% hardware utilization and ultra low-power. The architectures have regular structures, simple control flows, high throughputs and high scalabilities [15].

Thus, it is very suitable for new-generation image compression systems, such as JPEG-2000.

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Table 1. The comparison between previous works and this work in 2-D DWT

Architecture	Multipliers	Adders	Storage size	Computing time	Control complexity	System delay	Hardware utilization
Wu[11]	$4K$	$4K$	$K+KN$	$0.5N^2-0.67N^2$	Medium	long	100%
Marino[12]	$>(L+M^2)/4$	$>(L+M^2)/4$	$>(L-2)N$	$0.5N^2-0.67N^2$	Medium	long	$<100\%$
Park[13]	$4K$	$4K$	$K(N+J)$	$0.5N^2-0.67N^2$	Complex	long	-
Andra[14]	$4$	$8$	$N^2+4N$	$0.5N^2-0.67N^2$	Medium	long	100%
This work	$4$	$8$	$3.5N + 8$	$0.5N^2-0.67N^2$	Simple	short	100%

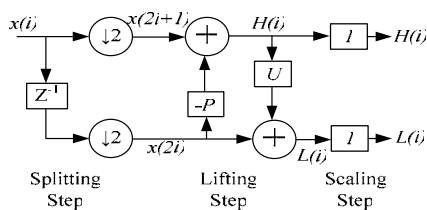


Fig. 1. The architecture of DWT based on lifting scheme

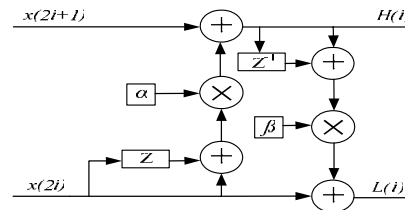


Fig. 2. 5/3 1-D lifting-based DWT

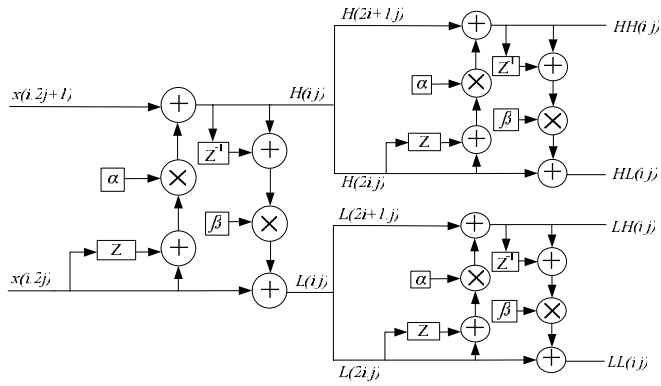


Fig. 3. 5/3 2-D lifting-based DWT

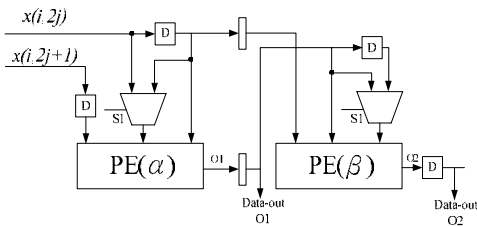


Fig. 5. The architecture of horizontal filter (HF)

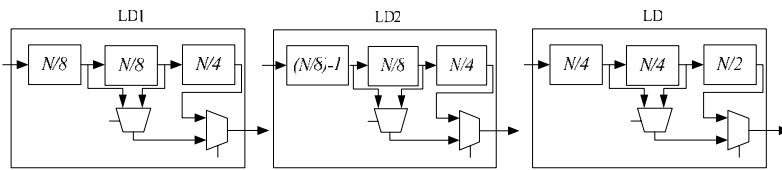


Fig. 7. The architectures of LD1, LD2 and LD

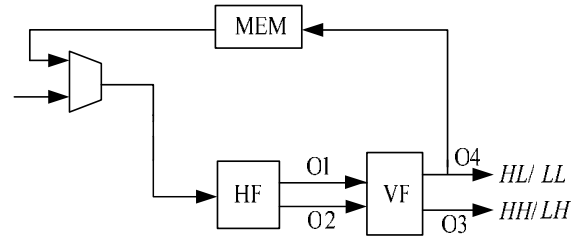


Fig. 4. The proposed system architecture of 5/3 2-D lifting-based DWT

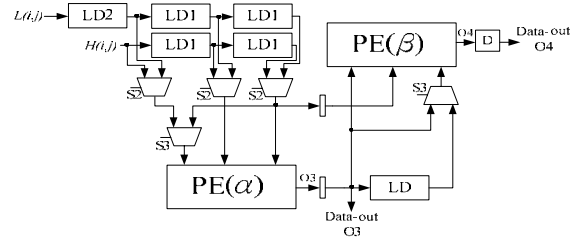


Fig. 6. The architecture of vertical filter (VF)

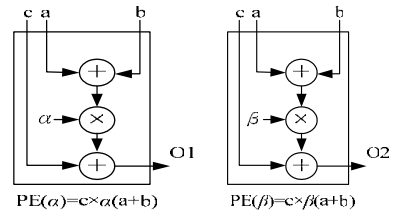


Fig. 8. The architectures of PE(alpha) and PE(beta)

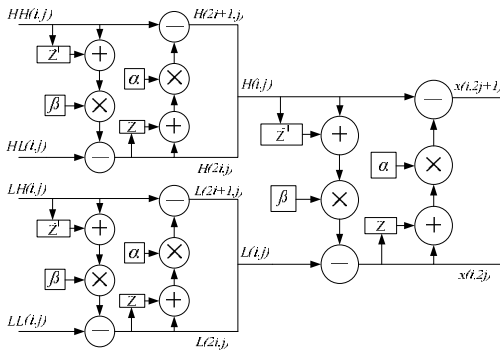


Fig. 9. 5/3 2-D lifting-based IDWT

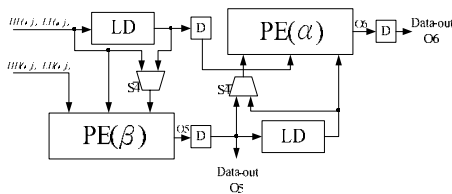


Fig. 10. The architecture of Inverse vertical filter (IVF)

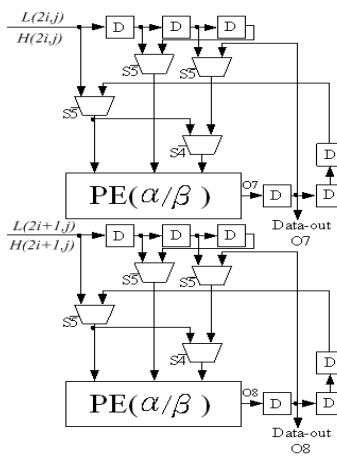


Fig. 11. The architecture of inverse horizontal filter (IHF)

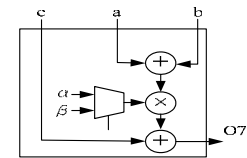


Fig. 12. The architecture of PE(alpha/beta)