# Research On High Precision TDC For Measuring The Continuous Pulses

Xia Yingqing
Institute of Physical Science and Technology
Central China normal university
Wuhan City,Hubei, P.R.China
e-mai l: y.q.xia@qq.com

Huang Honghong
Institute of Physical Science and Technology
Central China normal university
Wuhan City,Hubei, P.R.China
e-mail:214160446@qq.com

**Abstract—The system of time-to-digital conversion is based on the Field Programmable Gate Array (FPGA)[1], compared with the TDC system existing now, the innovation of this design is can measure the width of the continue pulses. This system is designed on the Spartan-6 platform of the Xinlinx company. There are three modules included in this design, the coarse count measurement modules, exact measurement modules and the manage of the measured data module. The key and the difficult of this design are in the exact measurement module, it is measured by using the carry chain which is consisted by the slices, the slices in the Configurable Logic Blocks(CLBs), which are the main logic resources for implementing sequential as well as combinational circuits, and each CLB element contains a pair of slices. The measurement accuracy of this design is within 100ps, and the measurement dynamic range is flexibility, it is based on the bits of the register used in the design, the register used in this design is 32 bits,so the dynamic range can up to about four seconds.**

***Keywords-time - digital conversion;FPGA;continuous pulses measurement;carry chain;***

## I. INTRODUCTION

The full name of TDC is Time-to-Digital Converter [2]. It is a special instruments to exactly measure the narrow pulse. High precision time measurement techniques is a indispensable key technology used in many areas, such as Atomic Physics, Astronomy Experiments,Laser Ranging and Satellite Positioning and so on[3-5]. Currently, the German company ACAM has successfully launched the TDC-GP series chips [6-7], these chips had achieved a very high measurement precision, but there is a limitation in the dynamic range of measurement[8] , and the prices of these chips is very high [9]. Compared with the TDC chip, FPGA-based design TDC has its advantages like high precision, wider dynamic range of measurement and wide application range [10-11].

nowadays, there are two implement method of TDC, one is use the Application-special Integrated Circuit,ASCI,and another is use the Field Programmable Gate Array,FPGA. This paper use the FPGA-based measurement to realized the function of TDC, Above all, in order to meet the conditions of high-precision and wider dynamic range at the same time,the method of FPGA-based design TDC has advantages like strong flexibility, short design time and low cost .Using FPGA-based TDC has a certain history research.In 1997,Jozef and his partner use pASIC-FPGA and differential time delay line method made the precision of the TDC to be 200ps,and in 2000,they used the special carry chain of pASIC-FPGA to improve the precision to 100ps.2006 AN Qi etc. Who from the University of Science and Technology of China use the spacial carry chain of FPGA reached the 50ps precision[12].In 2008,WU Jingyuan etc. firstly succeed improve the precision of TDC to 10ps by using the method of wave union[13]. Then, in 2011 Eugen who combined the wave union and Xilinx series FPGA make the precision of TDC achieved to 10ps[14-15].

## II. THE MEASURING PRINCIPLE OF TDC

As shown in the Fig .1, it is the structural schematic diagram of TDC, This design including coarse count measurement modules,exact measurement modules,control module and storage&calculation module.


Figure1 Structural Schematic Diagram of TDC

The Coarse measurement of TDC is measuring the numbers of the clk period(T0)that the pulse width contained.as the time of a clk period has been known,then we can used the number N that measured by the enumerator and the clk period(T0)to calculate the result of the Coarse measurement.

 

The exact measurement of TDC is use the interpolation technique[10-11],it is to measure narrowly pulses,the narrowly pulse is the time interval between the rising edge of signal and the rising edge of clk which following close the signal rising edge.And the time interval between the falling edge of signal and the rising edge of clk which following close the signal rising edge.Send these two narrow pulse to the carry_chain that consisted by n carry logic units,The carry logic unit is a slice of underlying resource of FPGA.Use the negation pulse of the narrow pulse to connect the flip-flop to latch the result,by this way,we can get the two time interval.

Finally, the storage and calculation module of the TDC is calculate for the all final measures, include the coarse measurement value, the exact measurement values, and the compensation value, And the calculated results is converted to decimal and send to the terminal device. We can use the result of Coarse measurement *N*T0*,the result of exact measurement *⊿ T1* and *⊿ T2* to calculatethe total time interval T.

$$T=N*T0+\Delta T1-\Delta T2 \qquad (1)$$

As shown in Fig .2, it is the principle of measurement of the TDC. the ⊿ T1 and ⊿ T2 is the value of the time intervals of the two pulse. During in the measurement process,it will have some invariable routing time delay and gate time delay,Such as the delay line between signal under test to the carry chain and the time delay of gates,these delays can be balanced by the time compensation,thus,it can reduce the error of measurement result.

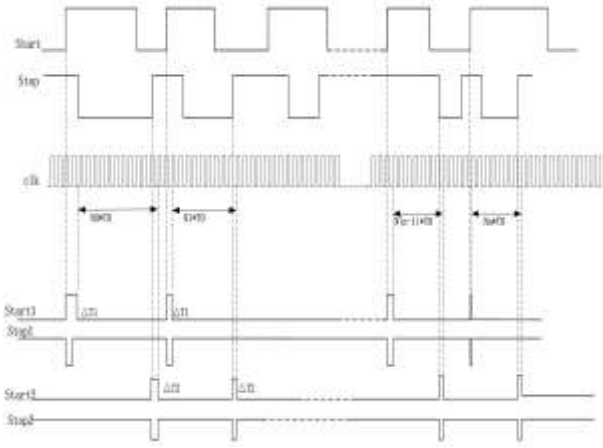

Figure 2. The measure principle of TDC

## III. The Construction of The Carry Chain

There are two slices in each CLB element, these two slices do not have direct connections to each other, and each slice is organized as a column. For each CLB, the slice in the bottom designate with the following definition. An "X"followed by a number identifies the position of each slice in a pair as well as the column position of the slice.The "X" number counts slices starting from the bottom in sequence 0, 1 (the first CLB column); 2, 3 (the second CLB column); etc. A "Y" followed by a number identifies a row of slices. The number remains the same within a CLB, but counts up in sequence from one CLB row to the next CLB row, starting from the bottom. Fig .3 shows four CLBs located in the bottom-left corner of the die.

As shown in the Fig .3, every slice contains four logic-function generators(or look-up tables,LUTs) and eight storage elements.these elements are used by all slices to provide logic and ROM functions. The another one is SLICEX, it is the basic slice,in this design, do not use this the SLICEX. The time delay between each unit is about 23*ps*, this value result can observed in the simulation.

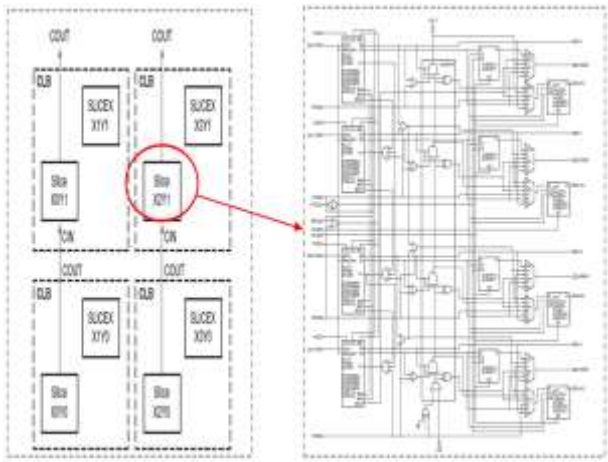

Figure 3 the Detail of the Carry Chain

The method of the exact measurement modules is interpolation technique, the measurement is conclude two parts,the measure of △T1 and measure △T2,using two same carry chain in the design. △T1 is the time interval between the rising edge of signal and the rising edge of clk which following close the signal rising edge. △T2 is the falling edge of the signal and the rising edge of clk which following close the signal falling edge. This carry chain is consisted by n slices.Put each slice in the specified location by the Verilog language. And send the start1(start2) and the stop1(stop2) to the carry_chain, the start1(start2) signal send to the delay unit, at the same time the stop1(stop2) send to the flip_flop as the latch clock. Fig .4 is the Schematic of the carry chain. Put each slice in the specified location by the Verilog language. As in the underlying resource module of SPARTAN-6, the number of slice in a vertical line is 144, as show in the Fig .3,in order to reduce the rout time delay extremely,the slice number used in a carry chain should less than 144.In this design , the delay_time of a slice is τ =93ps, as the period of the count clock is 1234ps, and in consideration of the routing time delay and the gate time delay, in each carry chain we use 40 slices,it not only can meet the requirements, but also save resources.

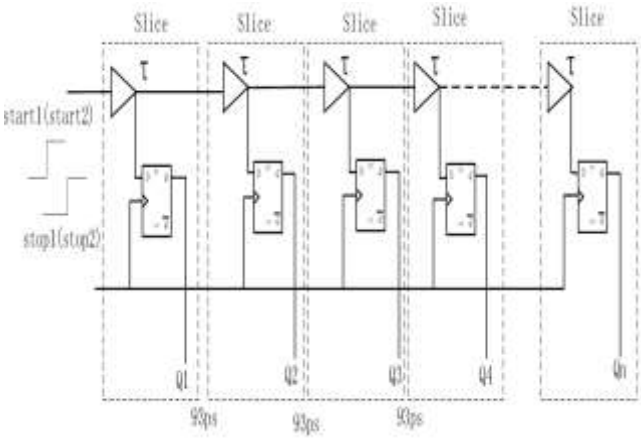


Figure 4 . The Schematic of The Carry Chain

## IV. THE RESULTS OF MEASUREMENT.

When measure the *⊿ T1*,As shown in Fig . 5, it is the result of measure *⊿ T1* of continue pulse by sent the *start1* and *stop1* to the carry chain. Observe the output port of the carry chain, if the value of S is not 4'b1111 any more ,then it is the place where the carry chain locked the delay time. We can observed from the figure, each pulse has its corresponding lock position, the larger the pulse's width, the more after the locked position by, the narrower the pulse's width, the more forward the locked position by. And we can see that the first locked position is *S[8]*, and the second locked position is *S[13]*, and the third one is *S[18]*, and so on.

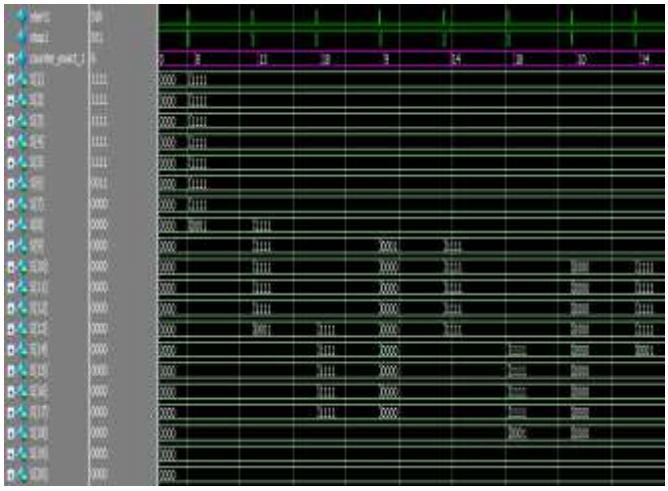

Figure 5. The Results of ⊿ T1 in Continuous Pulse

As shown in the following Fig .5, it is the measure results of the overall measurement of the width of a pulse. There are include the coarse measure value which is calculate by the counter clock. And the two exact measure values ⊿ T1 and ⊿ T2 which are precision measured through the carry_chain.

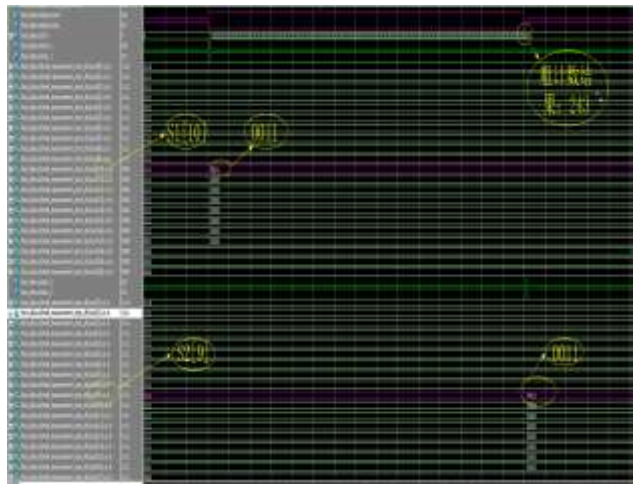

Figure 6 . The Simulation Results of ⊿ T1 in Single Pulse

According to the Fig .6, Simulation result of ⊿ T1 is the S10[3] change from 1 to 0, that is to say all the value of S0-S9 are 4'b1111, S10 is 4'b0011,and the following value of S are 4'b0000, then the time delay that go by a carry chain can be calculated out:

$$\Delta T1 = 93ps \times 10 + 23ps \times 2 = 976ps \quad (2)$$

$$\Delta T2 = 93ps \times 9 + 23ps \times 2 = 883ps \quad (3)$$

The process to measure ⊿ T2 is same as ⊿ T1, after measured the value of ⊿ T2 is 930ps,and the result of the coarse measurement N is 243, the corresponding time is 1234 × 243 = 299862ps, plus the constant compensation time, the total time interval is:

$$T = N \times T0 + \Delta T1 - \Delta T2$$

$$= 299862ps + 976ps - 883ps$$

$$= 29955ps \quad (4)$$

The actual width of the signal is set as 4400ps. For this width. Repeated measurements about 10 times, the average value of the measurements is: 3000468ps / 10 = 300046.8ps, and the error value is about 88ps, in the allowable error range.above is the result of the width of single pulse.

This design has carried on the multiple-point measurement, Measurement of the total time as shown in table

Table 2 THE MULTIPLE-POINT MEASUREMENT OF TOTAL TIME .

| No. | Actual value | Measure value | Absolute error | relative error/ % |
|---|---|---|---|---|
| 1 | 3000ns | 3000046ns | 46ps | $1.533\times10^{-3}$ |
| 2 | 450ns | 450.023ns | 23ps | $5.11\times10^{-3}$ |
| 3 | 30000ps | 30024ps | 24ps | 0.08 |
| 4 | 4000ps | 4009ps | 9ps | 0.225 |

By observing ,found that in the FPGA ,because of the routing between the logic cells in the underlying resource, will produce picosecond or nanoseconde time delay. The routing time delay impact the carry chain in three aspects: Firstly, between the flip-latch and carry

chain exist time delay, In order to reduce routing time delay, improve the precision of the data,should ensure that the flip-latch and carry chain in the same slice. Secondly,there are time delay between signal start1(start2) and c_in port of the first slice,at the same time, there are time delay between signal stop1(stop2) and the first order flip-latch. To ensure that the time delay of the two values are the same. Thirdly, There are also routing time delay between slices,to make all the length between the slices are same.above all, in order to overcome the influence of routing time delay, improve the technique of the interpolation method,and arrange the Slice of logical unit by semi-manual semi-automatic routing mode.and plus accordingly delay compensation when calculate the total time. Ensure the precision of the time data measured. Fig .7 is the optimizing routing drawing, it is the rout that from the start signal to the first slice of the carry_chain, and in this way, can shorten the time delay between signal start1(start2) and c_in port of the first slice of the carry_chain.

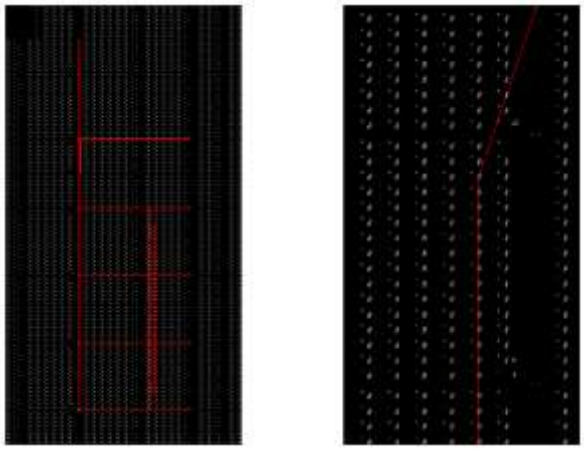

Figure 7. The optimizing routing drawing

## V. CONCLUSION

The key point of this design is to measure the width of continue pulses, and try the best to minimize the measurement accuracy and maximize the measurement dynamic range. The simulation result show that, use the special carry chain in the FPGA is an excellent method to design the TDC, and it can be applied in many field, for example, in the project we are studying now, it is used to measure the time interval between the pulses which come from different position. In the later period,we will design a calibration unit, through this unit can further improve the accuracy of the time measurement.

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