Phase-Locked Loop Technology Research Based on Photovoltaic Grid-Connected Inverter

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Abstract. In photovoltaic grid-connected system, it is an essential link to inspect frequency, phase position and amplitude of network voltage accurately and rapidly. Using DSP inner capture unit, common timer and comparing element realizes signal capture on network voltage and photovoltaic power generation, so as to reach the purpose of frequency modulation and phase modulation, as well as grid-connection condition. This paper selects network voltage positive zero-cross detection digital phase-locked loop, designs hardware implementation circuit and provides software flow pattern. The experimental result verifies the feasibility and effectiveness of this method.

Introduction

Photovoltaic grid-connected inverter not only needs to supply power for local area network independently, but also needs to connect with power grid and transit exported electric energy to power grid. In order to obtain excellent grid-connection performance and higher power factor, and avoid from impacting power grid, when grid-connected photovoltaic power generation system merges into power grid, it needs to inspect frequency and phase position of network voltage. Phase lock technique can extract phase angle information rapidly and accurately, so it becomes one of key technologies of controlling photovoltaic grid-connected device.

Phase-locked loop refers to automatic control closed-loop system that realizes phase synchronization of two electrical signals, for short PLL (Phase Locked Loop). Traditional phase-locked loop adopts the phase-locked loop constituted by artificial circuit. It exists disadvantages of complicated components, easy temperature excursion and being susceptible to interference constituted by phase discriminator, loop filter and voltage-controlled oscillator. Therefore, at present, digital phase-locked loop (DPLL) technology are adopted to finish phase lock of synchronizing signal. Digital phase-locked loop has simple hardware structure. According to different application situation, software algorithm processing has diversified forms. This experiment selects network voltage positive zero-cross detection digital phase-locked loop.

Phase Lock Principle

Zero phase lock is a phase locked method commonly used in single-phase grid connected converter. The physical mechanism of this method is: first, detecting the adjacent grid voltage of vs two positive (or negative) zero crossing, calculate the phase of S vs; and then calculate the converter output voltage of VC phase C, when Phi Phi cs and inconsistencies, cycle through the regulation of VC closed loop control system value after a certain time after accumulated error of s diameter and diameter of C between the reduced gradually, and finally tends to zero, thus realizing the Phi Phi c sand consistent, complete phase process.

The schematic diagram for:

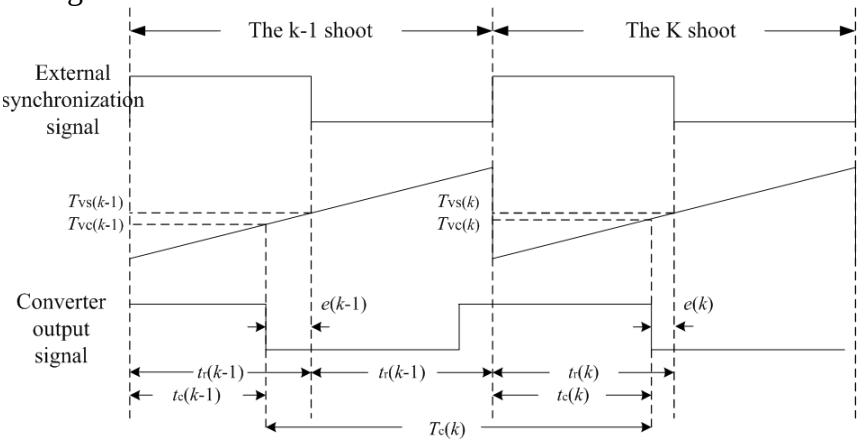

Fig. 1 Schematic diagram of PLL principle over zero

The realization process of zero phase locking can be represented by Figure 1, the Kshot refers to the K fundamental voltage cycle; tr (k), TC (k) vs and VC were expressedin the corresponding section K shoot jump along time; Tvs (k), Tvc (k) were tr (k), TC(k) count time Tcap; Tc (k+1) for the k film of VC updated the base period value.

Network voltage is sine power frequency alternating current. Output voltage of photovoltaic inverter is also sine power frequency alternating current. These two voltages are expressed by instantaneous value, as follows:

$$\begin{cases} u_s = U_{sm} \sin(2\pi f_s t \pm \theta) \\ u = U_m \sin 2\pi ft \end{cases} \tag{1}$$

In the formula: u_s is network voltage instantaneous value, U_{sm} is network voltage amplitude, f_s is network voltage frequency, θ is look-ahead or lagging phase angle, u is output voltage instantaneous value of photovoltaic inverter, U_m is output voltage amplitude of photovoltaic inverter and f is output voltage frequency of photovoltaic inverter.

If photovoltaic inverter wants to realize grid-connected electricity generation, it must make output voltage and network voltage of photovoltaic inverter have the same frequency and phase, while frequency and phase of network voltage should be changeless. It needs to adjust output voltage frequency of photovoltaic inverter to track network voltage, namely:

$$f = f_s \pm \frac{\theta}{2\pi t} \tag{2}$$

When network voltage look-ahead photovoltaic inverter phase is θ, it increases output voltage frequency of photovoltaic inverter to use for chase network voltage phase. When network voltage lagging photovoltaic inverter phase is θ, it reduces output voltage frequency of photovoltaic inverter to use for wait network voltage phase. After adjusting for a period of time, output voltage phase of photovoltaic inverter should be consistent with network voltage phase. Then it should conduct grid-connected operation.

Design and Implementation of Digital Phase Lock

Detection and Capture of Synchronizing Signal: Figure 2 is synchronizing signal detection and capture circuit. In order to realize tracking on frequency and phase, after voltage transformer, network voltage segregates, conducts differential detection and obtains u_{sdec} . Regulator potentiometer VR1 makes hysteresis comparison point voltage is zero and improves antijamming capability of positive zero-cross detection. Every voltage positive zero-cross point is rising edge jump point of hysteresis comparator’s output square wave. Hysteresis comparator output connects

to DSP’ s Capture unit. Initialized interrupt routine configuration is the rising edge trigger. When network voltage is normal, digital phase output tracking network voltage phase of photovoltaic inverter output voltage conducts genlock output.

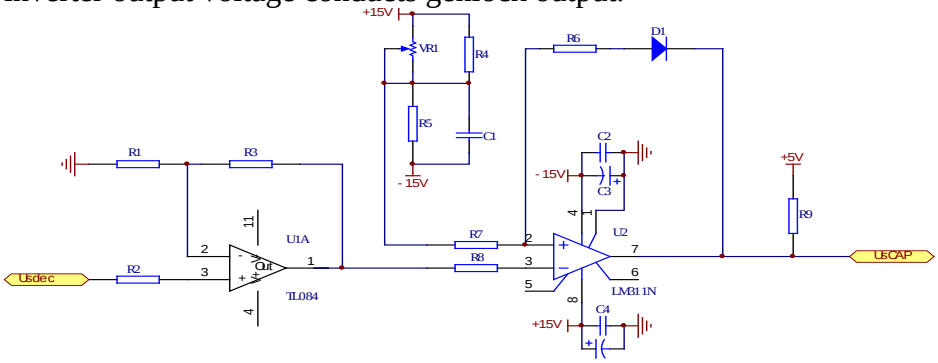

Figure 2 Synchronizing Signal Detection and Capture Signal

DSP to achieve zero phase lock step:

1 through the signal conditioning circuit will be vs by the sine wave signal is shaped into a square wave signal, square wave signal hop along the zero alignment and sinusoidal signals over;

2 the square wave signal into the DSP capture, when the DSP detects the effectivejump along appears, enter the capture interrupt. In the interrupt service program is first recorded values of counter current Tcap moment of the capturing unit plan, itsvalue by 2 as the diameter of S, and then Tcap reset (reset). Tcap uses a continuous increase in count mode;

3 in the EPWM interrupt service program performs the following operations:

Count 1 read Tcap in VC semi fundamental cycle time as the diameter of C,calculating the phase error;

The error of the line closed loop adjustment, output VC carrier cycle adjustment,adjustment calculation after the new carrier cycle value.

Digital Phase Lock Software Flow Pattern: The switching frequency selected by this experiment is 20 kHz. Therefore, in 20ms of a fundamental wave period of photovoltaic inverter output voltage, counts of VEC_NUM are 400. Network voltage period is about 20ms. Figure 3 is timer 2 period interruption subroutine flow chart and provides time base for calculating network voltage period. Figure 4 is to capture interruption subroutine flow chart. Its function is to calculate accurate network voltage period and provide accurate network voltage phase

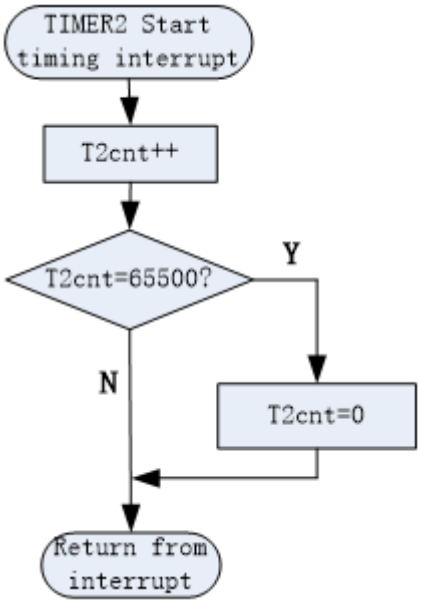

Figure 3 Timer 2 Period Interruption Subroutine Flow Chart

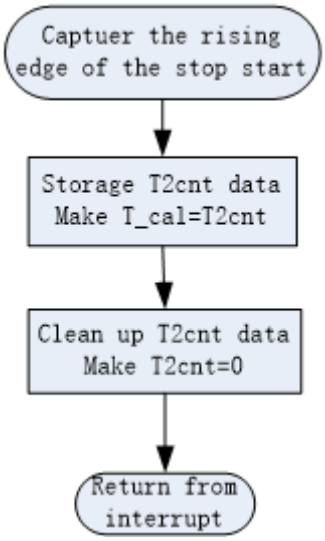

Figure 4 Capture Interruption Subroutine Flow Chart

Photovoltaic inverter output voltage phase is digital phase, while network voltage phase is practical phase. When VEC_NUM=200, namely digital phase $\phi = 180^{\circ}$, read current period count value of network voltage and obtain difference with the last network voltage period value, get phase difference between digital phase and practical phase. When deviation is in permissible range, it indicates that current digital phase has already traced practical phase correctly. Phase lock has already finished. When deviation is out of permissible range, it needs to conduct PI regulation on deviation and obtain regulating variable to change T1PR value, namely change frequency of photovoltaic inverter output voltage to trace network practical phase and finish phase lock through gradual regulation.

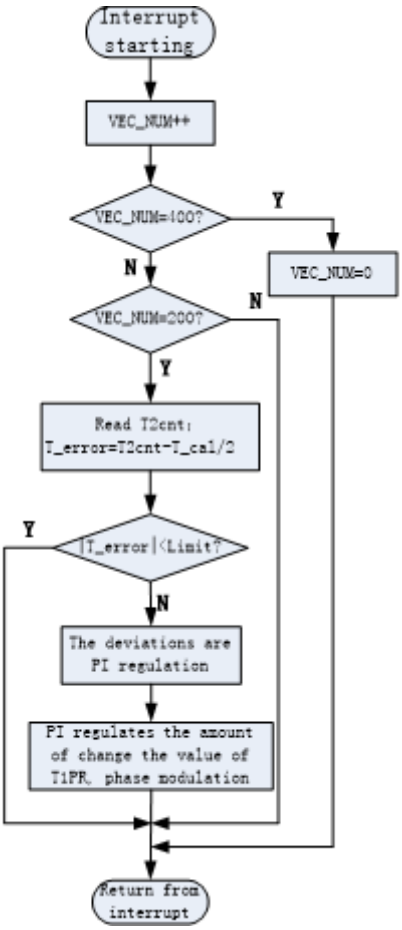

Figure 5 Underflow Interruption Phase Lock Parts of Subroutine Flow Chart

Experimental Results

Phase lock method of this paper has already used for single phase 3kW photovoltaic grid-connected inverter. Figure 6 gives out digital phase lock result. Alternating voltage is network voltage wave after being inspected by mutual inductor. Square wave signal is digital phase inspection signal wave after digital phase lock. It can be seen from the figure that it has high precision in phase lock and satisfies experiment requirements.

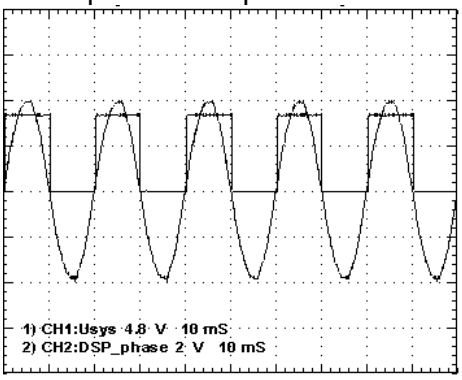

Figure 6 Digital Phase Lock Results

Conclusions

This paper studies DSP’s software phase lock technology based on TMS320F28010. Phase lock has high precision, is easy to realize can better satisfy phase lock technology requirements of photovoltaic grid connection. The experimental result verifies the feasibility and effectiveness of this method.

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