Design of Analysis Platform Used for Studying Soft Error Characteristic of 3D SRAM

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Keywords: Three-dimensional static random access memory (3D SRAM), soft error, analysis platform, cross section, single event upset (SEU), multi cell upset (MCU).

Abstract. This paper designs a novel 3D SRAM soft error analysis platform. It is used for studying the soft error characteristic of 3D SRAM stacked by multi dies and guiding the radiation hardened design for 3D SRAM. This platform integrates simulation tools including Geant4, TCAD and Nanosim, data recording and processing tools ROOT, layout processing tools Calibre, and Perl and Shell script used for linking task and analyzing results. After inputting the stacked structure, technology, circuit netlist and layout of 3D SRAM and incident particles information, this platform can simulate the particle striking 3D SRAM automatically, and then we get some kinds of cross sections, error information in a single word and sensitive node distribution for 3D SRAM. A 2 die stacked 3D SRAM based on 65nm CMOS technology is analyzed through this platform.

1. Introduction

Three-dimensional static random access memory (3D SRAM) based on 3D integrated circuit technology resolves the bottleneck faced by traditional SRAM, such as large-scale, high-bandwidth and high-speed memory access. However，3D SRAM also suffers the soft error induced by radiation. While 3D SRAM working in radiation environments, the radiation particles hit into 3D SRAM and produce single event effects (SEE), such as single event transient (SET) and single event upset (SEU), which are the main recourses for soft error [1][2]. With technology scaling, the multi cell upset (MCU) also induced by a single radiation particle make the soft error of SRAM more severely. Especially, the multi bit upset (MBU) happening in the same word makes the restraining soft error technology error-correcting codes (ECC) invalid [3].

Although 3D SRAM has multi stacked dies, it has been proved that incident particles can reach to each die and induce SET and SEU [4]. Because of the multi dies stacked structure, the SET and SEU producing and transfer becomes much complex in 3D SRAM. Thus, it is difficult to analyze the soft error and make the hardened design for 3D SRAM. In terms of resolving these problems, it is important to study the soft error characteristic of 3D SRAM.

Based on the conclusions about 3DIC radiation characteristic and radiation electronic response got before, we develop a novel 3D SRAM soft error analysis platform (3DSRAM-SEAP) using the industrial golden simulation methods and tools for analyzing the soft error characteristic and evaluating radiation sensitivity for 3D SRAM automatically, quickly and accurately. The results got form 3DSRAM-SEAP can guide the radiation hardened design for 3D SRAM.

2. 3DSRAM-SEAP Frame

To get the response of radiation particle striking, 3DSRAM-SEAP involves circuit netlist and layout information processing and analysis, 3D SRAM model establishment, striking particle information gained, excitation current source selection and extraction, simulation environment setup, circuit level striking simulation, data recording and processing and script generation. The integrated simulation tools include Geant4 based on Monte Carlo method, technology computer aided design (TCAD) used for SEE researching and Nanosim simulated circuit behavior. Calibre is used to get device coordinates from layout, and ROOT records and processes the data got in Geant4. The Perl and Shell script is compiled to link each tool and produce the final results characterized the

properties of soft error for 3D SRAM. The basic framework of 3DSRAM-SEAP is shown in Fig. 1.

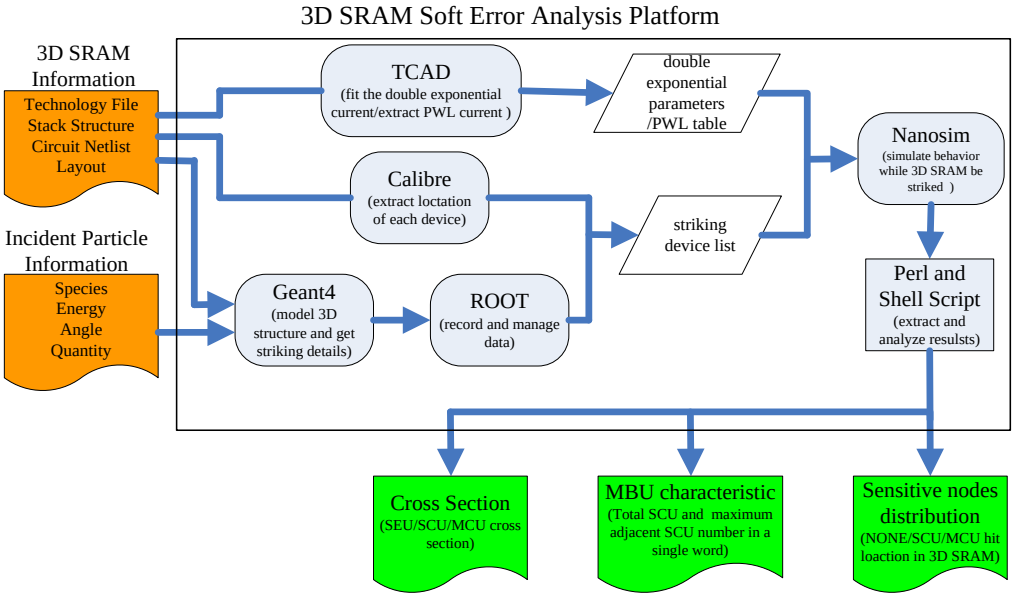


Fig. 1 Schematics of 3DSRAM-SEAP operational process from inputs to outputs.

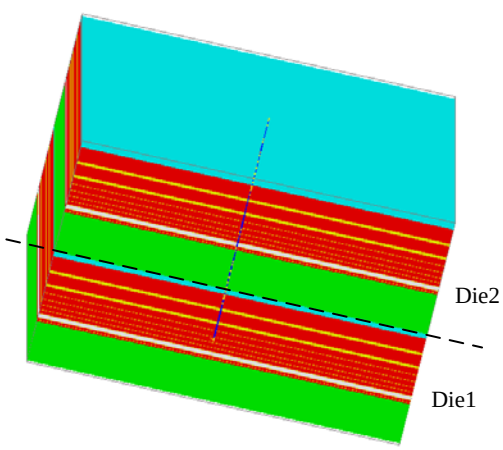
For approaching to the actual situation, a great deal of striking simulation is adopted. The location of striking particles in the device layer of 3D SRAM is got form Geant4 simulation. And the particle species, energy and angle are setup by users. All of these projects make 3DSRAM-SEAP close to real-time and accelerated testing methods.

3. Component Design and Link

3.1 Model Construction and Details Extraction

The compact model for 3D SRAM in Geant4 is constructed firstly according o the manufacturing technology and stacked structure of 3D SRAM input by users. In this sub-section, how to get hit details and collection of hit devices step is introduced via a 65nm 2 dies stacked 3D SRAM as an example.

The material and thickness for each layer of chip are extracted from the tech-file in process design kit (PDK). Based on this information the compact model of the 65nm two dies stacked 3D SRAM is constructed as shown in Fig. 2. In order to add the effect of secondary particles on soft error cross section of 3DIC, we change the material of one of the insulation layers from SiO2 to tungsten referring the method in [5]. The stacked mode is adopted as face-to-back in our 3D SRAM model as shown in Fig. 2.



Layer	Material	Thickness (um)
AP	Al	1.34
Si-Dioxide9	SiO_2	4
M9	Cu	0.78
Si-Dioxide8	SiO_2	3.07
M8	Cu	0.78
Si-Dioxide7	SiO_2	1.73
M7	Cu	0.14
Si-Dioxide6	SiO_2	1.68
M6	Cu	0.14
Si-Dioxide5	SiO_2	1.46
M5	Cu	0.14
Si-Dioxide4	SiO_2	1.23
M4	Cu	0.14
Si-Dioxide3	SiO_2	1
M3	Cu	0.14
Via-Tungsten	W	1
M2	Cu	0.14
Si-Dioxide2	SiO_2	0.54
M1	Cu	0.11
Si-Dioxide1	SiO_2	0.36
LET layer	SiO_2	0.01
SV	Si	1.2
substrate	Si	10

Fig. 2 Compact model of a 65nm two dies stacked 3D SRAM in Geant4 and description of each layer in it.

The inputs of Geant4 simulation are incident particle species, initial energy, incident angle and striking number. The list of the physical processes, which describes the reaction between particles and material, is based on the standard package of physics lists QGSP_BIC [6]. The data produced during simulations is recorded by ROOT. In Ref.[7], only while the distance between the device and the hit location is shorter than 2μm, the device can be effect by the deposited charge generated by incident particles. Thus, the influence radius in 3DSRAM-SEAP is set to 2μm.

3.2 Excitation Current Source Choice and Insertion

We choose circuit-level simulation as the simulation method. In circuit-level simulation, the transient current is inserted into the aimed device drain to simulate the device drain absorbing the deposited charge. We choose the piecewise linear (PWL) current as the transient current source. PWL current source is extracted from device drain current in TCAD device-level simulation. Comparing with the double exponential current source, PWL current source is more nearly to the actually. Due to the requirement of transient current with different device size and LET, a PWL current lookup table is established. The indexes of the lookup table are devices species and size and LET value.

3.3 Circuit-Level Behavioral Simulation

3DSRAM-SEAP uses circuit-level simulation tool Nanosim based SPICE for 3D SRAM behavior simulating. The speed of Nanosim is fast while keeping high-accurate. The inputs of Nanosim simulation are 3D SRAM netlist, the stroked device list and the transient current source. The netlist is provided by users, the stroked device list is given by the front part introduced in 3.1 section, and the transient current source is selected form one of the double exponential current source and PWL current source. During the Nanosim simulation, the transient current sources are inserted into the stroked device drain at the hit time.

According to the test scheme in real-time testing and accelerated testing, the radiation test in 3DSRAM-SEAP includes static test and dynamic test. Furthermore, static test is divided into All-0 test and All-1 test. The users can selected any test scheme in 3DSRAM-SEAP. The test inspires are compiled due to the test schemes, and the accurate results for these test inspires are recorded at once. At the beginning of each Nanosim simulation, the test inspires and the transient current sources are loaded into the simulation. During each simulation, the outputs of 3D SRAM are compared with the accurate results automatically. If there is difference between the real time outputs and recorded accurate results, it means a soft error occurs. Nanosim records this soft error information into sim.err file. While a simulation is completed, the soft error characteristic of 3D SRAM will be studied via analyzing the sim.err file.

3.4 Evaluation System Establishment

- cross section

The cross section includes the total cross section, SCU cross section and MCU cross section. The cross section is calculated by Eq.(1):

$$\sigma = \frac{N_1}{N} \times S \tag{1}$$

where σ is the cross section, N is the total number of particle striking, N_1 is the number of upsets, and S is the surface are of SRAMs. The upset number for each particle striking simulation is extracted from sim.err file, upset does not occur while upset number is 0, SCU is happened while the upset number is 1, and MCU is occurred while upset umber is more than 1. Finally, various kinds of cross section are obtained by analyzing the statistical simulation results for N times.

- maximum number of SCU in a single word (MTNS)

MTNS means the largest total number of upset in a word among all words. It is used for evaluating MBU. The larger MTNS makes MBU more serious. Thus, it is difficult to hardened 3D SRAM by using ECC technology while MTNS is large. MTNS is also got from sim.err file.

- maximum number of adjacent SCU in a single word (MTNAS)

MTNAS is another object to evaluate MBU characteristic of 3D SRAM. While correcting more than 1 error in a word, the data of adjacent bit needs to cooperate in ECC technology. Thus, the adjacent SCUs in a word make ECC design much difficulty and needs much redundancy circuit to detect and correct errors. The gained of MTNAS is the same to MTNS.

- sensitive location distribution

The sensitive location distribution is the position muster of the hit locations induced soft error. The most sensitive part of 3D SRAM can be found from the sensitive location distribution. Making significant attention on the most sensitive position may increase the hardened effect for 3D SRAM easily. In 3DSRAM-SEAP, each particle striking event is set a serial number and its location is recorded. If the upset number of the particle striking event is not zero, its hit location is lookup by serial number and marked at the 3D SRAM layout.

After ensuring the evaluation system for 3DSRAM-SEAP, the Perl and Shell scripts are written to extract the information from sim.err file, and then these data are processed also by scripts to get each object of evaluation system given above.

4. Results Evaluation

In this work, 3DSRAM-SEAP is used to analyze the soft error characteristic for a 3D SRAM based on 65nm CMOS technology. 3D SRAM is stacked by two dies generated by cutting 2D SRAM, which is generated by Memory Compiler with the size 256words×16bits, in the center. TSV array used for signal connecting is inserted at the edge of the die. Since, the TSV region can not be effected by particles, the efficiency area of 3D SRAM is 95.59μm×82.39μm. The memory array is divided into 4 banks, and two of them are put into the top die and the others are put into the bottom die.

The setups of 3DSRAM-SEAP in this work are as follows: Kr ion (Z is 36 and mass is 84) is closed for incident particles; the incident direction is vertical to the surface of chip; the test scheme is static test including All-0 and All-1; the number of particles striking simulations is 6000.

Table. 1 Cross section got from 3DSRAM-SEAP.

All-0 Pattern			**All-1 Pattern**		
Total cross-section （cm^2/bit）	**SCU cross-section（cm^2/bit）**	**MCU cross-section（cm^2/bit）**	**Total cross-section（cm^2/bit）**	**SCU cross-section（cm^2/bit）**	**MCU cross-section（cm^2/bit）**
2.59E-7	2.58E-7	2.56E-7	2.58E-7	2.69E-7	2.56E-7

Table. 1 gives the cross section for 3D SRAM. Due to the data processing of ROOT, LET value for the incident particles in device layer is about 40MeV •cm2/mg. As shown, SCU cross section is less than MCU cross section. It is because the influence radius of particle striking is set by 2μm, which may trigger MCU. It will be observed more clearly while giving the sensitive nodes distribution.

Table. 2 MTNS and MTNAS got from 3DSRAM-SEAP.

All-0 Pattern		**All-1 Pattern**	
MTNS	**MTNS**	**MTNAS**	**MTNAS**
4	4	4	4

Table. 2 gives the evaluation factors MTNS and MTNAS for 3D SRAM from 3DSRAM-SEAP under static scheme. There may be 4 SCUs occurring in a word, and 4 SCUs may be adjacent. Although the 4bit intercrossing technology is used, MBU can also happen. Moreover, it seems that MBU in 3D SRAM is more difficulty to be hardened by ECC technology. The reason for these is that the 8 high-bits and 8 low-bits in a word locate at die1 and die2, respectively, and they are in the same vertically direction. And the SCU may happen at 8 high-bit and 8 low-bit at the same time.

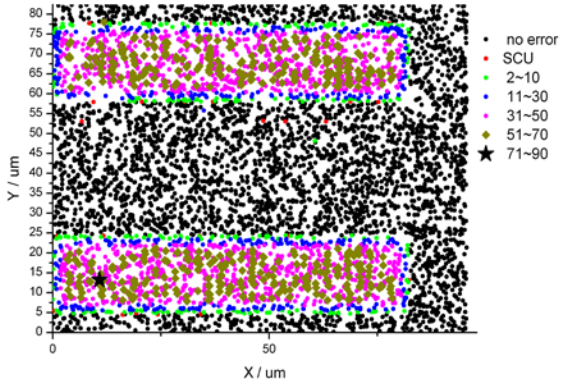


Fig. 3 Sensitive node distributions for 3D SRAM in All-0 pattern.

Fig. 3 gives the sensitive node distributions under different conditions. The color of point in the distribution denotes the number of induced SCU. The sensitive nodes concentrate on memory array. It indicates that only the SRAM cells are the radiation sensitive, and the combination-logic circuits do not induce soft error under static test. Since the particles striking combination-logic only induces SET but not SEU, and SET can not transmit to induce soft error. There are also some sensitive nodes locating in the combination-logic circuit. Via checking the simulation result details, we find there are two reasons resulted in these points: (1) the incident particles hit the combination-logic circuit of die1, and then it deflects a lot due to colliding with materials and enters into memory array to trigger SCU; (2) the secondary particles generated by nuclear reaction between active particles and materials hit the memory array and induce SCU while active particles hit the combination-logic circuit.

5. Conclusion

This paper constructs a novel 3D SRAM soft error analysis platform (3DSRAM-SEAP) based on the stacked structure of 3D SRAM. 3DSRAM-SEAP simulates incident particles striking 3D SRAM abundantly to get the soft error characteristic of 3D SRAM, and its analyzed results can guide the radiation hardened design for 3D SRAM. 3DSRAM-SEAP integrates Geant4, ROOT, Nanosim tools to simulate and deal with data and Perl and Shell script to join tasks together.

Using 3DSRAM-SEAP, we analyze the soft error characteristic of a 2 die stacked 3D SRAM based on 65nm CMOS technology. The cross section, MTNS, MTNAS and sensitive node distribute are got. It found that 3D SRAM is difficulty hardened by ECC technology. In static test scheme, the sensitive nodes only distribute in the memory array of 3D SRAM. It indicates that only the SRAM cells is radiation sensitive in static mode.

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