A Precise Model of TSV Parasitic Capacitance Considering Temperature for 3D IC

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Abstract. As the technology of three dimension integrated circuit (3D IC) develop quickly, through silicon via (TSV) plays a basic and important role.In consideration of real working environment, factors as temperature and working voltage are studied by TCAD simulator. And the contribution of physical sizes and the concentration of doping in the course are analyzed. A new analysis model of capacitance for TSV is given, which is with an error less than 4% with the measurement data. In the range of 25 to 125 degree centigrade with different physical sizes of TSV, this model of TSV's parasitic capacitance shows a better accuracy and takes less time than the former one. The neglect of temperature in course of design will lead to a big problem in real chip, an accurate mode considering temperature is important both in design and SI analysis.

Introduction

According to the law of Moore, the technology size of traditional chips grows smaller and the scale of chips increases. However the physical limits restrict the reduction of transistor size [1]. And there are problems of delay, power and parasitic effects as technology develops. Instead of transistors, interconnect issues become the major factors which determine the performance of integrated circuits [2]. 3D IC is an effective way to solve these problems where TSV is used as vertical interconnections. However TSV introduces a large and fickle parasitic capacitance inevitably. It can cause coupling noise and extra transmission delay and so on. The parasitic capacitance of TSV is a key point in its model [3]. In considering of the actual working environment of TSV, temperature cannot be ignored.

Based on TCAD simulator [4], the parameters of single TSV model are extracted and verified by measurement data. There are analysis on parasitic capacitance at different temperature considering of radius, length, and thickness of TSV oxide. The rules between temperature and related factors are list. An analytic formula of parasitic capacitance of TSV is formed considering temperature and is validated by data of measurement.

Parasitic capacitance of TSV

The parameter of TSVs on a chip is always the same, of which the number can reach thousands to hundreds of thousands. And TSV is a basic element which is used repeatedly to form arrays [5]. An accuracy model of TSV is significance for design works.

Factors effecting of parasitic capacitance of TSV

Depletion capacitance of parasitic capacitance is easily influenced by temperature. And with reduction of the size of TSV, this tend to be more apparent. Based on measurement data the minimum parasitic capacitance has a variation of 15.3% from 298K to 398K. The concentration of substrate doping also has an influence on it. Through TCAD simulation the minimum parasitic capacitance has a variation of 62.3% from 2×10^{15} cm-3 to 1.7×10^{16} cm-3.TSV for test and simulation use the parameters as follows, with diameter of 5um, the thickness of oxide layer of 0.12um, the length of 20um. The temperature in default is 298K and the concentration of substrate doping is 2×10^{15} cm-3 which is an N type substrate.
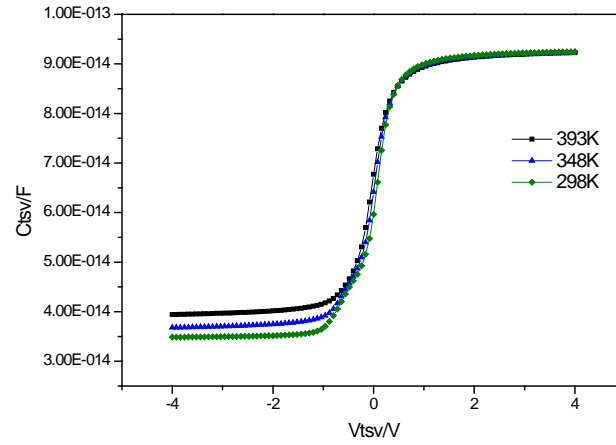
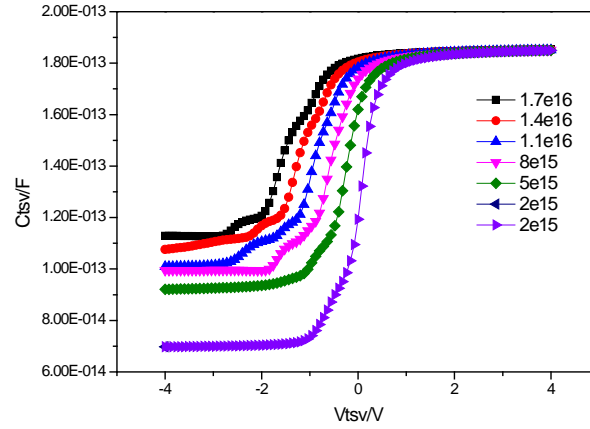Fig. 1. Simulated TSV C-V characteristics at different temperatures

Fig. 2. Simulated TSV C-V characteristics at different concentration of substrate doping

Parasitic capacitance of TSV at different temperatures is shown in figure 1 by TCAD simulation. With increasing temperature, the capacitance of oxide layer in accumulated phase and the flat band voltage remain unchanged. And the minimum capacitance of capacitance increases with the temperature. As temperature increases, the growth rate of depletion capacitance increases. The minimum parasitic capacitance changes 10.89% from 273K to 373K. As temperature changes, the intrinsic carrier concentration and thermal voltage changes which lead a change in the maximum width of the depletion. From figure 2 it can be find that as the concentration of substrate doping increase, the depletion capacitance tend to increase as the flat band voltage shift to the right.
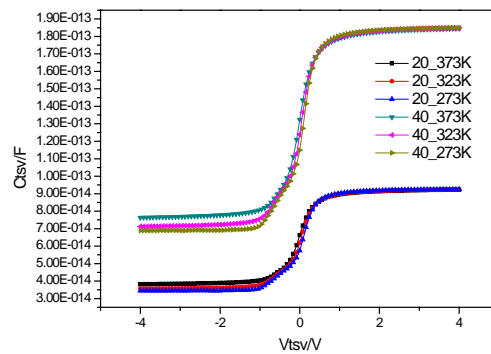

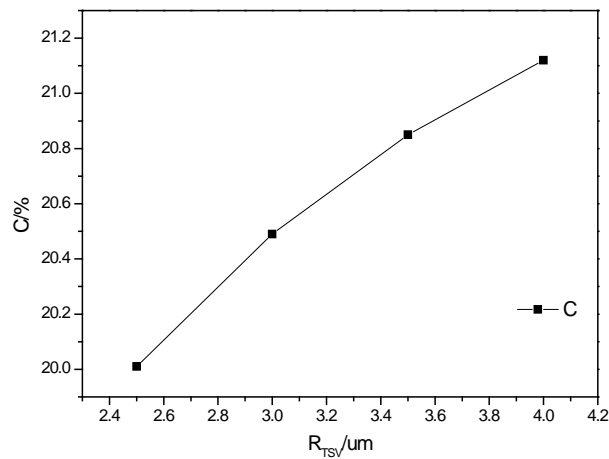Fig. 3. Simulated TSV C-V characteristics of different length

Fig. 4. Variation of TSV capacitance of different radius

The effect of temperature on the parasitic capacitance is also influenced by the physical dimensions of TSV. By keeping the other dimensions constant, change the lengths of TSV. Test the minimum capacitance of TSV from 273K to 393K, when the length is set to 20um to 40um. As shown in figure 3, the data are in a linear relationship. Use a similar method to study other parameters. Figure 4 shows the relationship between radius of TSV and parasitic capacitance of TSV with temperature changes. As the radius of TSV gradually increase, the minimum parasitic capacitance change more when temperature changes. But the lifting speed slow down. Figure 5 shows the study of oxide thickness. With an increase in oxide thickness of TSV, the parasitic capacitance of TSV change with temperature becomes smaller.

With the development of three-dimensional integrated circuit technology, TSV will be smaller both in radius or length and so on. With the capacitance of TSV changes 1%. On the other hand as the thickness of oxide layer of TSV enlarge 4 times, the minimum capacitance will change 13%. Form above it is obvious that the impact of radius is less than the thickness of oxide layers of TSV on depletion capacitance. And the minimum capacitance of TSV variation with temperature increases apparent as the technology of TSV develops.
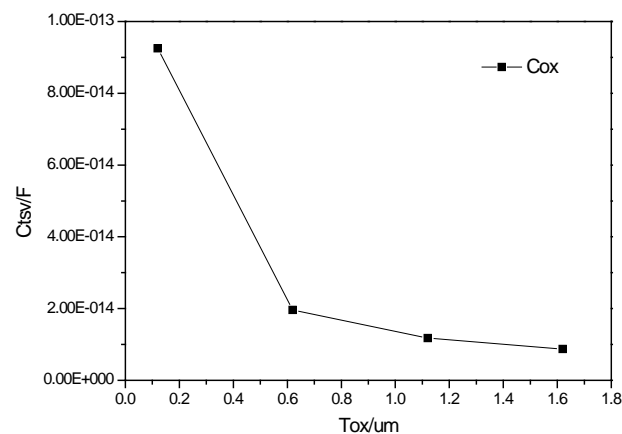

Fig. 5. Variation of TSV capacitance of different oxide thicknesschange of TSV radius of 60%, the minimum

TABLE 1.   COMPARISON BETWEEN SIMULATION AND ANALYTIC MODELS

D_{TSV} (um)	T_{OX} (um)	L_{TSV} (um)	N_A (cm^{-3})	C_{min}(fF) Simulated	C_{min} (fF) Former Analytic	Deviation (%)	C_{min} (fF) New Analytic	Deviation (%)
5	0.12	40	4e15	85.71	87.34	1.9	85.92	0.2
5	0.12	40	1.7e16	112.83	115.47	2.3	114.56	1.5
5	0.12	20	2e15	35.86	37.23	3.8	36.33	1.3
2	60	10	4e15	12.3	12.43	1.1	12.11	1.5
2	60	10	1.7e16	17.1	17.46	2.1	17.28	1.1

A. *Analytical model of the parasitic capacitance of TSV*

The parasitic capacitance of TSV mainly contain two parts which are the capacitance of oxide layer and depletion layer. When there is a depletion layer, the two capacitances are in series that can be regarded as the total capacitance of TSV. The capacitance of oxide layer is relatively fixed with little change of environment factors. The capacitance of depletion layer can be got by using one-dimensional Poisson equation. The largest width of the depletion can be got through Poisson equation and boundary conditions. Because the equation cannot be solve directly. Iterative approach is needed to solve the problem. As a consequence it usually takes a long time to analysis a large scale of TSV array. Here change the formula of depletion width with Eq. (1). Use Cartesian coordinate system instead of spherical coordinate system. Eq. (2) can be solve directly which reduced the computational difficulty and its deviations is in a tolerate range.

TABLE 2.   COMPARISON BETWEEN MEASUREMENT AND ANALYTIC MODELS

Temperature °C/K	C_{min} (fF) Measured	C_{min} (fF) Former Analytic	Deviation (%)	C_{min} (fF) New Analytic	Deviation (%)
25/298	60.009	60.499	0.81	59.91	0.16
50/323	60.303	61.698	2.31	61.25	1.5
75/358	61.210	62.961	2.86	62.76	2.5
100/373	63.774	65.187	2.21	64.48	1.1
125/398	69.229	67.12	3.04	66.46	3.9

$$\frac{\partial}{\partial x}\left(\frac{\partial \psi(x)}{\partial x}\right) = \frac{-qN_A}{\varepsilon_{si}} \qquad (1)$$

$$w_{dep} = \sqrt{\frac{4\varepsilon_{si}V_t \ln\left(\frac{N_A}{n_i}\right)}{qN_A}} (2)$$

As can be seen from the formula, the width of maximum depletion layer is related with the concentration of intrinsic carrier and substrate doping, the thermal voltage and other factors. The concentration of intrinsic carrier is controlled by temperature and the thermal voltage varies linearly with temperature. When temperature is higher than 250K, the relationship between the concentration of intrinsic relationship and temperature can be described as Eq. (3) [6]. And the thermal voltage line with Eq. (4).

$$n_i = C_1 T^{\frac{3}{2}} e^{\left(\frac{-Eg}{2kT}\right)} (3)$$

$$V_t = \frac{kT}{q} (4)$$

$$C_{dep} = \frac{2\pi\varepsilon_{si}l_{tsv}}{\ln\left(\frac{R_{metal}+t_{ox}+w_{dep}}{R_{metal}+t_{ox}}\right)} (5)$$

The width of depletion layer can be got from Eq. (2) using Eq. (3) and Eq. (4). Then use Eq. (5)

to obtain the capacitance of depletion layer in different temperature. According to the TCAD simulation, the variation of the capacitance of oxide is small, and the depletion capacitance changes with temperature more obviously. Based on the two capacitance, the minimum capacitance can be calculated. The modeling environment of TSV before is nearly ideal, some parameters directly use constant which ignore the variation caused by temperature. That approach put all of TSV in 3D IC on the equal sign, no matter which layer TSVs are or whether there is hotspot. Analysis design using former model will ignore some error.

Compare the minimum capacitance at room temperature using the former model and the new model. Data are shown in figure 1. The new model of TSV capacitance is more accurate and the solving time is shorter. The former one not only ignore the factor of temperature, but also is less accurate in fixed temperature.

Ref. [6] also consider the effect of temperature on TSV parasitic capacitance. Based on the measurement data from Ref. [6] here, compare the two models with the measurement data. the model here is more accurate. This new model of TSV parasitic capacitance can be used in large-scale analysis of TSV arrays which is accurate and rapid.

Conclusion

Based on TCAD simulator, an analysis is made about the parasitic capacitance of TSV and related factors. Temperature and working voltage have an obvious influence on the parasitic capacitance. And different size of TSV differs from each other. In view of that, anovel precise model of parasitic capacitance of TSV is given and verified with data of simulation and measure. It helps to establish analysis flow in EDA tools used in design or SI analysis.

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