ARINC - 429 airborne communications transceiver system based on FPGA implementation

Liu Hao[1]，Gu Cao[2] ,MA Shi-guo[3], Li Xin[1] , He Gang[1,4]

[1]Naval Arm Academy, Shanghai, 200436

[2]Air Force Command College, Beijing 100089

[3]Unit 91445, Dalian Liaolin, 116043

[4]Unit 91230, Fu'zhou Fujian，350000

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Abstract. High performance integrated circuits are increasingly used in the aviation equipment. Airborne equipment to solve the data transmission, airborne equipment and the ARINC-429 bus is based on PC/104 bus standard problem of communication between the microprocessor, and designs a scheme, using the FPGA's high-speed, flexibility to control the HI-8582 chip, to realize the real-time receiving and sending of ARINC-429 bus, the control system adopts industrial computer PC104 transceiver channel, sending number, baud rate and other parameters, and real-time display to send and receive information, realize the human-computer interaction. The FPGA control is applied to save the hardware resources effectively, has fast processing speed, strong anti-interference ability, low cost, etc.

Introduction

With the ultra large scale integrated circuit technology leap development, integrated avionics, integrated more and more high. Data bus for fast, efficient equipment, reliable data transmission has irreplaceable function. ARINC-429 bus is a joint Aeronautical Radio Incorporation set up by the America aviation electronic equipment manufacturers, scheduled airlines, aircraft manufacturers and other national airline, developed by the company of a series of unified industry standards and specifications of [1-2]. PC/104 embedded system with low power consumption, small volume, wide working temperature range, high reliability and outstanding advantages of [3-5]. Early implementation of ARINC-429 data transmission method generally uses the MCU control [6-8] system, but there exist low communication speed, timing control deficiencies is not flexible enough, not suitable for ARINC-429 high-speed communication.

FPGA (Filed Programmable Gate Array, field programmable gate array) has the advantages of high work frequency, the advantages of parallel processing data. The disadvantage of the traditional methods based on, this paper uses FPGA as the timing and decoding control chip, using 16 bit data bus, the chip ARINC429, HI-8582 bus, so that the transmission rate of airborne communication equipment to achieve high data rate 100kbit/s.

The basic idea and framework

Airborne communication system is mainly composed of the following three parts: the human-machine interactive part, data processing part, the underlying link transmission part of airborne equipment. The three part between the relatively independent, each section independently to complete each function, data transmission through the corresponding interface, the system has one one integral whole, work together to complete the data communication of airborne equipment.

Work system, is divided into two processes: the process of sending data and receiving data process. When sending data when the sender of information through the system, man-machine system will need to send the data information is sent to PC104, PC104 will convert the information into a data format in accordance with HI-8582 data form, and the address information and data information is also written to the FPGA internal memory, FPGA after receiving the message, using

the first in first on the order of 32 bits of data are written in two chip HI-8582, in the FPGA control unit for configuring HI-8582 to start the two receivers within HI-8582, sends out the data; when the system receiving the data, serial data from airborne equipment to transmit the flow inside the chip serial data are combined into 32 the bits of the data word, and stored in the internal FIFO, when the FIFO has data, the external pin data ready flag DR is set to a low level, at the same time interrupt trigger signal external microprocessor, the microprocessor to control HI-8582 chip corresponding signal pin line, transmits the data to the FPGA internal memory, and then data transfer to PC104. Through the above two processes, the process of exchange system can orderly completion of PC and airborne equipment data.

Composed of FPGA and HI-8582 of the ARINC-429 airborne communication system module

Using top-down design (Top-Down) in the forward design technical route [9-11], FPGA needs to complete the PC104 bus to read and write timing control, address decoding, data transmission and other functions, at the same time, also need to control receives two ARINC429 special chip and a way to send, so that various data exchange orderly flow. Therefore, FPGA bus interface control logic is mainly divided into two function modules: one is to control the PC104 bus to read and write the logic, control the ARINC429 chip two is sending and receiving logic. This design adopts XILINX company Spartan3A series devices of XC3S200A as the main control chip.

PC104 read and write control module.This module is mainly used for PC104 bus data storage and read. The corresponding read-write control signal generated by FPGA, the width of the data bus is 16 bits, address line width is 20 bits, memory address unit used in the internal distribution of D0000-DFFFF, 64K storage. In the process of reading data, in order to make the data synchronization and address sequence, using the same clock edge trigger, FPGA control logic will cache the data and address and sent to the PC104 bus; in the write data process, in the same clock edge trigger, data and address information at the same time into the FPGA internal cache. The read and write timing as shown in figure 1.

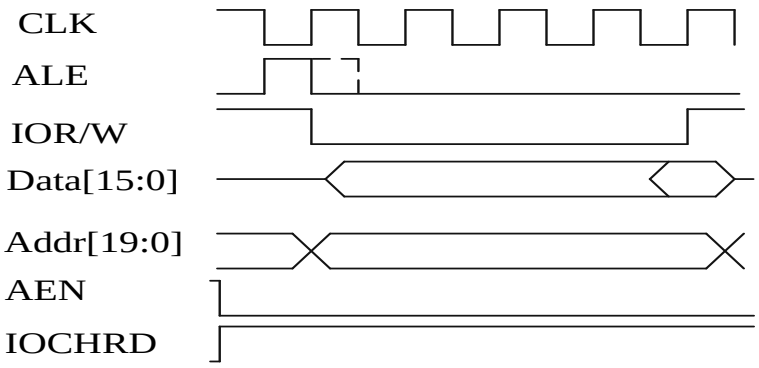

Figure 1 PC/104 bus read and write timing

ARINC429 transmit / receive control module.ARINC429 bus communication specification is designed for the air transport industry standard between avionics transmission of digital information and the development of the transport protocol, is a kind of point to point, bus consists of two differential signal circuit [12]. A total of 32 bit data words of bit ARINC429 specification, the composition of each data word is composed of 5 parts: the flag (Label the 1-8), the source / target identification code (SDI the 9-10), the data area (Data eleventh - 29), symbol / status bit (SSM the 30-31), parity bit (Parity thirty-second). Consisting of 32 bit data words in the form of pulse through the STP serial transmission, and using the bipolar zero debug mode.

The design used in the 429 communication chip HI-8582 for a 16 bit interface chip, the chip has two receivers and one transmitter, each receiver and transmitter has a 32 x 32 FIFO buffer, during data transmission, can register to detect the three FIFO via an external pin or state, when there is data, interrupt processing data in the cache trigger external microprocessor. The HI-8582 chip two receivers and one transmitter can work independently, but share a 16 bit data path, in order to make the two receivers and one transmitter HI-8582 coordinate work orderly, finite state machine is

adopted in the design of [3-5] (Finite State Machine, FSM) design method, FPGA devices by XC3S200A chip control work.

A state machine consists of,,, and a total of five states, respectively, said wait state, the sending state, the receiver 1 working state, the receiver 2 working state and all kinds of position signal clear status. After system reset enter wait state, on each rising edge of the clock arrived, send interface logic module to query the HI-8582 pin of the sign bit, data ready flag and the half full flag, when the effective, then enter the job ready state, according to the sign bit, into the corresponding sending / receiving state, when the data transmission / receive after the treatment, then enter the state, the position signal restoration, the address, data and enable signal reset. Fig. 2 Schematic shown in Figure state transition:

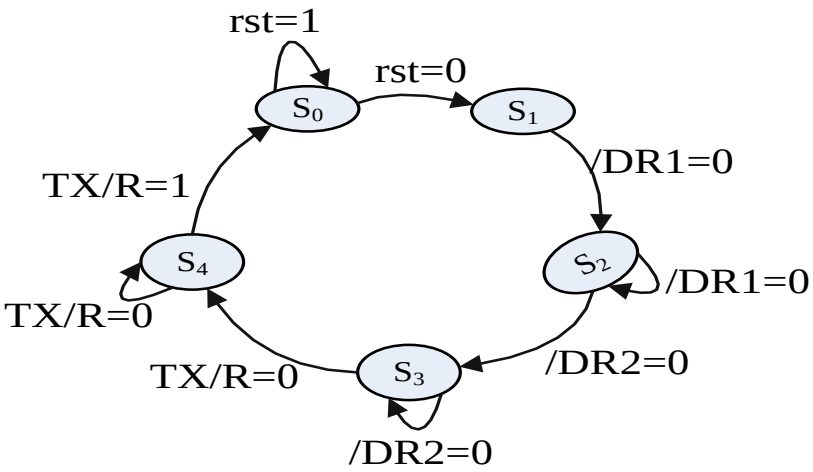

Figure 2 state transition diagram

interrupt processing.Take appropriate interrupt processing mode and strategies have an important role to complete the reliable transmission of [13] 429 data. Because of the communication system, in addition to receiving 429 microprocessor system bus data process, also need to process the video signal another expansion board, and interrupt priority video signals must be high, therefore the microprocessor in the interrupt subroutine process 429 bus, may at any time may be video signal interrupt subroutine interrupt execution process 429, will cause the interruption of bus data transmission.

Since microprocessor response is positive edge triggered interrupt mode, the interrupt signal and the 429 special chip for signal generated from the 8582 level, namely the cache data, data ready signal is set to a low level, has been maintained until the cache is empty post is high, therefore, the direct application of the data signal as interrupt sources, when PC interrupt response subroutine video signal is high priority interrupt subroutine interrupt, when the processor is idle, not again in response to the 429 bus generated interrupt response signal, so the design of the scheme is that when the 429 bus data processing required, in each interrupt source signals effectively in the process of generating a pulse signal from inside FPGA and by the pulse trigger processor interrupt response subroutine, so that the processor can effectively at the same time for processing the video signal and the 429 data bus.

Simulation test

The system uses ModelSim6.5b simulation tool to verify the FPGA design. The overall design of the structure of FPGA kernel, mainly includes the following modules:

1) PC/104 bus decoding module: FPGA received from the host computer through the PC/104 bus to instruction, and decodes them, generates corresponding control command, coordination of each module at the same time, to make it orderly work;

2) the data send / receive control module: mainly used to control the ARINC429 chip to read and write operations, data transmission is responsible for the completion of the underlying link. This design adopts the design method of finite state machine, the HI-8582 two receivers and one

transmitter shared a 16 bit channel orderly completion of data transmission / reception work, its state transition simulation figure 3 as shown in fig.;

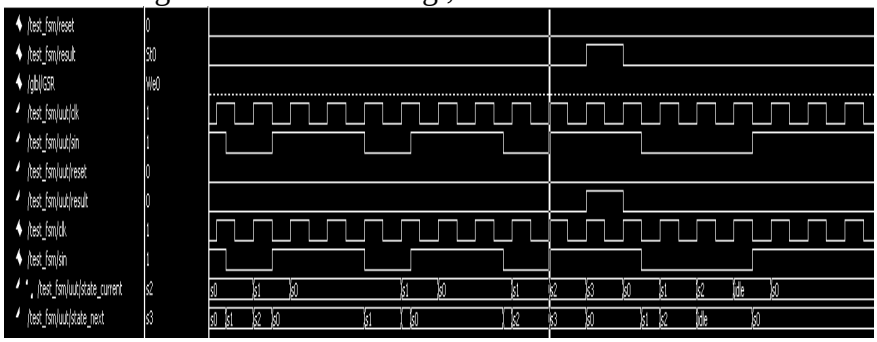

Figure 3 finite state machine state transition simulation map

3) interrupt processing control module: for external interrupt trigger microprocessor, interrupt processing simulation as shown in figure 4. Because the HI-8582 given the data ready flag to level signal effective signal and micro processing the response to the rising edge triggered, so need to deal with;

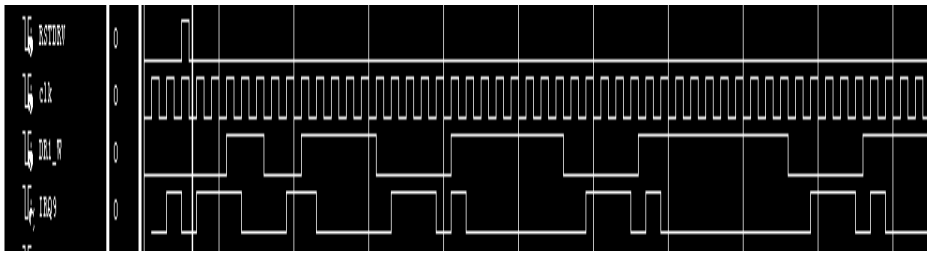

Figure4 interrupt processing simulation

Conclusion

In this paper, from the design requirements of airborne products are stable and reliable, high degree of integration of the starting, and adopt XILINX company Spartan3A series FPGA devices, XC3S200A combines the high performance ARINC429 chip HI-8582, and with the periphery of the level conversion circuit, the design and implementation of ARINC429 interface module based on PC/104, this module supports various ways of working, less components, high reliability. At present, the entire ARINC429 airborne communication system has been applied to one type of machine, the actual work in the use of that, the design of the working performance of the communication system is stable, the reliability is good.

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