Chaotic Signal Generator Design Based on Discrete System

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Abstract. This paper presents an implementation of a chaotic signal generator based on digital processing for three dimension system. A detailed description of the structure and function of each module design are presented, by comparing the experimental results and simulation results verify the feasibility of this method. The proposed chaotic signal generator offers a new alternative in random testing system or in secured data communication applications.

Introduction

Chaotic signal has been used in many fields for its characteristics of pseudo random and noise[1-4]. Chaotic signals are generated by the differential dynamic systems[5-7]. Because of the affect of component parameters which are used to establish the dynamic analog systems, it is difficult to achieve the desired chaotic signals. With the development of the modern digital signal processor, the speed of numerical calculation is increasing. It is possible to simulate the motion of differential dynamic system by using discrete system[8], and finally acquire the chaotic signals. By means of this method, the design process of chaotic system is simplified, and the overall volume and total effective cost of the system can be reduced. Meanwhile, the reliability of the system is improved. If the simulation algorithm is designed properly, this method could generate all types of chaotic signals needed in different chaotic system. At the same time, it is easy to make sure the parameters of chaotic model in digital system which is very important for chaotic synchronization. This paper describes a method of generating chaotic signal by digital system..

Digital Chaotic System Realization

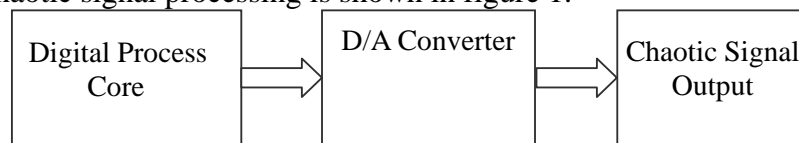The overall chaotic signal processing is shown in figure 1.

Fig.1 chaotic signal processing flow

In this method, the differential dynamic equations are replaced by discrete difference equations in order to obtain the digital computing core. Take the Rössler three-dimension model as an example[4], the formula is as follows:

$$\begin{cases} \dot{\mu} = -v - \omega \\ \dot{v} = \mu + av + 0.1\mu\ln(\omega) \\ \dot{\omega} = c + \omega(\mu - b) \end{cases} \tag{1}$$

When The differential dynamic equations are transformed into discrete difference equations, the rule of equation discretization is using the forward difference quotient to replace the derivative, By solving the differential equation to calculate the numerical solutions of discrete nodes, the numerical solutions are not equal to the solution of differential equations

or the formula, but give approximate values at each discrete node of the simulation process, this algorithm is more suitable for digital signal processing. The numerical solutions are calculated by using two order Runge-Kutta method shown in equations(2) which gives more exact solutions of the difference equations.

$$\begin{cases} y_{i+1} = y_i + h*(K1+K2)/2 \\ K1 = f\left(x_i, y_i\right) \\ K2 = f\left(x_i + h, y_i + h*K1\right) \end{cases} \tag{2}$$

So the new discrete difference equations are shown as follows:

$$\begin{cases} \mu_{k+1} = \mu_k + (-v-w)(h+1/2\,h^2) \\ v_{k+1} = v_k + Kv + h/2(u+Kv)\ln\left[\omega+Kv\right] \\ w_{k+1} = w_k + +Kw + h/2\left[c+\left(w+Kw\right)\left(\mu+Kw-b\right)\right] \\ Kv = h/2\left[u+av+1/10\mu\ln w\right] \\ Kw = h/2\left[c+w(\mu-b)\right] \end{cases} \tag{3}$$

where μ, v and w are three chaotic signals, a, b and c are constants, k is the number of iterations, h is step length, we can adjust the step length h to change The variation rate of discrete chaotic signal, the smaller of the step length, the more of discrete sampling points, the precision of simulation is more precise, however the costs are more iterative times, large amount of calculation.

The equation (3) difference equations are divided into different modules when operation. The chaotic differential equation is analyzed to find the required operation types in this design. We need to carry on the functional design of the digital logic circuit of the operation type, then to perform the simulation for each module, to ensure that it reaches the expected design goal, finally to deal with the timing design of the digital circuit.

(a) Diagram of variable μ

(b) Diagram of variable v
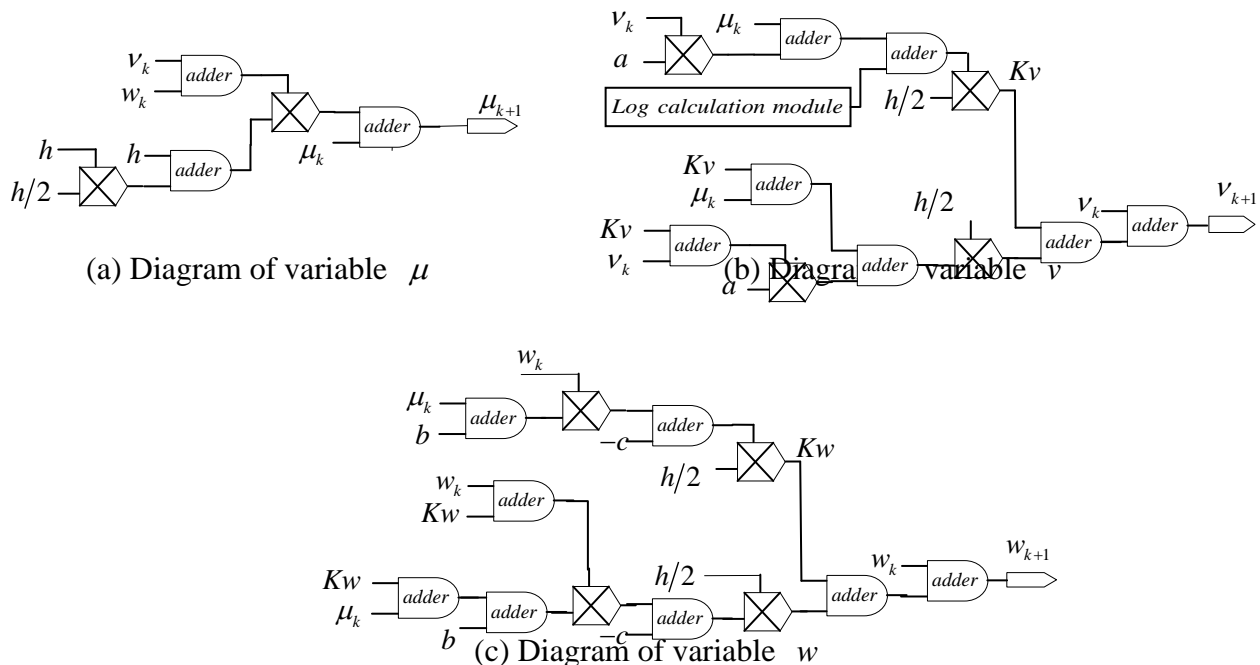
(c) Diagram of variable w

Fig.2 Electric circuit structure diagram

Due to the use of the iterative solution of the differential equation algorithm, the input state variables of each step are influenced by the output state variables of the previous step. While the path complexity of three signals are not the same, and the calculation time delay of each module are not the same, we need to design a sequential circuit to control the calculation time and hold time of each step for the whole computing time.

According to the equations (3), we can give structure diagram of arithmetic operations as shown in figure 2. Each diagram shows the calculation process of a variable in the difference equations (3). We can find out that three kinds of modules are needed to use, such as adder module, multiplier module, logarithmic module. For logarithmic operation is difficult to realize in digital processor, it is replaced with a look-up table structure in the design. Before constructing all the modules, the data width is fixed as 20 bit, where bit 20, '1' or '0' means that negative or positive, and bit 19 to 7 represent the integer part, the others represent the decimal part of a real number , then we can describe the module by using digital logic circuit.

Test results

The device used in hardware system to structure the digital chaotic signal generator includes: Xilinx Spartan 3 XC3S400-F-Core FPGA development board, the external D/A converter expansion board for the FPGA has more Hardware multipliers, and the Schematic diagram of D/A converter expansion board is shown in Figure 3.
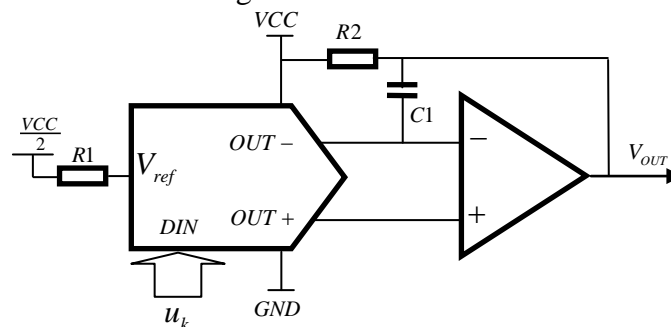

Fig.3 D/A converter circuit principle diagram

When we download the Digital logic algorithm to the processor, the output signal of μ can be test by the oscilloscope as shown in Fig.4. The plot of the signal has the same characteristic with software simulation.
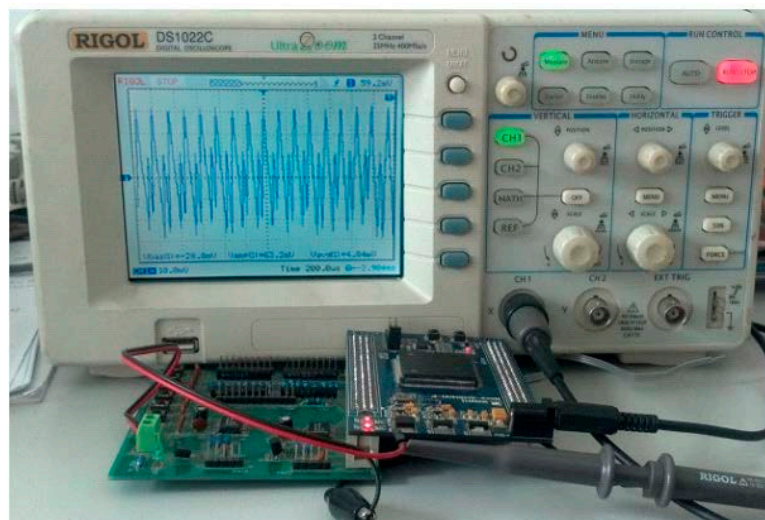

Fig.4 Chaotic signal generator and the waveform tested

Conclusion

Using digital signal processing method to generate chaotic signal based on the FPGA platform is proposed in this paper. The results show that, by the way of realization of hardware module, it can not only realize the generation of chaotic signal accurately and quickly, but also can be combined with the adjustment of parameters of chaotic model to modify the spectrum characteristic of chaotic signal to satisfy the requirement of   chaotic secure communication system flexibly.

Acknowledgement

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