Research on Synchronization Technology of OQPSK Signal Based on FPGA/DSP

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Abstract. The rapid development of information technology is promoting people's strong demand for perfect efficient digital communication system. Offset Quadraphase Shift Keying modulation technology is a constant-envelope digital modulation technology, which is the improved QPSK[1]. It overcomes the 180° phase jump of OQPSK，which has more advantages, such as fast power descent, low sidelobes and high spectrum efficiency, ect. Synchronization technology play a key role in high effectiveness of digital communication system. As the communication technology is developing continuously, the requirement is higher and higher in synchronization. So the research of synchronization is a wide attentive focus.

Introduction

For the design and implementation of digital communication system with better application performance, on one side, it needs to choose a better digital communication mode, on the other side, it needs a precise synchronous design. For the former, with many advantages, such as high frequency utilization-rate, QPSK is widely used nowadays. However, that mode has 180° phase jump among neighboring symbols, which makes the spectrum diffusion seriously[2]. That leads to interference between adjacent channels. Therefore, OQPSK emerges as the times require. For the later, it mainly achieves by frame synchronization, bit synchronization and carrier synchronization, which is the most important link. In addition, the design of the digital communication system should be based on the corresponding digital hardware platform to realize. DSP (digital signal processor), is a specialized microprocessor, which is used in digital signal processing. The FPGA (field programmable logic gate array), which improved the deficiency of the early programmable logic devices, has high programmable flexibility. Using the combined digital hardware platform of DSP and FPGA to realize the digital modulation demodulation and synchronization technology research has a very good value.

Synchronization Principle

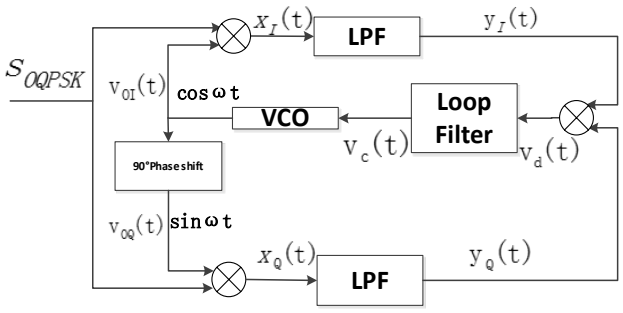

Fig. 1 Schematic diagram of costas loop

As shown in Fig. 1 is the principle diagram of costas loop.

Assumption that the in-phase and quardrature carrier signals, generated by the local NCO local, are expressed as:

$$v_{OI}(t) = \cos(\omega_c t + \theta_O(t)). \quad (1)$$

$$v_{OQ}(t) = -\sin(\omega_c t + \theta_O(t)). \quad (2)$$

Multiplier output signals can be expressed as:

$$x_I(t) = \frac{A}{2}\cos(\theta_n - \theta_0) + \frac{A}{2}\cos(2\omega_c t + \theta_n + \theta_0). \quad (3)$$

$$x_Q(t) = \frac{A}{2}\sin(\theta_n - \theta_0) - \frac{A}{2}\sin(2\omega_c t + \theta_n + \theta_0). \quad (4)$$

The two filter output branches can be expressed as:

$$y_I(t) = \frac{A}{2}\cos(\theta_n - \theta_0). \quad (5)$$

$$y_Q(t) = \frac{A}{2}\sin(\theta_n - \theta_0). \quad (6)$$

Multipling the two branches, get the signal as follow:

$$v_d(t) = \frac{A^2}{8}\sin[2(\theta_n - \theta_0)] \approx \frac{A^2}{4}(\theta_n - \theta_0). \quad (7)$$

The loop filter is a narrow band low pass filter, as a result, the output of the loop filter is equivalent to the dc component $v_d(t)$, the error of the control voltage $\theta_n - \theta_O$. So, the VCO is controlled by $\theta_n - \theta_O$ [3].Based on the above principle, the costas loop makes local carrier and receiving carrier as close as possible, reducing the relative error, and achieving the goal of carrier synchronization.

Frame synchronization is by using add frame head and identifying frame head to achieve the precise receiving of every frame code[4]. Bit synchronization is by comparing the local clock with the demodulated bit stream, to get the precise sampling clock.

System Design Scheme

That paper is based on FPGA (EP3C55F484C7N) and DSP (TMS320C6416) to realize the system design scheme. The whole system design includes seven links: the UART transceiver design, the FIFO data buffer, communication design between DSP and FPGA, A/D and D/A, OQPSK modulator, OQPSK demodulator, synchronization design. In that paper, it focuses on synchronization design implementation.

Carrier synchronization is the most important link of synchronization design. In that paper, it chooses costas loop to realize the carrier synchronization, mainly including the following several parts: NCO (digital controlled oscillator), multiplier, low-pass filter, the loop filter. All parts can be realized by using different types of IP core, which are mature function blocks designed by ALTERA corporation. However, the crucial works are parameter designs, which guarantees the reasonable matching between different parts. For the design of every filter, it uses sampling theory to calculate relative frequency, and use the principles shown in previous chapter to design relative parameters. Fig. 2 is NCO result block in Quartus II. Fig.3 is multiplyers' result block in Quartus II. Fig. 4 is FIR low-pass filter's result block in Quartus II. Fig. 5 is the loop filter result block in Quartus II.

Frame synchronization is continuously check the code stream and identify the frame head. Here use four bits barker code as the frame head. The design idea is as follow: put the data in turn into a dozen buffer; Constantly judge the four high bits. When the four high bits are 1101(meaning that the buffer has received a frame data), put the eight low buffer bits to data_send, and at the same time, set the

enable port to be high; When the four high bits of the buffer are not 1101, the enable signal is kept to zero. The frame synchronization block in Quartus II is shown in Fig. 6.

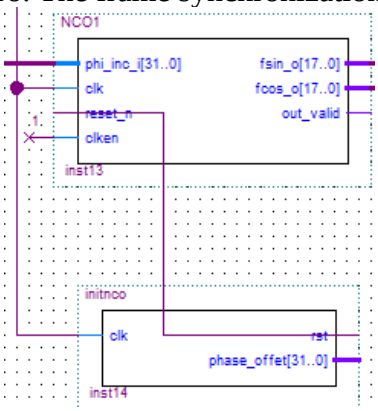

Fig. 2 NCO result block in Quartus II

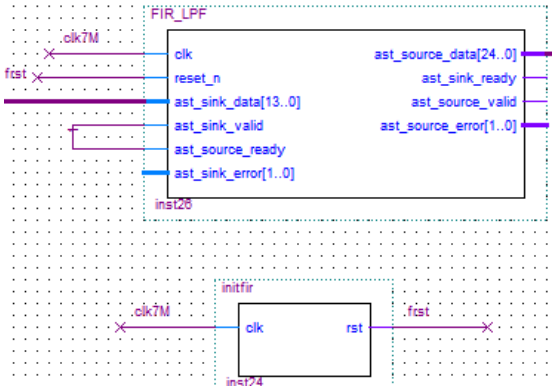

Fig.4 FIR low-pass filter's result block in Quartus II

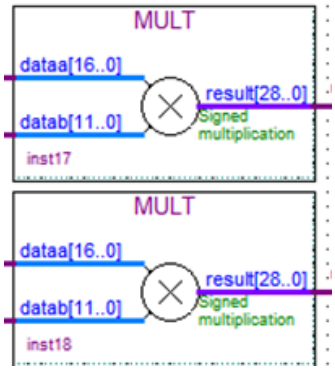

Fig. 3 Multiplyers' result block in Quartus II

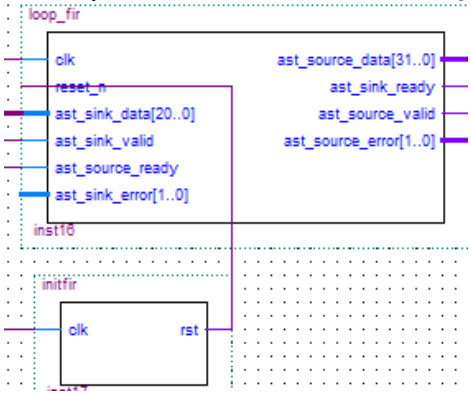

Fig.5 Loop filter's result block in Quartus II

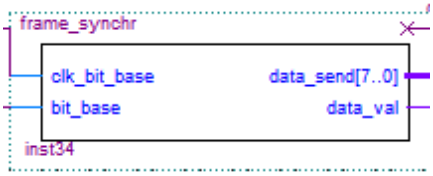

Fig. 6 Frame synchronization's result block

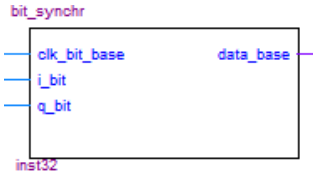

Fig.7 Bit synchronization's result block

The synchronous design's purpose is to appropriately sample to the in-phase and quadrature branches.The design idea is as follow: first, put the two branch datas in the in-phase and register respectively. Then, judge the sampling time, and when the value of counting register is 1, put the data from the quadrature register to data_base, at the same time, set the count register value to 0; When the count register value is 0, put the data from the in-phase register to data_base, at the same time, set the count register value to 1. Fig. 7 is bit synchronization's result block in Quartus II.

Experimental test results

Fig. 8 is the PC interface with data emission. In the experimental test, transmitter launched "abcdefg 123456" 2355 times. After demodulation, the digital information displays information in the PC interface ,as shown in Fig. 9. By observing the PC interface with receiving data can know the feasibility and correctness of that design systems, and that receiver received "abcdefg 123456" 2355 times.

Conclusion

Based on OQPSK, the paper gived synchronization design. With many tests, the results show that the system works stably and the various technical indexes achieve the target of design.

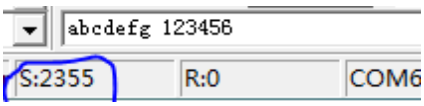

Fig. 8 PC interface with data emission

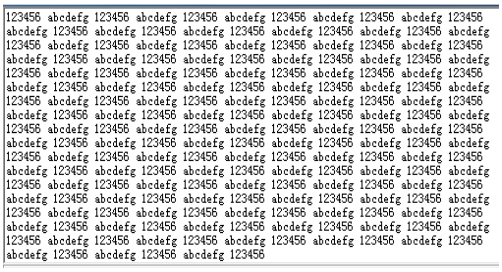
Fig. 9 PC interface with receiving data

Acknowledgments

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